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## 1. Basic Specifications

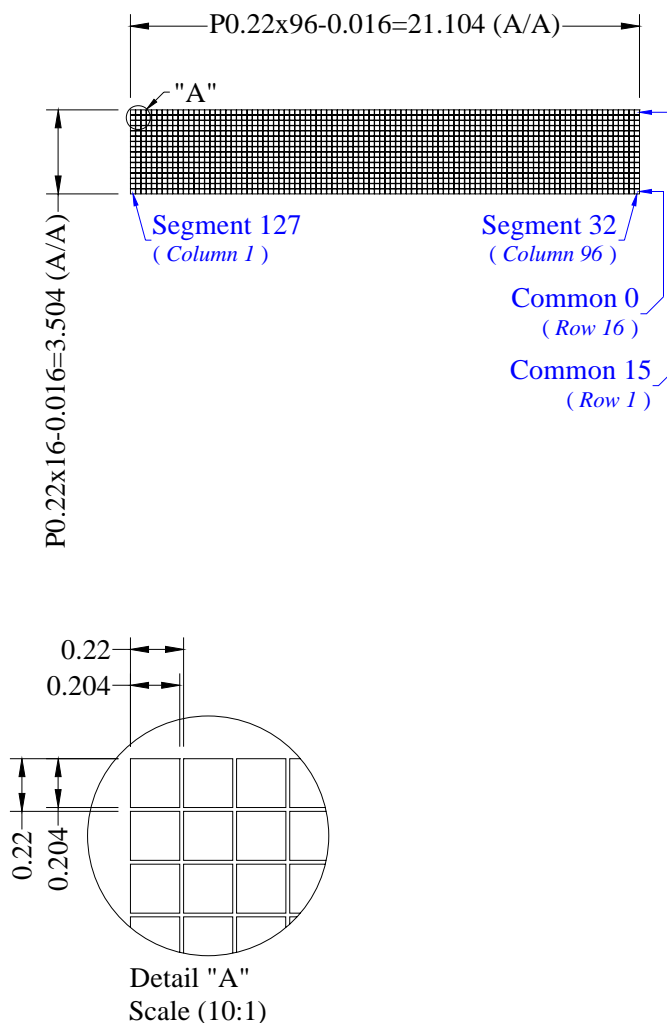
### 1.1 Display Specifications

- 1) Display Mode: Passive Matrix
- 2) Display Color: Monochrome (White/Blue)
- 3) Drive Duty: 1/16 Duty

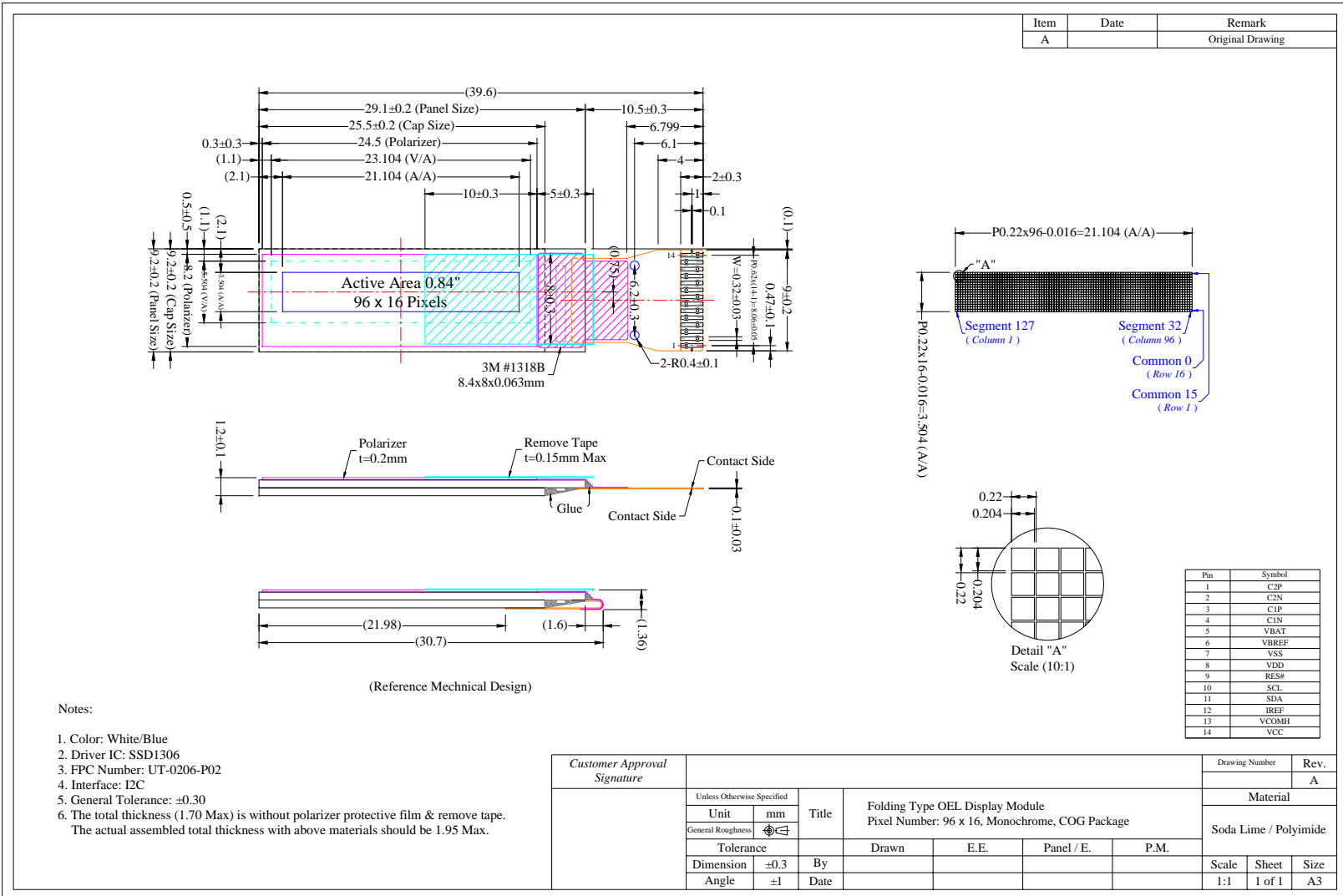
### 1.2 Mechanical Specifications

- 1) Outline Drawing: According to the annexed outline drawing
- 2) Number of Pixels:  $96 \times 16$
- 3) Panel Size:  $29.10 \times 9.20 \times 1.60$  (mm)
- 4) Active Area:  $21.104 \times 3.504$  (mm)
- 5) Pixel Pitch:  $0.22 \times 0.22$  (mm)
- 6) Pixel Size:  $0.204 \times 0.204$  (mm)
- 7) Weight: 0.89 (g)

### 1.3 Active Area & Pixel Construction



# 1.4 Mechanical Drawing



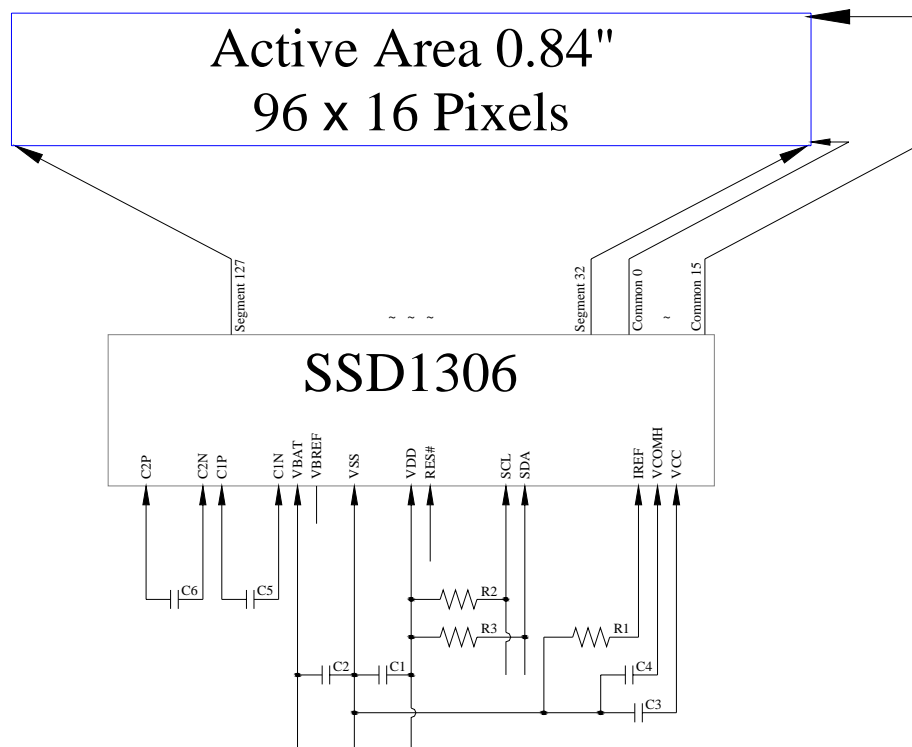
**Notes:**

1. Color: White/Blue
2. Driver IC: SSD1306
3. FPC Number: UT-0206-P02
4. Interface: I2C
5. General Tolerance: ±0.30
6. The total thickness (1.70 Max) is without polarizer protective film & remove tape. The actual assembled total thickness with above materials should be 1.95 Max.

## 1.5 Pin Definition

Pin Number	Symbol	Type	Function
<b>Power Supply</b>			
8	VDD	P	<b>Power Supply for Logic</b> This is a voltage supply pin. It must be connected to external source.
7	VSS	P	<b>Ground of OEL System</b> This is a ground pin. It also acts as a reference for the logic pins, the OEL driving voltages, and the analog circuits. It must be connected to external ground.
14	VCC	P	<b>Power Supply for OEL Panel</b> This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and VSS when the converter is used. It must be connected to external source when the converter is not used.
<b>Driver</b>			
12	IREF	I	<b>Current Reference for Brightness Adjustment</b> This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current lower than 12.5 $\mu$ A.
13	VCOMH	O	<b>Voltage Output High Level for COM Signal</b> This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.
<b>DC/DC Converter</b>			
5	VBAT	P	<b>Power Supply for DC/DC Converter Circuit</b> This is the power supply pin for the internal buffer of the DC/DC voltage converter. It must be connected to external source when the converter is used. It should be connected to VDD when the converter is not used.
6	VBREF	P	<b>Voltage Reference for DC/DC Converter Circuit</b> This pin is the internal voltage reference of booster circuit. It should be left open.
3 / 4 1 / 2	C1P / C1N C2P / C2N	I	<b>Positive Terminal of the Flying Inverting Capacitor</b> <b>Negative Terminal of the Flying Boost Capacitor</b> The charge-pump capacitors are required between the terminals. They must be floated when the converter is not used.
<b>Interface</b>			
9	RES#	I	<b>Power Reset for Controller and Driver</b> This pin is reset signal input. When the pin is low, initialization of the chip is executed.
10	SCL	I	<b>I2C Bus Clock Signal</b> The transmission of information in the I2C bus is following a clock signal. Each transmission of data bit is taken place during a single clock period of this pin.
11	SDA	I/O	<b>I2C Bus Data Signal</b> This pin acts as a communication channel between the transmitter and the receiver.

## 1.6 Block Diagram



Pins connected to MCU interface: RES#, SCL, and SDA

C1, C2, C5, C6: 1 $\mu$ F

C3, C4: 2.2 $\mu$ F

R1: 820k $\Omega$ ,  $R1 = (\text{Voltage at IREF} - VSS) / IREF$

R2, R3: 2k $\Omega$

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## 2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V <sub>DD</sub>	-0.3	4	V	1, 2
Supply Voltage for Display	V <sub>CC</sub>	0	11	V	1, 2
Operating Temperature	T <sub>OP</sub>	-30	70	°C	-
Storage Temperature	T <sub>STG</sub>	-40	80	°C	-

Note 1: All the above voltages are on the basis of “VSS = 0V”.

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. “Optics & Electrical Characteristics”. If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

### 3. Optics & Electrical Characteristics

#### 3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	$L_{br}$	With Polarizer	100	120	-	cd/m <sup>2</sup>
C.I.E. (White)	(x)	Without Polarizer	0.26	0.32	0.34	
	(y)		0.29	0.33	0.37	
Dark Room Contrast	CR		-	>2000:1	-	
View Angle			>160	-	-	degree

\* Optical measurement taken at  $V_{DD} = 2.8V$ ,  $V_{CC} = 7.25V$ .  
Software configuration follows Section 4.4 Initialization.

#### 3.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	$V_{DD}$	-	1.65	2.8	3.3	V
<i>Supply Voltage for DC/DC</i>	$V_{BAT}$	<i>Internal DC/DC Enable</i>	<i>3.3</i>	-	<i>4.2</i>	<i>V</i>
<i>Supply Voltage for Display (Generated by Internal DC/DC)</i>	$V_{CC}$	<i>Note 3</i>	<i>7</i>	<i>7.25</i>	<i>7.5</i>	<i>V</i>
High Level Input	$V_{IH}$	-	$0.8 \times V_{DD}$	-	$V_{DD}$	V
Low Level Input	$V_{IL}$	-	0	-	$0.2 \times V_{DD}$	V
High Level Output	$V_{OH}$	$I_{OUT} = 100\mu A, 3.3MHz$	$0.9 \times V_{DD}$	-	$V_{DD}$	V
Low Level Output	$V_{OL}$	$I_{OUT} = 100\mu A, 3.3MHz$	0	-	$0.1 \times V_{DD}$	V
Operating Current for $V_{DD}$	$I_{DD}$	-	-	180	300	$\mu A$
<i>Operating Current for <math>V_{BAT}</math> (<math>V_{CC}</math> Generated by Internal DC/DC)</i>	$I_{BAT}$	<i>Note 4</i>	-	<i>7.5</i>	<i>9.4</i>	<i>mA</i>
		<i>Note 5</i>	-	<i>12.6</i>	<i>15.8</i>	<i>mA</i>
Sleep Mode Current for $V_{DD}$	$I_{DD, SLEEP}$	-	-	1	5	$\mu A$
Sleep Mode Current for $V_{CC}$	$I_{CC, SLEEP}$	-	-	1	5	$\mu A$

Note 3: Brightness ( $L_{br}$ ) and Supply Voltage for Display ( $V_{CC}$ ) are subject to the change of the panel characteristics and the customer's request.

*Note 4:  $V_{DD} = 2.8V$ ,  $V_{CC} = 7.25V$ , 50% Display Area Turn on.*

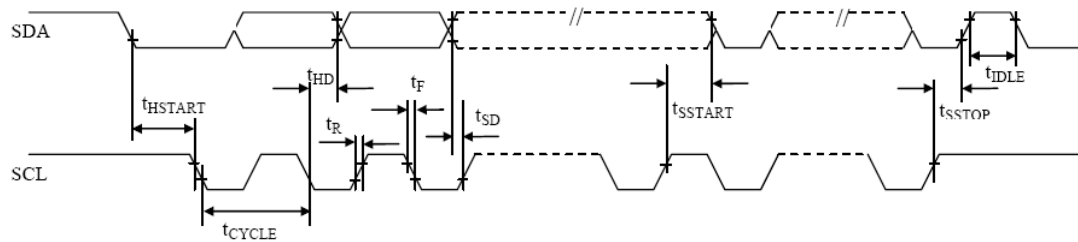
*Note 5:  $V_{DD} = 2.8V$ ,  $V_{CC} = 7.25V$ , 100% Display Area Turn on.*

\* Software configuration follows Section 4.4 Initialization.

### 3.3 AC Characteristics

Symbol	Description	Min	Max	Unit
$t_{\text{cycle}}$	Clock Cycle Time	2.5	-	us
$t_{\text{HSTART}}$	Start Condition Hold Time	0.6	-	us
$t_{\text{HD}}$	Data Hold Time (for “SDA <sub>OUT</sub> ” Pin)	0	-	ns
	Data Hold Time (for “SDA <sub>IN</sub> ” Pin)	300		
$t_{\text{SD}}$	Data Setup Time	100	-	ns
$t_{\text{SSTART}}$	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	us
$t_{\text{SSTOP}}$	Stop Condition Setup Time	0.6	-	us
$t_{\text{R}}$	Rise Time for Data and Clock Pin		300	ns
$t_{\text{F}}$	Fall Time for Data and Clock Pin		300	ns
$t_{\text{IDLE}}$	Idle Time before a New Transmission can Start	1.3	-	us

\* ( $V_{\text{DD}} - V_{\text{SS}} = 2.8\text{V}$ ,  $T_{\text{a}} = 25^{\circ}\text{C}$ )





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## 4. Functional Specification

### 4.1. Commands

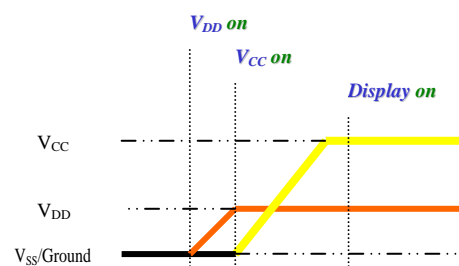
Refer to the Technical Manual for the SSD1306

### 4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

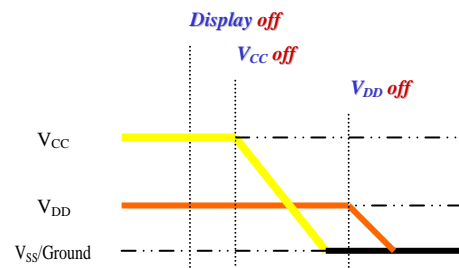
#### 4.2.1 Power up Sequence:

1. Power up  $V_{DD}$
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up  $V_{CC}$
6. Delay 100ms  
(When  $V_{CC}$  is stable)
7. Send Display on command



#### 4.2.2 Power down Sequence:

1. Send Display off command
2. Power down  $V_{CC}$
3. Delay 100ms  
(When  $V_{CC}$  is reach 0 and panel is completely discharges)
4. Power down  $V_{DD}$



### 4.3 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

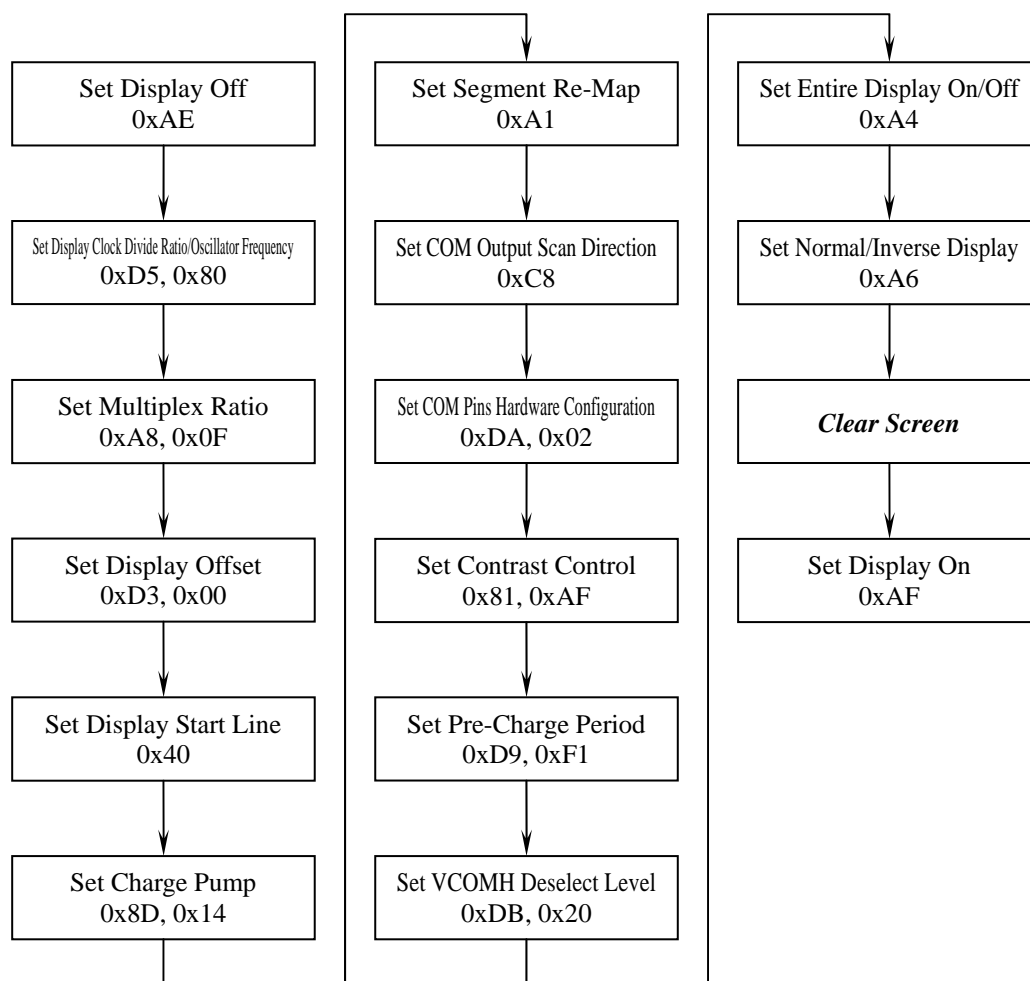
1. Display is OFF
2. 128×64 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

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## 4.4 Actual Application Example

Command usage and explanation of an actual example

<Initialization>



If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

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## 5. Reliability

### 5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The operational functions work.
Low Temperature Operation	-30°C, 240 hrs	
High Temperature Storage	80°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 120 hrs	
Thermal Shock	-40°C ⇔ 85°C, 24 cycles 60 mins dwell	

- \* The samples used for the above tests do not include polarizer.
- \* No moisture condensation is observed during tests.

### 5.2 Lifetime

End of lifetime is specified as 50% of initial brightness reached.

Parameter	Min	Max	Unit	Condition	Notes
Operating Life Time	10,000	-	hr	120 cd/m <sup>2</sup> , 50% Checkerboard	6
Storage Life Time	20,000	-	hr	T <sub>a</sub> = 25°C, 50% RH	-

Note 6: The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

### 5.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

## 6. Outgoing Quality Control Specifications

### 6.1 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	$23 \pm 5^{\circ}\text{C}$
Humidity:	$55 \pm 15\% \text{RH}$
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	$\geq 50 \text{ cm}$
Distance between the Panel & Eyes of the Inspector:	$\geq 30 \text{ cm}$
Finger glove (or finger cover) must be worn by the inspector.	
Inspection table or jig must be anti-electrostatic.	

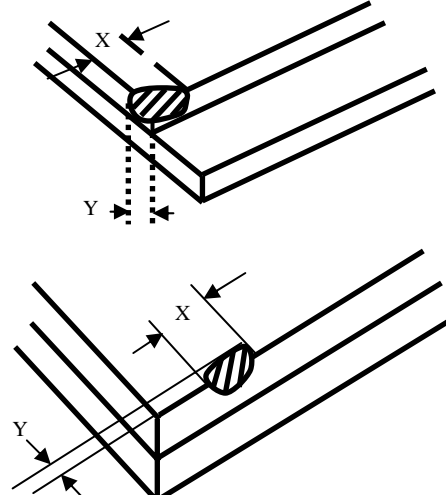
### 6.2 Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

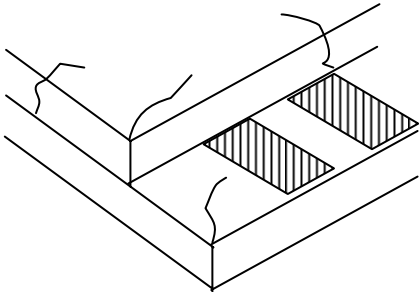

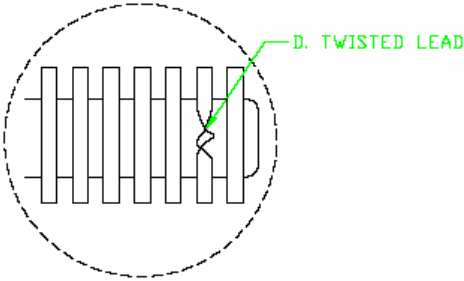
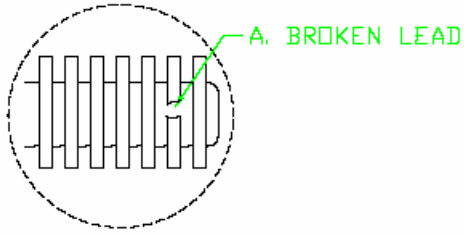
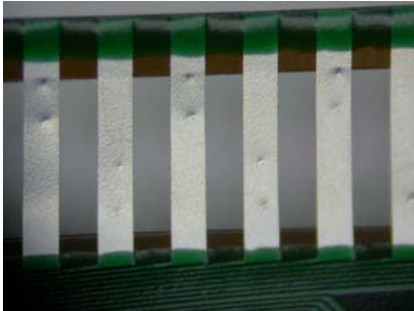
### 6.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

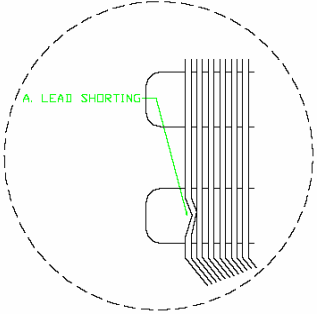
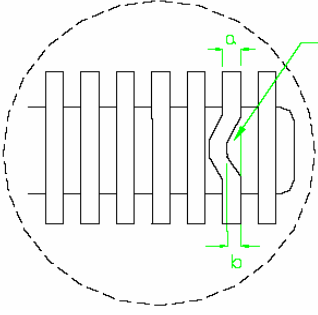
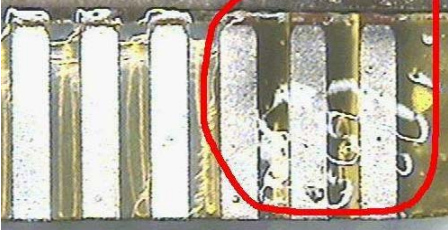
#### 6.3.1 Cosmetic Check (Display Off) in Non-Active Area

Check Item	Classification	Criteria
Panel General Chipping	Minor	<p><math>X &gt; 6 \text{ mm}</math> (Along with Edge)  <math>Y &gt; 1 \text{ mm}</math> (Perpendicular to edge)</p> 

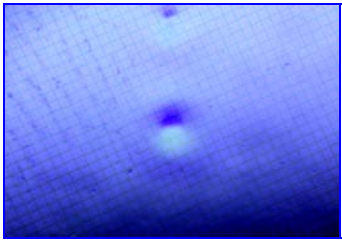
6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check Item	Classification	Criteria
Panel Crack	Minor	<p>Any crack is not allowable.</p>  <p>A 3D perspective diagram showing a rectangular panel with a crack running along one of its edges. The crack is shown as a jagged line that penetrates the surface of the panel.</p>
Copper Exposed (Even Pin or Film)	Minor	<p>Not Allowable by Naked Eye Inspection</p>
Film or Trace Damage	Minor	 <p>A close-up photograph of a yellow printed circuit board (PCB) showing a circular hole or damage in the copper film or trace area.</p>
Terminal Lead Twist	Minor	<p>Not Allowable</p>  <p>A diagram showing a row of terminal leads. One lead is circled with a dashed line and labeled 'D. TWISTED LEAD' with a green arrow pointing to a lead that is twisted or bent at an angle.</p>
Terminal Lead Broken	Minor	<p>Not Allowable</p>  <p>A diagram showing a row of terminal leads. One lead is circled with a dashed line and labeled 'A. BROKEN LEAD' with a green arrow pointing to a lead that is broken or fractured.</p>
Terminal Lead Prober Mark	Acceptable	 <p>A photograph showing a row of terminal leads with green solder masks. There are small, dark marks on the leads, which are identified as prober marks.</p>

6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

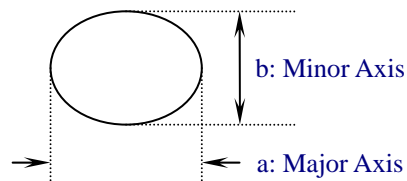
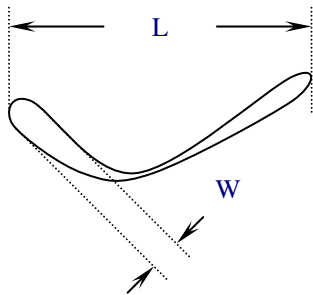
Check Item	Classification	Criteria
Terminal Lead Bent (Not Twist or Broken)	Minor	<p>NG if any bent lead cause lead shorting.</p> 
	Minor	<p>NG for horizontally bent lead more than 50% of its width.</p> 
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

6.3.2 Cosmetic Check (Display Off) in Active Area

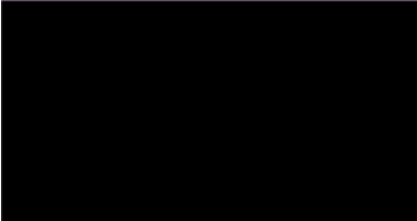
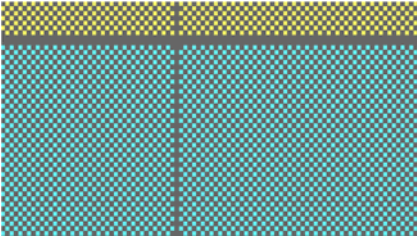
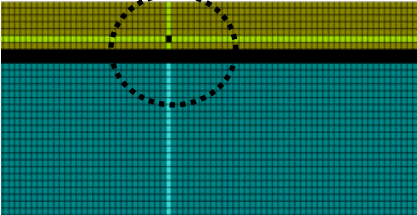
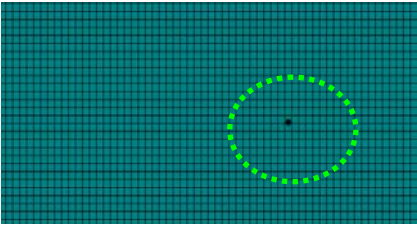
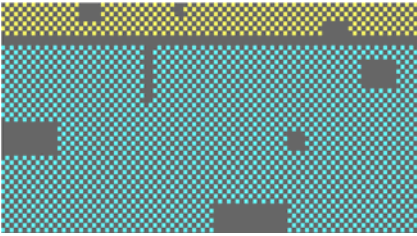
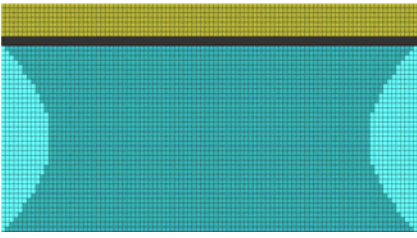
Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	$W \leq 0.1$ Ignore $W > 0.1, L \leq 2$ $n \leq 1$ $L > 2$ $n = 0$
Dirt, Black Spot, Foreign Material, (On Polarizer)	Minor	$\Phi \leq 0.1$ Ignore $0.1 < \Phi \leq 0.25$ $n \leq 1$ $0.25 < \Phi$ $n = 0$
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	$\Phi \leq 0.5$ → Ignore if no Influence on Display $0.5 < \Phi$ $n = 0$ 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

\* Protective film should not be tear off when cosmetic check.

\*\* Definition of W & L &  $\Phi$  (Unit: mm):  $\Phi = (a + b) / 2$

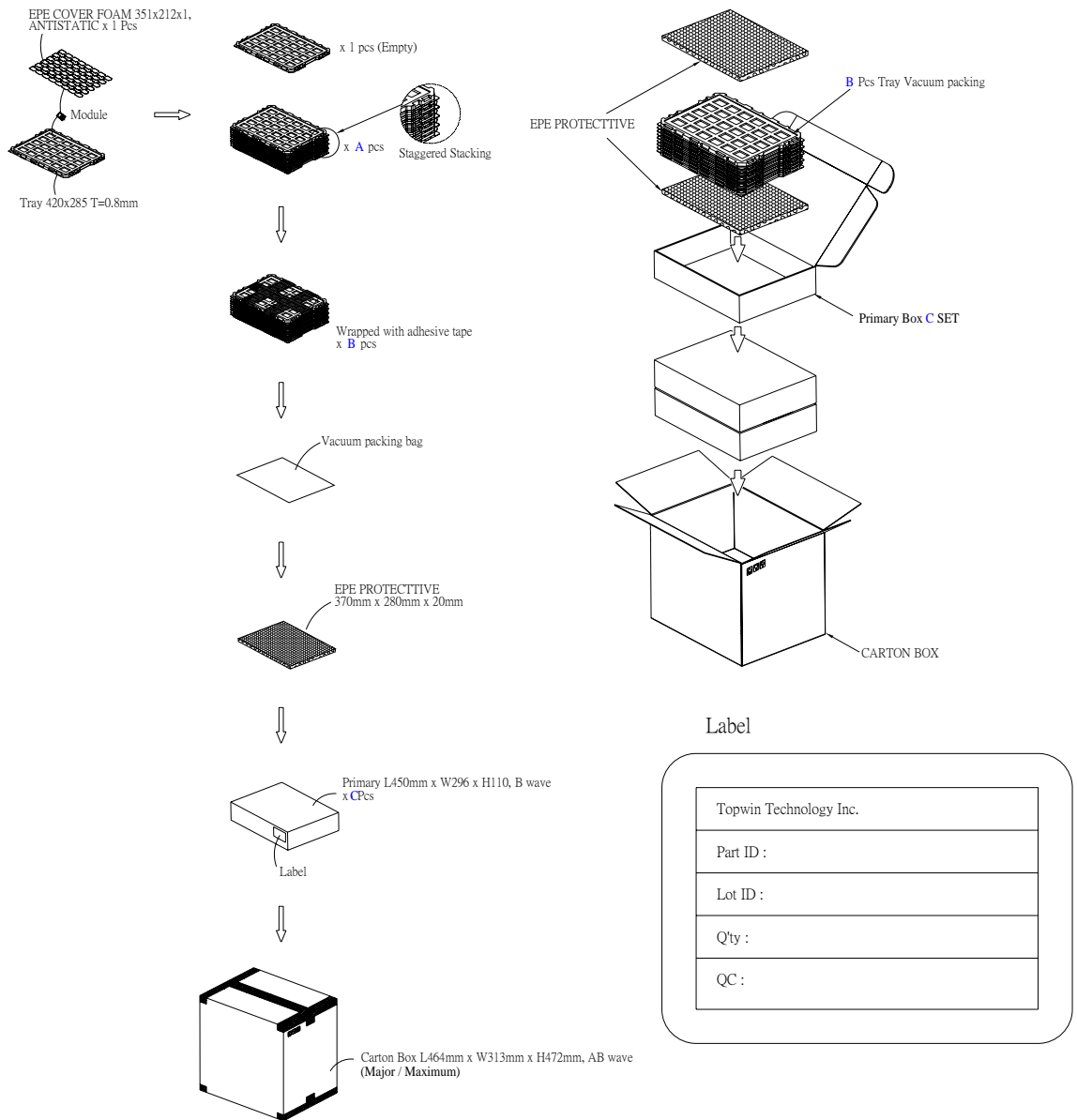


6.3.3 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Flicker	Major	Not Allowable
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	



## 7. Package Specifications



Item	Quantity
Holding Trays (A)	15 per Primary Box
Total Trays (B)	16 per Primary Box (Including 1 Empty Tray)
Primary Box (C)	1~4 per Carton (4 as Major / Maximum)

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## 8. Precautions When Using These OEL Display Modules

### 8.1 Handling Precautions

- 1) Since the display panel is being made of glass, do not apply mechanical impacts such as dropping from a high position.
- 2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
- 3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
- 4) The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
- 5) When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.

\* Scotch Mending Tape No. 810 or an equivalent

Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.

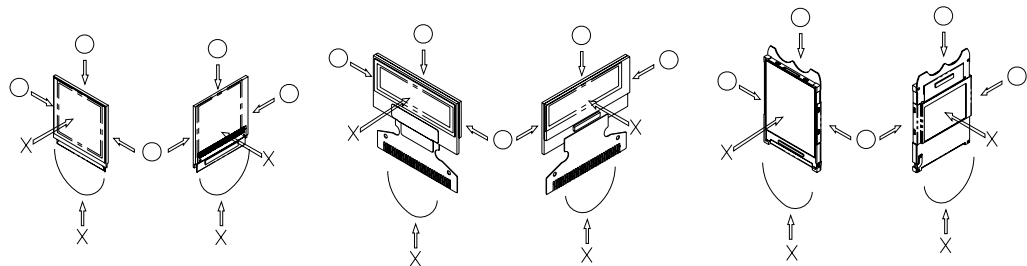
Also, pay attention that the following liquid and solvent may spoil the polarizer:

\* Water

\* Ketone

\* Aromatic Solvents

- 6) Hold OEL display module very carefully when placing OEL display module into the system housing. Do not apply excessive stress or pressure to OEL display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



- 7) Do not apply stress to the LSI chips and the surrounding molded sections.
- 8) Do not disassemble nor modify the OEL display module.
- 9) Do not apply input signals while the logic power is off.
- 10) Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
  - \* Be sure to make human body grounding when handling OEL display modules.
  - \* Be sure to ground tools to use or assembly such as soldering irons.
  - \* To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
  - \* Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.

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- 11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
  - 12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

## **8.2 Storage Precautions**

- 1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps, etc. and, also, avoiding high temperature and high humidity environments or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Topwin Technology Inc.)  
At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
- 2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

## **8.3 Designing Precautions**

- 1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
- 2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
- 3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
- 4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
- 5) As for EMI, take necessary measures on the equipment side basically.
- 6) When fastening the OEL display module, fasten the external plastic housing section.
- 7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
- 8) The electric potential to be connected to the rear face of the IC chip should be as follows: SSD1306  
\* Connection (contact) to any other potential than the above may lead to rupture of the IC.

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#### 8.4 Precautions when disposing of the OEL display modules

- 1) Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

#### 8.5 Other Precautions

- 1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur. Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
- 2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
  - \* Pins and electrodes
  - \* Pattern layouts such as the FPC
- 3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
  - \* Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
  - \* Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.
- 4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
- 5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.