13.56MHz Non-contact card reader IC

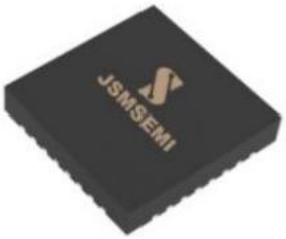
1 Product overview

MFRC 522 Is a widely used contactless card reader chip that integrates a variety of non-connections under 13.56MHz

Touch communication mode and protocol, have a very high degree of technical integration.

2. Functional features

- The reader mode supports the ISC / IEC 14443A standard
- The reader mode supports the ISO / IEC 14443B standard
- Highly integrated demodulation and decoding of the analog circuits
- It takes only a few external devices to connect the output drive to the antenna
- In reader mode, typical operating distances are up to 70mm, depending on the clip design and power supply
- Supported host interface
  > I2C interface, fast mode rate up to 400k, high speed mode up to 3400k
  The UART interface, up to 1228.8k
  > SPI interface with a maximum rate of 10 Ml



- 64-byte FIFO buffer for receiving and sending
- Flexible interrupt mode
- Low-power consumption of the hardware power-lo
- Support for software power loss mode
- MFRC523 supports LPCD functionality
- programmable timer
- Internal oscillator, connected to the 27:12 MHz crystal
- 2.5V-5Y, wide-range power supply voltage
- The CRC coprocessor
- Programmable I / 0 tube pins

A wide range of applications, in attendance, access control, public transportation, canteen dining, water and electricity recharge,

Portable handheld equipment, various member systems and other aspects of the comprehensive application, has a strong system application scalability.

MFRC522

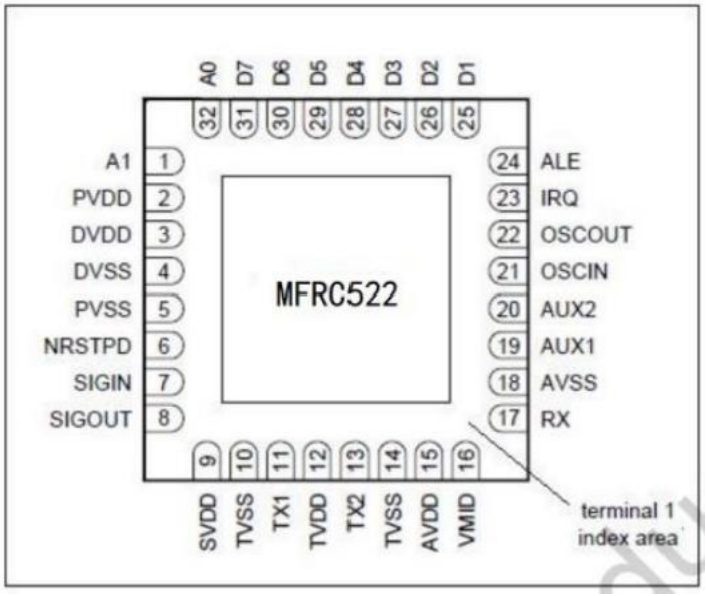


Figure 1 QFN 32, the package pipe pin diagram

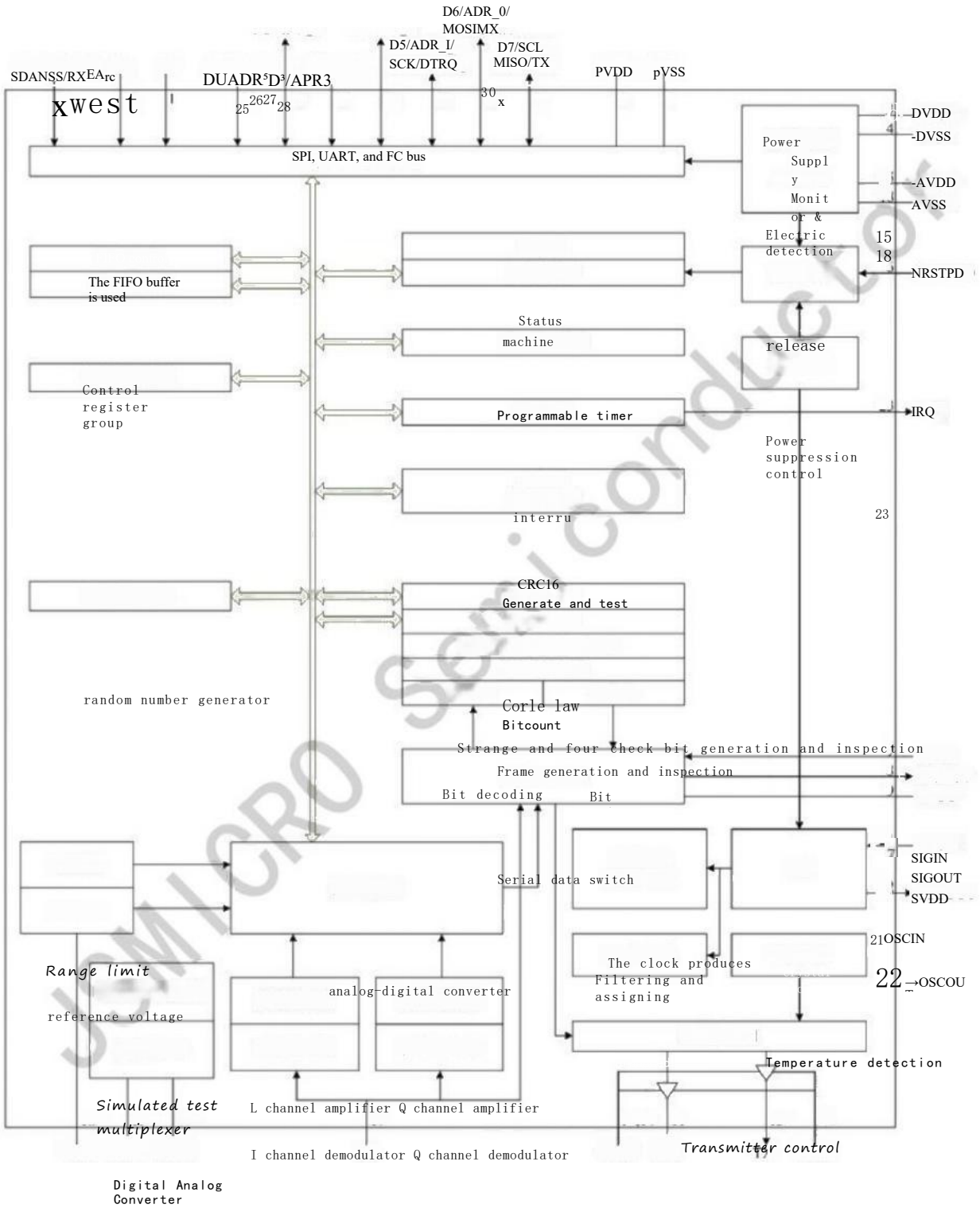
4. Pin configuration and functionality

Table 1 Note of pipe feet

Pipe foot number	Tube foot name	type	Pipe foot description
1	A1	I	address line
2	PVDD	P	Feet power supply
3	DVDD	P	Digital power supply
4	DVSS	G	Digitally
5	PVSS	G	Pipe foot power supply ground
6	NRSTPD	I	Return pin: at a low level, the internal function module including the oscillator stops working, and the input pin is disconnected from the outside. The rising edge on the pin can be used to open the internal reset phase.
7	SIGIN	I	Communication interface input: receiving digital data stream and serial data stream
8	SIGOUT	0	Communication interface output: output serial data flow
9	SVDD	P	S ℃ pin power supply: supply power to the S ℃ pin
10	TVSS	G	The ground of the transmitter TX 1 and TX 2 output levels
11	TX1	0	Carrier transmission tube pin 1
12	TVDD	P	Send the drive power supply
13	TX2	0	Carrier transmission tube pin 2
14	TVSS	G	Send the drive power supply ground

Pipe foot number	Tube foot name	type	Pipe foot description
15	AVDD	P	Analog power supply
16	VMID	P	Internal reference voltage
17	RX	I	RF signal input
18	AVSS	G	Simulated to
19	AUX1	O	Auxiliary output used for testing
20	AUX2	O	Auxiliary output used for testing
21	OSCIN	I	Anti-phase amplifier input; also an input to the external clock. The pin can also be used as an input to an external clock (fosc=27.12MHz)
22	OSCOUT	O	Crystal anti reverse phase amplifier output
23	IRQ	O	Interrupt request output: indicates an interrupt event
24	ALE	I	Address latch enables: the AD0-AD5 latches to the internal address latch at a high level
25-31	D1-D7	I/O	8-bit bidirectional data bus Note: The 8-bit parallel interface is not supported Note: If the main controller selects I ℃ as the digital main controller interface, these pins can be used to define the PC address Note: For serial interfaces, these pins can be used as test signals or I / O
32	A0	I	address line

5. Functional block diagram



16 19 20
VMID AUxi AUx2

2
RX

Figure . unctional block diagram
Figure]

MERC522

6 Functional description

MFRC 522 When working in the reader mode, its transmission module supports ISO / IEC 14443 A and ISO / IEC 14443 B standard, and can adopt a variety of transmission rates and modulation methods.

MFRC522 Support for the following working modes:

· Support ISO / IEC 14443A, ISO / IEC 14443B, reader / writer mode

These modes support different transmission rates and modulation methods, and these several different modes are detailed in the following sections type.

Note: All the modulation coefficients and modulation modes mentioned in this chapter are system parameters. This means that, besides the IC setting, Proper antenna tuning is also needed to obtain the optimal performance.

6.1 ISO / IEC1443A function

Physical layer parameters are described in Table 2.

Table 2 Overview of the communication parameters of ISO / IEC 14443A readers

Communication direction	Signal category	transmission speed		
		106kBd	212kBd	424kBd
Card reader to card	modulate	100%ASK	100%ASK	100%ASK
	Bit coding	Modified Miller Code	Modified Miller Code	Modified Miller Code
	Long	128(13.56us)	64(13.56us)	32(13.56us)
Card to card reader	modulate	Subcarrier load modulation	Subcarrier load modulation	Subcarrier load modulation
	subcarrier frequency	13.56MHz/16	13.56MHz/16	13.56MHz/16
	Bit coding	Manchester encoding	BPSK	BPSK

6.2 ISO / IEC1443B function

MFRC 522, The reader IC fully supports the ISO 14443A and ISO 14443B standards. Refer to this information for technical details

The ISO14443's Part 1 to 4.

7 The MCU interface

7 .1 Controller interface detection

MFRC522 Support supports various microcontroller interfaces, such as SPI, I2C and UART. MFRC522 Can reset its interface, and can automatically detect the type of the current microcontroller interface that performs the power-up or hard reset. MFRC 522 Determine the microcontroller interface by controlling the logic level on the pin after the reset stage. Each interface
Connection combinations with fixed tube pins. Table 11 lists the different connection configurations:

Table 11 detects the connection methods for the different interface types

pin	interface type		
	UART(input)	SPI(output)	I²C-bus(I/O)
ALE	RX	NSS	SDA
A1	0	0	1
A0	0	1	EA
D7	TX	MISO	SCL
D6	MX	MOSI	ADR 0
D5	DTRQ	SCK	ADR 1
D4			ADR 2
D3			ADR 3
D2	-		ADR 4
D1			ADR 5

7 .2 Serial peripheral interface

MFRC 522 Supports the high-speed communication between the SPI interface and the host machine, and the interface can handle data rates of up to 10 Mbit / s. When communicating with the host, MFRC 522, as a slave, receives data from the peripheral host to set the register,
Send and receive the data related to the RF interface communication.

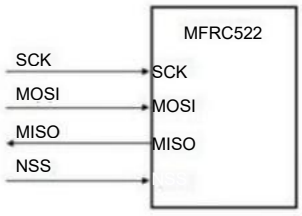


Figure 3 Connect to the host machine using the SPI interface

In the SPI, the MFRC 522 acts as the slave in the communication. The SPI clock signal SCK must be generated by the host. The data through

The MOSI lines are transferred from the host machine to the slave machine. Through MISO, the line data is sent back from the MFRC 522 to the host.

MOSI and MISO transmit every byte first. The data on the MOSI and MISO are on the clock

The ascending edge must remain the same, changing at the descending edge of the clock.

7.2.1 SPI, read the data

The data can be read out through the SPI interface using the structure shown in Table 12. This reads out n bytes of data.

The first byte sent defines the pattern and the address.

Table 12 MOSI and MISO byte order

pin	Byte 0	Bytes 1	Bytes 2	To	byte n	Bytes n + 1
MOSI	Address 0	Address 1	Address 2	……	address n	00
MISO	x	Data 0	Data 1		Data n-1	data n

[1] X= irrelevant Note: Send the highest bit first.

7.2.2 SPI to write the data

Data can be written to the MFRC 522 through the SPI interface using the structure shown in Table 13. This corresponds to an address n data bytes can be written.

The first byte sent defines the pattern and the address.

Table 13 MOSI and MISO bytes sequence

pin	Byte 0	Bytes 1	Bytes 2	To	byte n	Bytes n + 1
MOSI	Address 0	Data 0	Data 1	…	Data n-1	data n
MISO	x	x	x		x	x

[1] X= irrelevant Note: Send the highest bit first.

7.2.3 SPI address

Address bytes must be transferred in the following format.

The MSB bit of the first byte defines the usage pattern. The data is read from MFRC 522 when the MSB bit is set to 1, and the data is written to MFRC 522 when the MSB bit is set to 0. The bit 61 of the first byte defines the address, the LSB bit
It should be set to 0.

Table 14 Address byte format

7(MSB)	6	5	4	3	2	1	0(LSB)
1= Read	address						0
0= Write							

7.3 The UART interface

7.3.1, to connect to the host machine

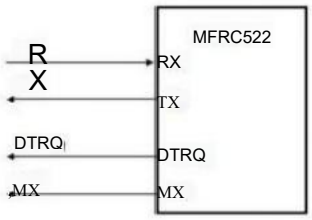


Figure 4 Connect to the microcontroller using the UART interface

Note: Zero the RS 232LineEn bit of the TestPinEnReg register

prohibit.

7.3.2 UART, transmission speed

Internal UART, the interface is compatible with the RS232 serial interface.

The default transfer rate is 9.6kBaud 。To change the transfer rate, the host controller must write a new transfer rate value to the SerialSpeedReg register. Bit BR _ TO [2:0] and bit BR _ T 1 [4:0]

The defined factors are used to set the transmission rate in the SerialSpeedReg.

Reference Table 15 for the settings of BR _ TO [2:0] and BR _ T 1 [4:0]. Table Table 16 lists some of the transmission rates and the corresponding ones

Register settings.

Table 15 Settings of the BRTO [2:0] and the BR T1 [4:0]

BR_Tn	Position 0	Position 1	Position 2	Position 3	Position 4	Position 5	Position 6	Position 7
BR_TO parameter	1	1	2	4	8	16	32	64
The BR _ TO range	1-32	33-64	33-64	33-64	33-64	33-64	33-64	33-64

Table 16 Optional UART transmission rates

Transmission Rate (kBd)	The SerialSpeedReg value		Transmission rate accuracy of (%)
	decimal system	hexadecimal	
7.2	250	FAh	-0.25
9.6	235	EBh	0.32
14.4	218	DAh	-0.25
19.2	203	CBh	0.32
38.4	171	ABh	0.32
57.6	154	9Ah	-0.25
115.2	122	7Ah	-0.25
128	116	74h	-0.06
230.4	90	5Ah	-0.25
460.8	58	3Ah	-0.25
921.6	28	ICh	1.45
1228.8	21	15h	0.32

[1] The results of the transmission speed errors in all described transmission speeds are less than 1.5% The optional transmission rates listed in Table 16 can be calculated using the following formula:

If BR_T0[2:0]=0:

$$transfer\ speed = \frac{27.12 \times 10^6}{(BR\_T0 + 1)}$$

If BR_TO[2:0]>0:

$$transfer\ speed = \left(\frac{27.12 \times 10^6}{(BR\_T1 + 33)} \right) \frac{}{2^{(BR\_T0-1)}}$$

MERC522

7.3.3 UART frame format

Table 17: UART frame format

Position	length	price
start bit	One	0
data bit	Eight	data
end bit	One	1

Note: For data and address bytes, the LSB bits must be sent first. Parity bits are not used during transmission.

read data:

Using the structure in Table 18, the data can be read out using the UART interface. The first byte sent defines the module Type and address.

Table 18 Read the data byte order

pin	Byte 0	Bytes 1
RX (tube pin 24)	address	
TX (tube pin 31)		Data 0

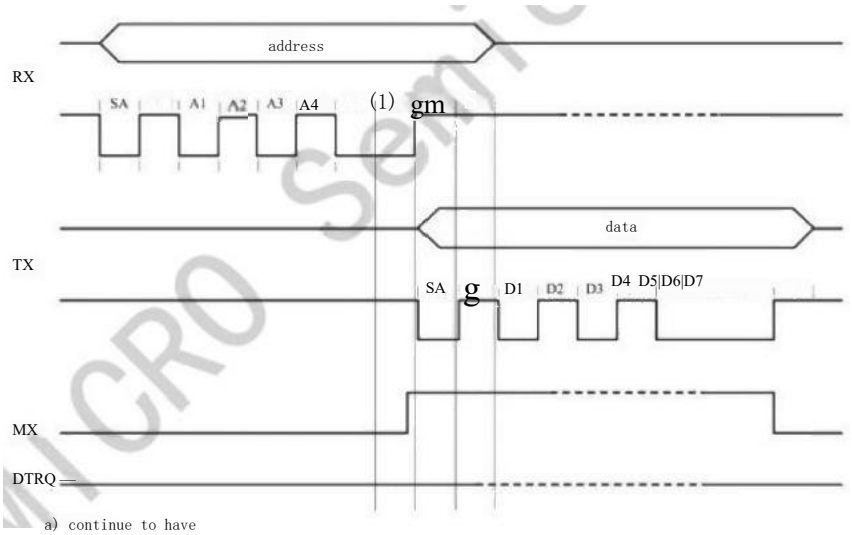


Figure 5 Time diagram of UART reading data

WD:

Using the structure in Table 19, the data can be written to the MFRC 522 using the UART interface. The first word that is sent to the same Section defines the patterns and addresses.

Table 19 writes the data byte order

pin	Byte 0	Bytes 1
RX (tube pin 24)	Address 0	Data 0
TX (tube pin 31)		Address 0

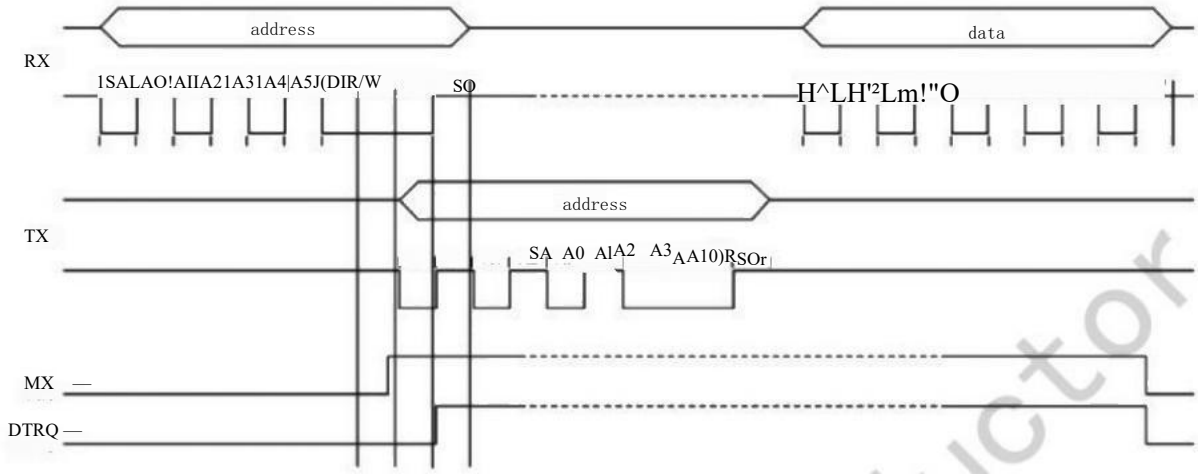


Figure 6 UART write data timing diagram

Note: After the address bytes reach the RX pin, the data bytes can be sent directly

Address Bytes: Address bytes are transferred in the following format:

The mode used for the MSB bit setting for the first byte. Data is read from the MFRC 522 when the MSB bit is set to 1. Write the data to the MFRC 522 when the MSB bit is set to 0. The bit 6 of the first byte is reserved for future use, the bit

5-1 defined address; see Table 20 for details.

Table 20 Address bytes

7(MSB)	6	5	4	3	2	1	0(LSB)
1= Read 0= Write	continue to have	address					

7.4 I2C interface

Supporting the I2C bus interface allows the host to connect to the MFRC 522 with fewer pins. I2C, the interface operation

Follow the I2C bus interface specification. This interface can only work in the slave mode.

7.4.1, to connect to the host machine

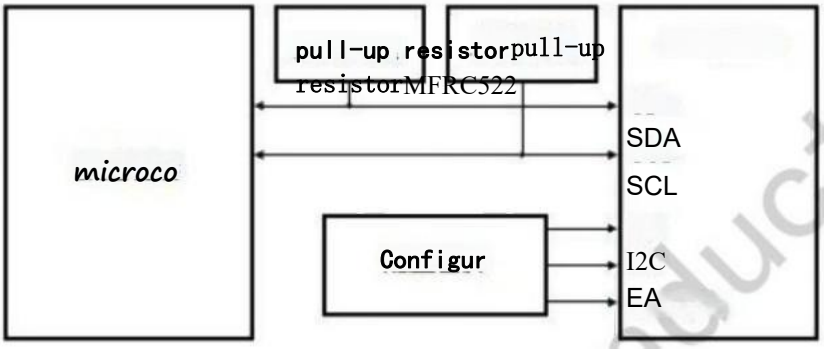


Figure 7 I ℃ bus interface

In standard mode, fast mode, and high speed mode, MFRC 522 can be used as a slave receiver or slave transmitter.

The SDA is a bidirectional data line, connected to a positive voltage by a pull-up resistance. Both SDA and SCL are high levels without transmitting data. The I2C bus travels at 100 kBd in standard mode, and at 400 kBd in fast mode,

3 in high-speed mode.4Mbit /s 。

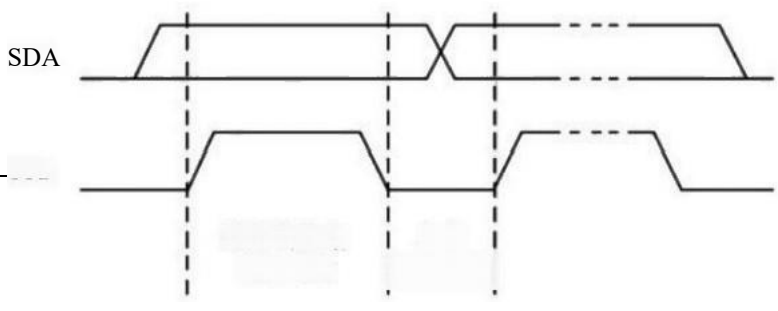
If the I2C bus interface is selected, the pin SCL and SDA pins have spike bursts that comply with the I2C interface specification

Suppression function.

7.4.2, data validity

The data on the SDA line remains constant during the high level of the clock period. Only if the clock signal on the SCL is

At a low level, the high level or low level state of the data line can change.



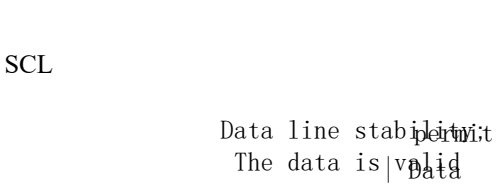


Figure 8 I The bit transmission of the ℃ bus

7.4.3 Start and stop conditions

To process data transfer for the I2C bus, start (S), and stop (P) conditions must be defined.

• The starting condition is defined as the high to low jump in the SDA line at the high SCL level.

• Stop condition is defined as a low to high jump on the SDA line at high SCL level.

Start and stop conditions are usually generated by the host. The host is considered busy after the starting condition; the host is in

The stop condition is considered back to be idle after a period of time.

If the repeat start condition (Sr) instead not the stop condition, the bus remains busy. At this time, the starting condition (S) and the repeat starting condition (Sr) function exactly the same. The S symbol is therefore used as a common one

Terms, which stand for the origin (S) and repeat origin (Sr) conditions.

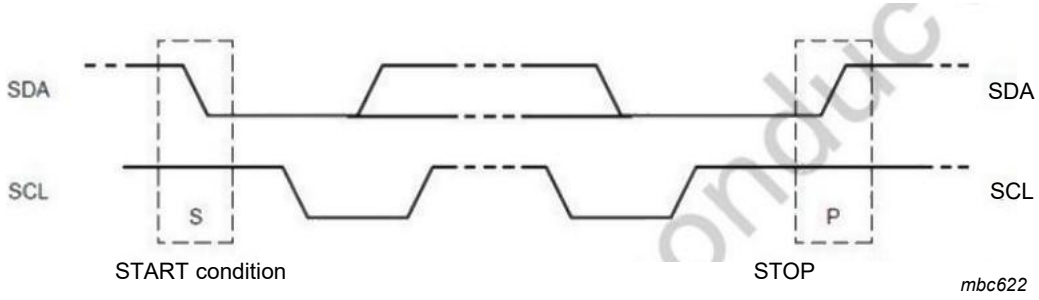


Figure 9. Start and stop conditions

7.4.4-byte format

Each byte must be followed by a reply bit. High level in front during data transmission. A word sent by a single data transmission

The number of sections is not limited, but it must conform to the read / write cycle format.

7.4.5 Response

Responses are forced into generation after the end of a data byte. The response corresponding clock pulse is generated by the host. The data transmitter releases the SDA line during the response clock pulse cycle (high level). During the response clock pulse, the connect

The receiver pulls down the SDA line to keep it low for the high level time of the clock pulse.

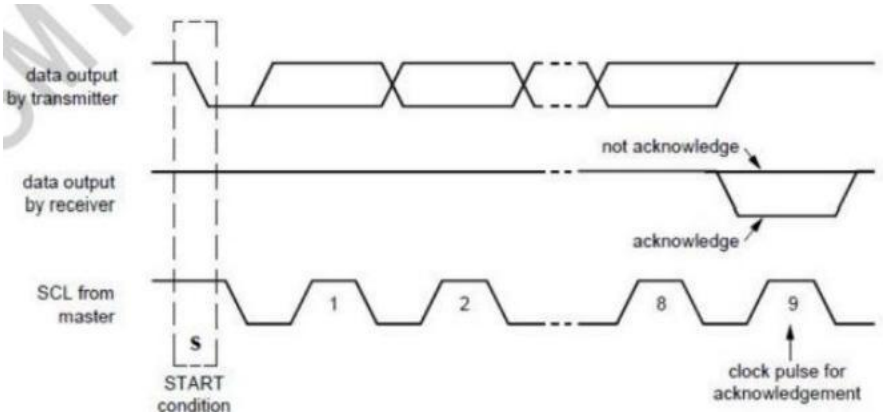


Figure 10 I2C bus response

The host can generate a stop (P) condition to terminate the transmission or a repeat start (Sr)

Condition to start a new transmission.

MFRC522

The primary receiver indicates the end of the data to the slave transmitter by generating no response after the last byte. From hair

The transmitter shall release the data line to allow the host to generate a stop (P) or repeat start (Sr) condition.

7.4.6 7-bit address

During the I2C bus address process, the first byte after the starting condition is used to determine the communication slave to be selected.

The I2C bus address is related to the definition of the EA pins. After NRSTPD pin release or power reset, the device root

The I2C bus address is determined according to the logical level of the EA pin.

If the EA pin is low, the high 4-bit of the device bus address is fixed to 0101b for all MFRC 522 devices. The remaining 3 bits of the device bus address (ADR _ 0, ADR _ 1, ADR _ 2) can be freely configured by the user

The sample can prevent the conflict with the other I2C devices.

If the EA pin is set to a high level, the ADR _ 0-ADR _ 5 is then determined entirely by the external pin in Table 13.

The ADR _ 6 is always set to 0.

In both modes, the external address codes are locked immediately after release of the reset condition. Use of tube pins is not considered

Further changes on the top. By configuring external connections, the address pin of the I2C bus can also be used as the output of the test signal.

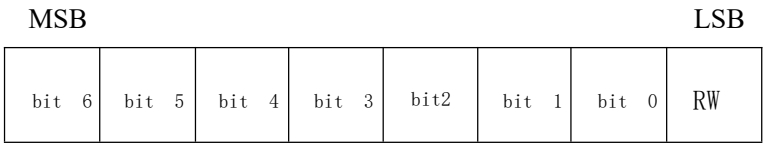


Figure Figure 11 The first byte after the starting condition

7.4.7 Register-write access

Using the following frame format available I2C, the interface writes data from the host controller to the mail specified in the MFRC 522 storage.

- The first byte of the frame is the device address following the I2C rules.
- The second byte is the register address, followed by n data bytes.

In one frame, all the data bytes are written to the same register address. This method can enable the FIFO fast access. Read / write bits should be set to 0.

7.4.8 Register-read access

Use the following frame format to read out the data for the specified registers in the MFRC 522.

- The first byte of the frame is the device address following the I2C rules.
- The second byte is the register address to be read.
- Read / write bit is 0.

After the write address operation completes, start the read access. The device address where the host sends the MFRC 522. In response, MFRC 522 sends the contents of the read access register. In one frame, all the data bytes are read out from the same register address. This method enables quick access or register queries from FIFO.

Read / write bits should be set to 1.

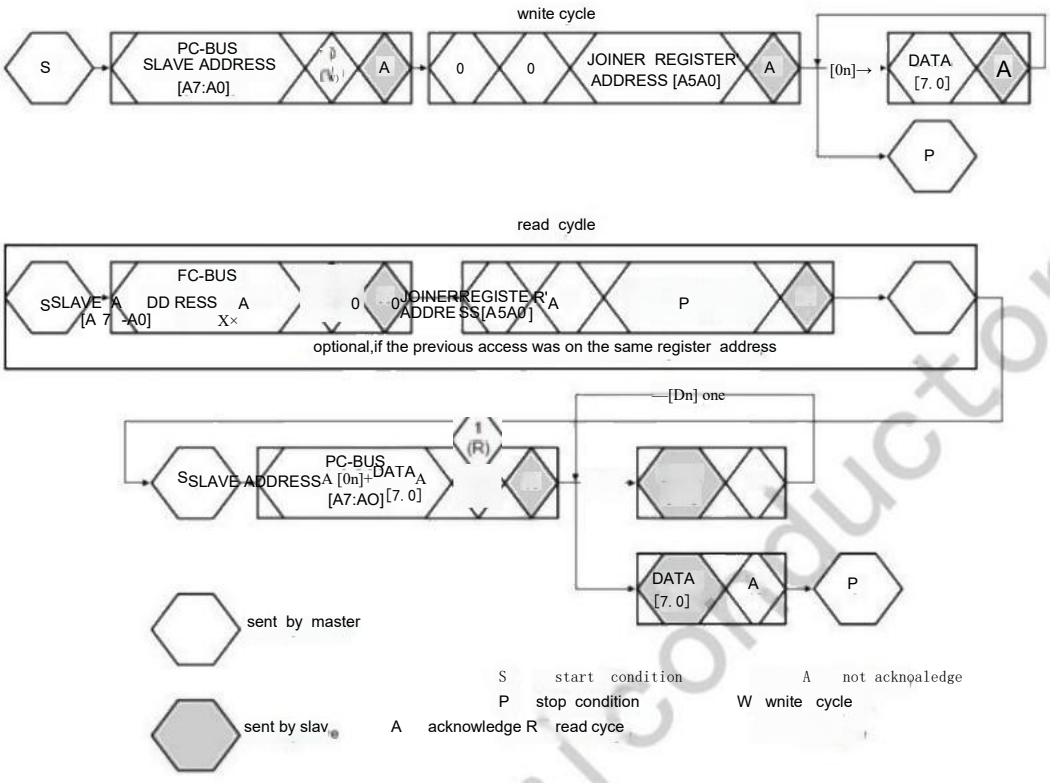


Figure 1 2. Register for read and write access

7.4.9 High Speed mode

In the high-speed mode (HS mode), the device transmits at a bit rate of up to 3 Mbit / s. In the mixing rate of the total.4

In the line system, it maintains bidirectional communication in fast or standard mode (F / S mode).

7.4.10 High-speed transmission

.4To achieve bit transmission rates of up to 3 Mbit 7s, the following improvements were made to the I2C bus operation.

- The input end of the device in high-speed mode has the spike pulse suppression function, and one application at the input end of SDA and SCL is provided

Mt triggers, which have different timing constants compared to the F / S mode.

- The output of the device in high speed mode controls the descending slope of the SDA and SCL signals, which are with the F / S mode

With different timing constants compared to the one.

7.4.11 Serial data transmission format in high-speed mode

The serial data transmission in the high-speed mode meets the I2C bus specification in the standard mode. Only if the following conditions are met are high

Fast mode transmission (all conditions in F / S mode):

- Starting conditions (S)
- 8-bit host code (00001 XXXb)
- Non-responsive position (A)

After the high speed mode starts, the host sends a repeat start condition (Sr), following the 7-bit slave address and

A read / write bit and then receive a response bit from the selected MFRC 522.

Continue data transfer in high speed mode after the next repeated start condition (Sr) and only switch back to F / S mode after the stop condition (P). To reduce host code overhead, hosts can link together a large number of high-speed transfers that are separated by repeated starting conditions (Sr).

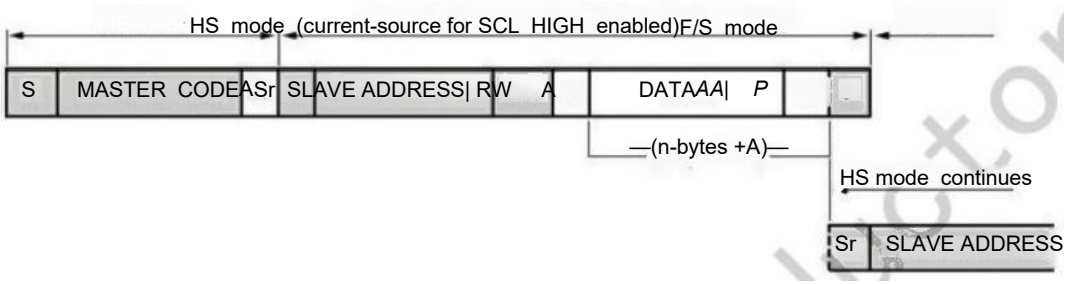


Figure 1 3 protocol conversion of I 2 C bus

7.4.12 F / S, switching between mode and HS mode

After reset and initialization, MFRC 522 works in fast mode (when the fast mode is down compatible with standard mode, it is actually F / S mode). The ated MFRC 522, identified to the "S 00001XXXA" sequence, will it

The internal circuit switches from fast mode setting to high speed mode setting.

Perform the following actions:

- The input filters for SDA and SCL were adjusted according to the spike pulse suppression requirements of HS mode.
- Adjust the slope control of the SDA output level.

For a system configuration without the other 12C device, it can be permanently switched to the HS mode by another method. Just set the I2CForceHS bit of the register to 1. After entering the permanent HS mode, this is no need to send the host code. This operation does not conform to the bus specification, and can only be used in the bus without other device connection

In the case of. Furthermore, spiking on the I2C bus.

7.4.13 The MFRC522 in the low-speed mode

MFRC 522 Fully downward compatible, connected to the F / S, mode I2C bus system.

Because it is not sent in this configuration

The host code is sent, so the device is in F / S mode and communicates at the rate of F / S mode.

A 7.5 8-bit parallel interface

MFRC 522 Support different types of 8-bit parallel interfaces in 2, Intel and Motorola compatibility modes.

7.5.1 Supported master control interface

MFRC 522 Supports direct connection to various microcontrollers. The following table shows the parallel interfaces supported by MFRC 522 type.

Table 21 Supported interface types

Supported interface type	highway	Independent address and data bus	The plex address and data bus
Independent read / write option (Intel compatible)	control	NRD, NWR, NCS	NRD, NWR, NCS, ALE
	address	A0...A3[..A5]	AD。…AD7
	data	D。…D7	AD。…AD7
Multiplex read / write option (Motorola concurrently)	control	R/NW, NDS, NCS	R/NW, NDS, NCS, AS
	address	A0...A3[..A5]	AD。…AD7
	data	D0…D7	AD0…AD7

8 Interrupt the request system

MFRC 522 The break is indicated by the IRq bit of the place register StatuslReg or the activated IRQ pin. IRQ

The signal of the pin enables the host to use the disconnection processing mechanism. This makes the software execution much more efficient.

8.1 Overview of the interrupt source

Table 28 lists the usable interruption bits, corresponding interruption sources and resulting conditions. The TimeHRq break bit of the ComlrqReg register indicates a break generated by the timer, in, when the timer is reduced from 1 to 0

The cut-off was placed.

The TxIRq bit of the ComlrqReg register indicates that the transmitter is complete. If the state changes from the sending data to the sending end frame, the transmitter automatically places the corresponding interrupt bit. The CRC coprocessor places the CRCIRq bit of the DivIrqReg register after processing all the data in the FIFO buffer, as indicated by the CRCReady position 1.

The RxIRq bit of the ComlrqReg register indicates the detected end of the received data. If an instruction is executed and the contents of the Command [3:0] bit of the CommandReg register become idle, the IdlelRq bit of the ComlrqReg register is placed.

At the HiAlert position 1 and the HiAlertIRq position bit of the ComlrqReg register, the FIFO buffer has reached the length indicated by the WaterLevel [5:0] bit.

FIFO buffer is indicated at LoAlert position 1 and the ComlrqReg register

The device has reached the length of WaterLevel [5:0] position.

The ErrIRq bit of the ComlrqReg register indicates that the contactless UART detected an error during sending or receiving. An error is generated when either position 1 in the ErrorReg register.

Table 22, Interruption source

interruptible identification	interrupt source	trigger action
TimerIRq	Timer unit	The timer counts from 1 to 0
TxIRq	transmitter	Data sent to an end

CRCIRq	CRC coprocessor	FIFO buffer
RxIRq	acceptor	End of data receiving
IdlelRq	ComIRQReg Register	The execution of the directive is over
HiAlertIRq	FIFO buffer	When the HFO buffer is fast to overflow
LoAlertIRq	FIFO buffer	When the HFO buffer is almost empty
ErrIRq	Non-contact-type UART	An error was detected

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9. Timer unit

MFRC 522 There is a timer unit that external hosts can use to handle timing tasks. The timer can make

As shown below

Any one of the timing / count configuration:

- Timeout Counter
- Watchdog counter
- stopwatch
- Programmable to trigger once
- Periodic triggers

The timer unit can be used to measure the time interval between two events or to indicate the occurrence of a specified event after a certain time. It can be triggered by the events explained below. The timer does not affect any internal events, for example, the timer timeout during data receiving does not affect the automatic processing of the receiving process. In addition, some are timer-related Bits can be used to generate interruptions.

The clock oscillation frequency of the timer is 13.56MHz, which is obtained by dividing the quartz crystal oscillator of 27.12MHz and so on. The timer consists of two stages: prefrequency and counting.

The predivider (TPrescaler) is a 12-bit counter. Its reloading value (TReloadVal _Hi [7:0] and TReloadVal _ Lo [7:0]) is between 0 and 4095 by TPrescaler _Hi of the TModeReg register [3:0] Bit and TPrescalerReg register TPrescaler _ Lo [7:0] to set.

The 16-bit reload value in the timer is defined in register TReloadReg to range from 0 to 65535.

The current value of the timer is shown in the register TCouterValReg.

When the count value reaches 0, an interrupt is automatically generated, indicated by placing the TimerIRQ bit of the CommonIRQReg register. If enabled, the IRQ pin will interrupt. The TimerIRQ bit can be placed and reset by the host. Depending on the configuration, the timer can stop running when counting to 0 or send TReloadReg

The value of the depository is restarted for counting as the initial value.

The status of the timer is indicated by the TRunning bit of the StatusIReg register.

The start and stop of the timer can be controlled by the TStartNow and TstopNow bits of the ControlReg register, respectively.

The timer can also be automatically activated by setting the TAuto bit of the TModeReg register to 1 to satisfy the specific

The agreement requires.

The delay time during the timing process is the reloading value plus 1.

The value of

For example, to get a 25us delay, 339 clock cycles and TPrescaler

In the value of the number 169. This configuration enables the counter to count to 65535 per 25us cycles.

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10 power-saving mode

10 .1 Hard power drop mode

When the pin NRSTPD is low, enter the hard drop mode. In this mode, turn off all internal power supplies, including the oscillator. All digital input buffer and input end separate and turn off their functions (except NRSTPD pins),
The output pins are also maintained at high or low levels.

10 .2 Soft power drop mode

The PowerDown bit of the CommandReg register is set to 1 and immediately enter the soft power drop mode. Turn off all internal power supplies, including the oscillator buffer. However, the digital input buffer does not separate from the input, and the function remains not
become different. The status of the digital output pin is unchanged.

During soft dropout, all register values, FIFO values and configuration remain unchanged.

After setting PowerDown bit to 0, exit soft power mode after 1024 clock cycles. PowerDown

The bit set to 0 does not clear it immediately, but automatically clear it after quitting the soft drop mode.

If an internal oscillator is used, it must be considered that it is a power supply supplied by the pin AVDD, after a period of time (Tosc) for the oscillator to stabilize and the internal logic to detect the clock cycle. When using serial UART communication, it is recommended to send 55h to MFRC 522, and the oscillator must remain stable before further access to the register. To ensure this, read access to address 0 is not performed until MFRC 522 responds to the read command with the last register content is address 0. This indicates that the MFRC522 can perform further operations.

10 .3 Transmitter power-out mode

The itter power off mode cuts off the internal antenna driver to close the RF field and can be done by setting TXControlReg

Register the TXIRFEn or TX 2RFEn bit of 0 to implement.

10.4LPCD pattern

MFRC 522 Internal integration of low power automatic card search and timing wake up function, card seeking time interval and card search time can be programmed, the card search process does not need

MCU operation, the card can interrupt the MCU. The LPCD functions in low power consumption

At the same time, it also realizes the card inspection, taking into account the power consumption and function.

11 The oscillator circuit

The clock of MFRC 522 is used as the clock reference for the system encoder and the decoder. Therefore, the stability of the clock frequency is an important factor to ensure the good performance of the system. For optimal performance, clock jitter must be minimized whenever possible.

It is best to use an internal oscillation buffer with a recommended circuit.

If external clock sources are used, the clock signal must be connected to the OSCIN pin. In this case, in particular

Note to verify the clock duty cycle, clock jitter and the quality of the clock signal.

12 MFRC522 register

12.1, the register bit

Depending on the register function, the register access conditions are also varied. In principle, has the same characteristics

The position is classified as the same group. Table Table 23 describes the access conditions for the registers.

Table 23. Features of the register bits

abbreviation	characteristic	description
r/w	Read / write	The microprocessor can read and write to these bits, and because they are only for control, their content is not affected by the internal state machine. For example, the microprocessor can read or write on the register ComlEnReg, but internally The state machine can only read the register and can not change their values.
dy	trends	The microprocessor can read or write these bits, but the internal state machine can also change the value of these registers. For example, the register CommandReg automatically changes certain values inside its instruction after its execution.
r	read only	The value of these registers can only be determined by the internal state. For example, the CRCReady bit can only represent the internal state, outside Neither part or internal state machine can change its value.
W	write only	The bit-read result of these registers is always 0.
RFU	_	These registers are reserved for future use, and it is best to write them all as 0.
RFT		These registers are reserved for future use or for production testing.

12.2 The register is registered

Table 24 Register overview

address	Register name	function
Page 0: Command and status register groups		
0h	PageReg	Page selection register
1h	CommandReg	Power drops and command registers
2h	ComlEnReg	Interrupt the request to control the register
3h	DivlEnReg	Interrupt the request to control the register

4h	ComlrqReg	Interrupt the request bit register
5h	DivIrgReg	Interrupt the request bit storage
6h	ErrorReg	Error state register for instruction execution
7h	StatuslReg	Communication status register
8h	Status2Reg	Receiver and transmitter status registers
9h	FIFODataReg	A 64-byte FIFO buffer
Ah	FIFOLevelReg	The FIFO buffer has stored the number of bytes in the registers
Bh	WaterLevelReg	FIFO buffer overflow and empty warning register

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Ch	ControlReg	Other items control the register
Dh	BitFramingReg	Adjustment register of the bit-facing frames
Eh	CollReg	Check the address of the first bit that produced the bit conflict
Fh	RFU	continue to have
Page 1: Command register group		
0h	PageReg	Page selection register
1h	ModeReg	Defines the registers for sending and receiving the common mode
2h	TxModeReg	Registers that define the data transfer rate and structure of the sending process
3h	RxModeReg	Defines that registers the data transfer rate and structure during the receiving process
4h	TxControlReg	Controls the registers of the antenna drive pins TX 1 and TX 2
5h	TxAutoReg	The sters that controls the antenna drive settings
6h	TxSelReg	Select the register for the internal signal source of the antenna driver
7h	RxSelReg	Select the register for the settings of the internal receiver
8h	RxThresholdReg	Select the register for the threshold of the bit decoder
9h	DemodReg	The register that defines the setting of the demodulator
Ah	FelNFC1Reg	A register that defines the effective length range of the received packet
Bh	FelNFC2Reg	A register that defines the effective length range of the received packet
Ch	MifNFCReg	Registers that control the communication between the ISO / IEC14443A and NFC target modes at the 106 kbit rate
Dh	ManualRCVReg	Allows manual tuning of the register of the internal receiver
Eh	TypeBReg	Configure the registers for the ISO / IEC14443B
Fh	SerialSpeedReg	Select the rate register for the serial UART interface
Page 2: Configure the register group		
0h	PageReg	Page selection register
1h	CRCResultReg	The MSB and LSB values calculated by the CRC are shown
2h		
3h	GsNOffReg	Drive the conductance register for modulation on the antenna pins TX 1 and TX 2 when the drive is off
4h	ModWidthReg	A setting register for controlling the modulation width
5h	TxBitPhaseReg	Adjust the phase register of the TX bit at the

		106 kbit rate
6h	RFCfgReg	Register sters for receiver gain and RF voltage
7h	GsNOnReg	Drive drives tance register on pins TX 1 and TX 2 for modulation on drive
8h	CWGsPReg	During no modulation, the antenna drives the pins TX 1 and TX 2 for modulation Conductor register
9h	ModGsPReg	During modulation, the antenna drives the electricity on the pins TX 1 and TX 2 for modulation Guide register
Ah	TModeReg	Set-up register of the internal timer
Bh	TPrescalerReg	

Ch Dh	TReloadReg	Defines the overloaded value register for a 16-bit timer
Eh Fh	TCounterValReg	Count value register of the 16-bit timer
Page 3: Test the register group		
0h	PageReg	Page selection register
1h	TestSel1Reg	Universal test signal configuration register
2h	TestSel2Reg	Configuration of the universal test signals and the PRBS control registers
3h	TestPinEnReg	Output drive enabling D0-D7 (Note: for serial interface only)
4h	TestPinValueReg	Define the value when pin D0-D7 when used as I / O bus
5h	TestBusReg	Status register of the internal test bus
6h	AutoTestReg	Digital self-check register
7h	VersionReg	Software version register
8h	AnalogTestReg	Fins AUX 1 and AUX 2 output registers
9h	TestDAC1Reg	The test value register of the TestDAC1
Ah	TestDAC2Reg	The test value register of the TestDAC2
Bh	TestADCReg	The 1 and Q channel registers in the ADC
Ch-Fh	RFT	Reserved for product testing

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13 of the instruction set

13.1 Overview

The operation of the MFRC 522 is determined by an internal state machine capable of executing a series of instructions. By writing the instruction code Enter the CommandReg register to execute the corresponding instructions.

13.2, general features

• In addition to the Transceive instruction, instructions that require a data stream or (data byte stream) immediately process the data of the FIFO buffer. When executing the Transceive instruction, by setting the StartSend of the BitFraming register
Bit to start the transmitter.

• Instructions requiring preset parameters are only on when the correct number of parameters is received from the FIFO buffer
Start running.

• FIFO buffer will not immediately clear up when instructions start. FIFO command parameters and data can be written into FIFO first
Start the instruction after the buffer.

• Instructions newly written into the CommandReg register will interrupt the instructions currently being executed.

13.3, the instruction overview

Table 25 for the instruction overview

instruct	instruction code	meaning
Idle	0000	No action; cancel the currently executed instruction
Config	0001	For configuring the FeliCa and NFCIP-1 communication
Generate RandomID	0010	Generates a 10-byte block of random ID data
CalcCRC	0011	Start the CRC coprocessor
Transmit	0100	Send the data from the FIFO buffer
NoCmdChange	0111	Do not interrupt the executing instructions to modify some bits in the CommandRe g register that do not affect the execution of the command, such as the PowerDown bit
Receive	1000	Start the receiver circuit
Transceive	1100	Send the data from the FIFO buffer to the antenna and automatically start the receiver after sending

AutoColl	1101	Handle FeliCa polling (card-only working mode) and ISO / IEC14443A conflict prevention C. Card-only working mode)
SoftReset	1111	soft reset

14. Electrical parameters

14.1, and the limit parameters

Table 26. Limit parameters

parameter	least value	crest value	unit
Vooa, Vooo, Pvoo, Svop	-0.5	+4.0	V
TVDD	-0.5	+5.5	V
Storage temperature	-40	85	℃
ESD(HBM)	_	2000	V
ESD(MM)	_	200	V

14.2 Main parameter and parameter index

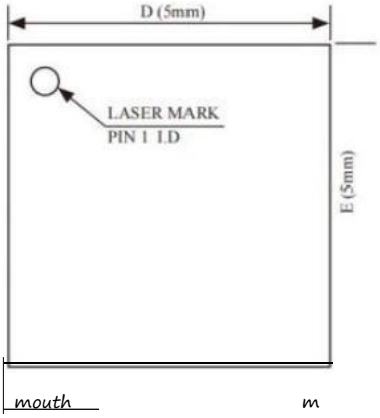
Table 27. Main parameters and indicators

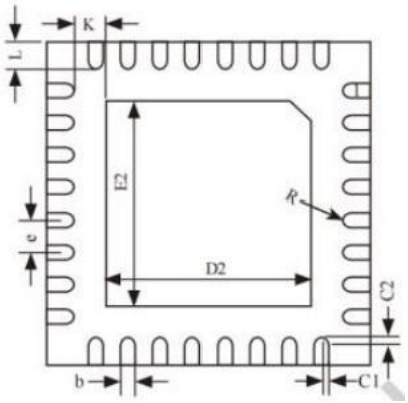
symbol	parameter	condition	least value	representative value	crest value	unit
Vooa	Analog power supply	Vvoo≤Voo ₄ =Vooo≤Vvoo	2.5	3.3	5.5	V
Vooo	Digital power supply	Vvoo≤VooA=Vooo≤Vnoo	2.5	3.3	5.5	V
V ₁ voo	TVDD source	Vpvop≤VooA =Vooo≤Vrvon	2.5	3.3	5.5	V
Vvoo	PVDD source	Vpvoo≤VooA=Vooo≤Vrvoo	2.5	3.3	5.5	V
Vsvoo	SVDD source		2.5		5.5	V
Tmb	ambient temperature		-40	_	+85	℃
lu	Discharge current	VooA=Voop=Vvoo=Vwoo =3.3V				
		Hard to drop electricity NRSTPD=0	-	-	5	uA
		Soft off the electricity The RF detector is turned on	_		10	uA

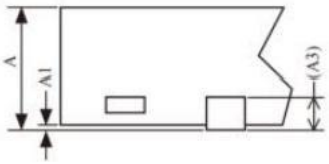
looo	Digital power current	Vooo=3.3V		1	2	mA
lPco	Low-power card search current	500ms auto-search interval		10uA	20uA	uA
looa	Analog power current	Voo ₄ =3.3V;RcvOff=C	_	2	3	mA
		The receiver turns off the Voo=3.3V RcvOff=1	-	1	2	mA
lrvoo	TVDD source current	Fin TVDD; continuous wave		60	100	mA

15 Package dimension diagram

QFN32 OUTLINE PACKAGE







stock size (Measurement unit =MILLMETER / mm)			
symbol	MIN	NOM.	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20REF	
b	0.18	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.10	3.20	3.30
E2	3.10	3.20	3.30
e	0.40	0.50	0.60
K	0.20		
L	0.35	0.40	0.45
R	0.09		
CI		0.08	–
C2		0.08	

NOTES :
ALL DIMENSIONS REFER TO JEDEC STANDARD MO-220 WHHD-4