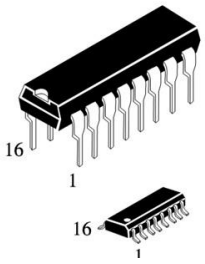
HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS



N SUFFIX
DIP

D SUFFIX
SOP

ORDERING INFORMATION

HT2003ANZ DIP
HT2003ARZ SOP

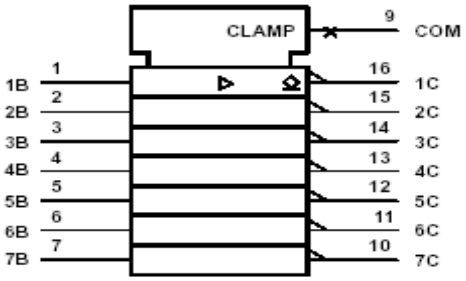
The HT2003A are monolithic high-voltage, high-current Darlington transistor arrays. Each consists of seven n-p-n Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs may be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers.

The HT2003A has a 2.7-kΩ series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices.

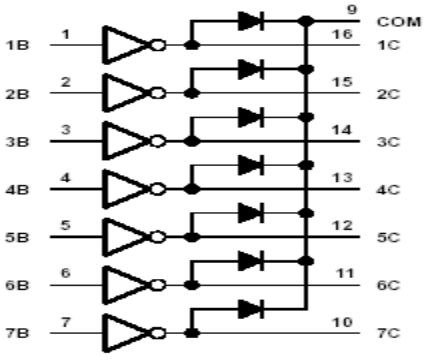
- 500-mA Rated Collector Current (Single Output)
- High-Voltage Outputs . . . 50 V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay Driver Applications
- Ordering Information

Operation Temperature	PKG Type	Ordering part number
-40°C ~ 85°C	DIP - 16	HT2003ANZ
	SOP - 16	HT2003ARZ

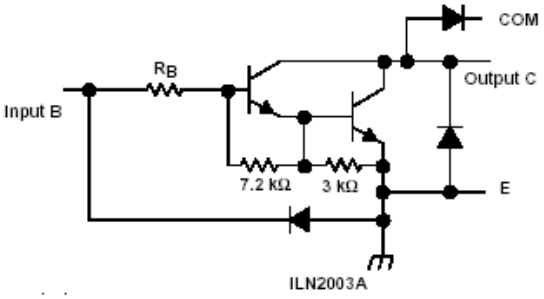
LOGIC SYMBOL



LOGIC DIAGRAM



SCHEMATICS (each Darlington Pair)



All resistor values shown are nominal.

HT2003A: R_B = 2.7 kΩ

Absolute Maximum Ratings (Ta =25°C)

Parameter		Symbol	Limit Values		Unit
			min.	max.	
Output Sustaining Voltage		$V_{CE(SUS)}$	–0.5	50	V
Output Current		I_{OUT}	500		mA/ch
Input Voltage		V_{IN}	– 0.5	30	V
Clamp Diode Reverse Voltage		V_R	50		V
Clamp Diode Forward Current		I_F	500		mA
Power Dissipation	DIP	P_D	1.15		W
	SOP		0.95		
Operating Temperature		T_{opr}	-40	85	°C
Storage Temperature		T_{stg}	-55	150	°C

* Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.
Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

(Ta=-40~85°C)

Parameter		Symbol	Test Condition	Limit Value			Unit
				Min	Typ	Max	
Output Sustaining Voltage		$V_{CE(SUS)}$		0	-	50	V
Output Current	DIP	I_{OUT}	T_{pw}=25ms,Duty=10%, 7 Circuits	0	-	370	mA/ch
			T_{pw}=25ms,Duty=30%, 7 Circuits	0	-	200	
	SOP		T_{pw}=25ms,Duty=10%, 7 Circuits	0	-	290	
			T_{pw}=25ms,Duty=30%, 7 Circuits	0	-	150	
Input Voltage		V_{IN}		0	-	30	V
Clamp Diode Reverse Voltage		V_R		-	-	50	V
Clamp Diode Forward Current		I_F		-	-	400	mA
Power Dissipation	DIP	P_D		-	-	0.52	W
	SOP			-	-	0.4	

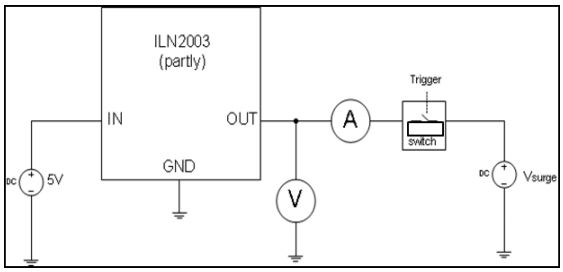
Electrical characteristics, T_A = 25℃ (unless otherwise noted)

Parameter		Test Fig.	Test Conditions		Min	Typ	Max	Unit
$V_{I(on)}$	On-state Input Voltage	6	V_{CE}=2V	I_C=125mA				V
				I_C=200mA			2.4	
				I_C=250mA			2.7	
				I_C=275mA				
				I_C=300mA			3	
				I_C=350mA				
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	I_I=250uA	I_C=100mA		0.9	1.1	V
			I_I=350uA	I_C=200mA		1	1.3	
			I_I=500uA	I_C=350mA		1.2	1.6	
I_{CEX}	Collector outoff current	1	V_{CE}=50V	I_I=0			50	uA
		2	V_{CE}=50V, T_A=85℃	I_I=0			100	
				V_I=1V				
h_{FE}	DC Current Transfer Ratio	5	V_{CE}=2V, I_{OUT}=350mA		1000	-	-	
V_F	Clamp forward voltage	8	I_F=350mA			1.7	2	V
$I_{I(off)}$	Off-state input current	3	V_{CE}=50V T_A=85℃	I_C=500uA	50	65		uA
I_I	Input current	4	V_I=2.4V			0.4	0.7	mA
			V_I=5V					
			V_I=12V					
I_R	Clamp reverse current	7	V_R=50V				50	uA
			V_R=50V	T_A=85℃			100	
C_I	Input capacitance		V_I=0	f=1MHz		15	25	pF

Switching Characteristics, T_A=25°C

Parameter	Test Conditions	Min	Typ	Max	Unit
t_{PLH} Propagation delay time, low-to-high-level output	See Figure 9		0.25	1	us
t_{PHL} Propagation delay time, high -to- low -level output			0.25	1	us
V_{OH} High-level output voltage after switching	V_S=50V, I_O=300mA, See Figure 10	V_S-20			mV

* EOS (Electrical Over Stress) Immunity Level
Test Circuit



Test conditions	
Vcc	12V
Power on time	5000ms
Current max	1.0A
IN	pin4
OUT	pin13

tE (Endurance time) : time until IC damage / Criterion : IC should survive EOS
EOS Immunity Level: More than 5000ms

PARAMETER MEASUREMENT INFORMATION

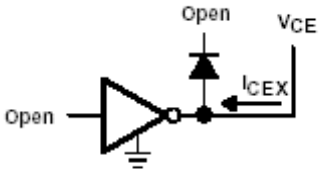


Figure 1. I_{CEX} Test Circuit

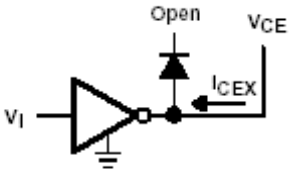


Figure 2. I_{CEX} Test Circuit

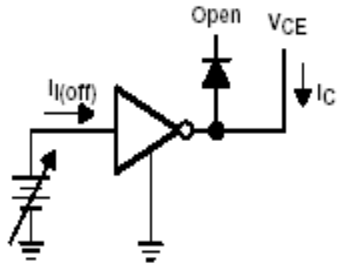


Figure 3. $I_{I(off)}$ Test Circuit

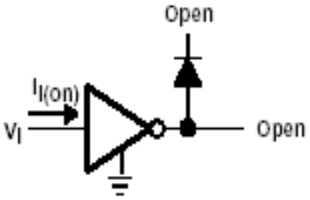
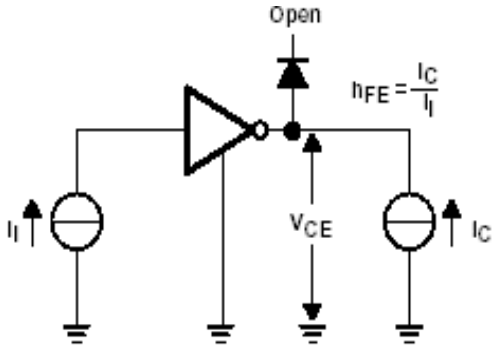


Figure 4. I_I Test Circuit



NOTE: I_I is fixed for measuring $V_{CE(sat)}$, variable for measuring h_{FE}.

Figure 5. h_{FE}, $V_{CE(sat)}$ Test Circuit

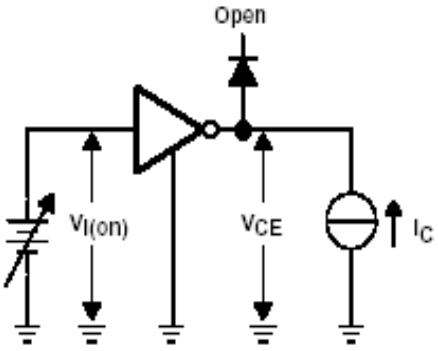


Figure 6. $V_{I(on)}$ Test Circuit

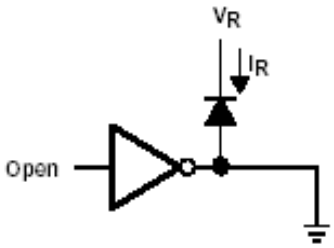


Figure 7. I_R Test Circuit

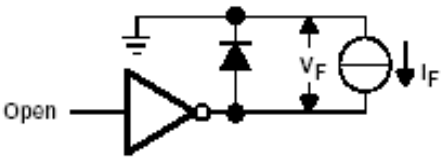


Figure 8. V_F Test Circuit

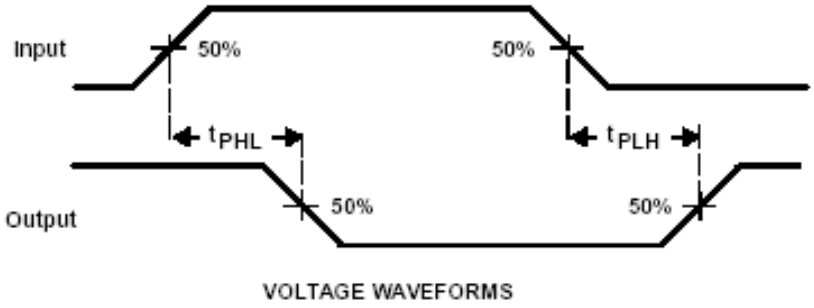
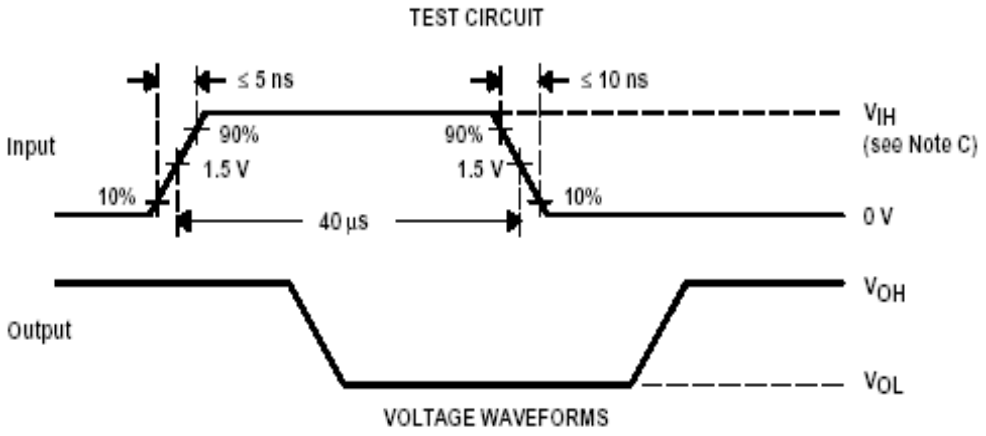


Figure 9. Propagation Delay-Time Waveforms



NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 .
B. C_L includes probe and jig capacitance.
C. V_{IH} = 3 V;

TYPICAL CHARACTERISTICS

COLLECTOR-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT (ONE DARLINGTON)

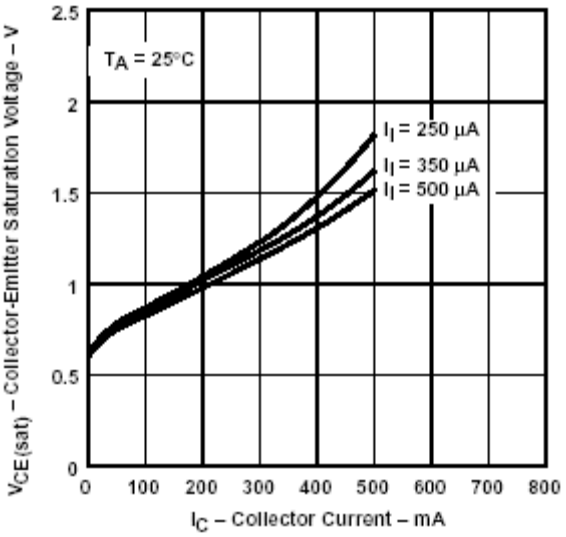


Figure 11

COLLECTOR-EMITTER SATURATION VOLTAGE vs TOTAL COLLECTOR CURRENT TWO DARLINGTONS PARALLELED)

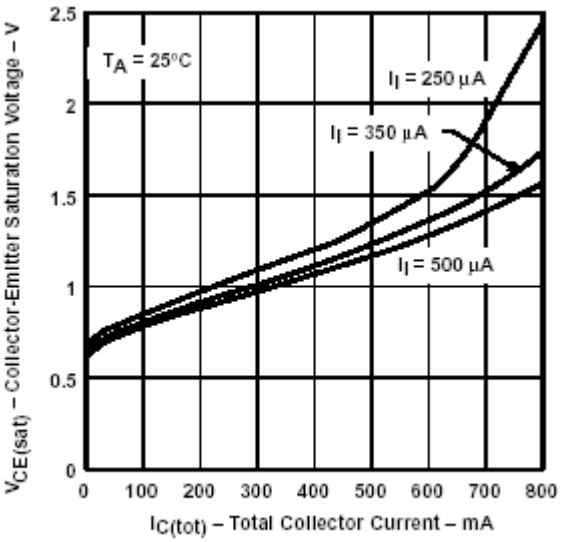


Figure 12

COLLECTOR CURRENT vs

INPUT CURRENT

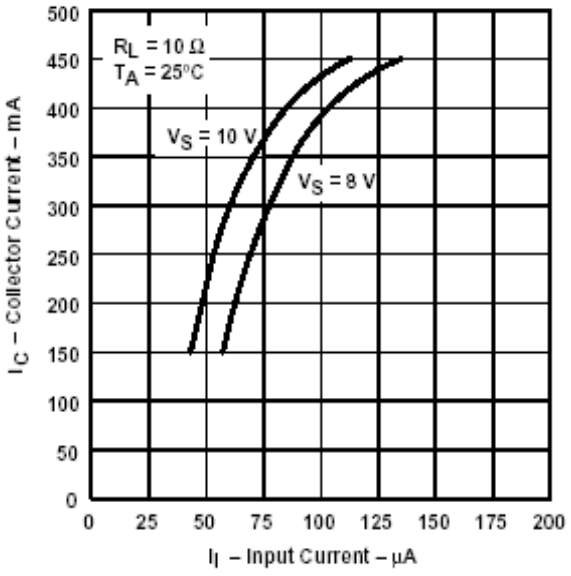


Figure 13

THERMAL INFORMATION

D PACKAGE
MAXIMUM COLLECTOR CURRENT
Vs
DUTY CYCLE

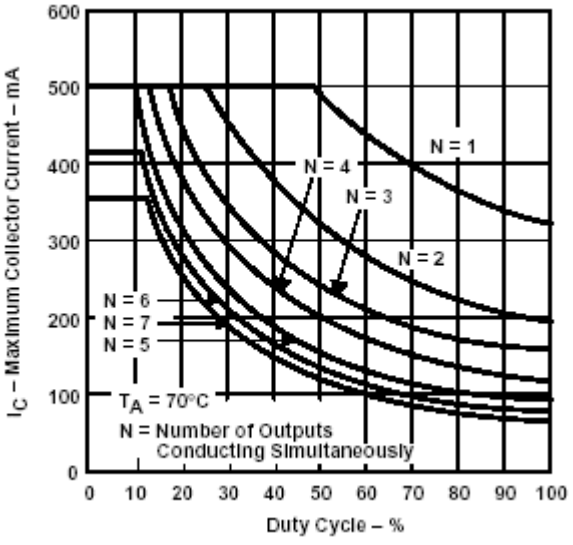


Figure 14

N PACKAGE
MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

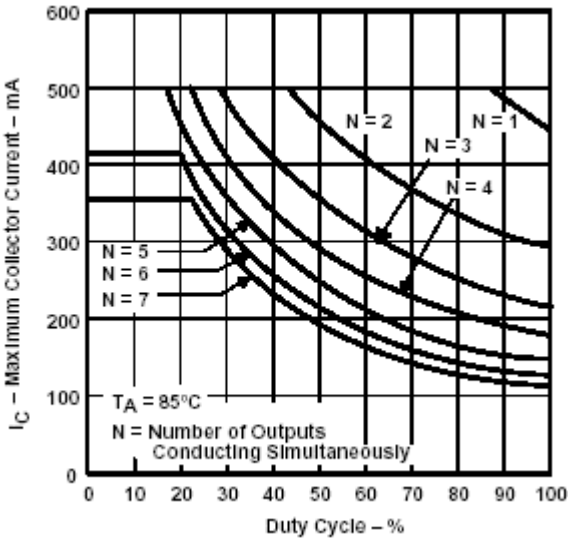
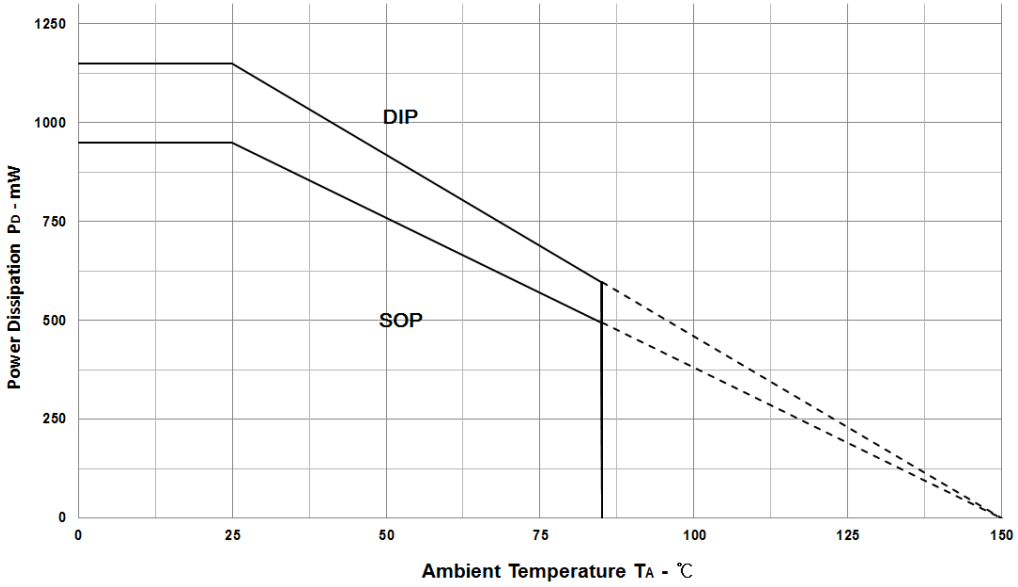


Figure 15

POWER DISSIPATION

VS.
AMBIENT TEMPERATURE



APPLICATION INFORMATION

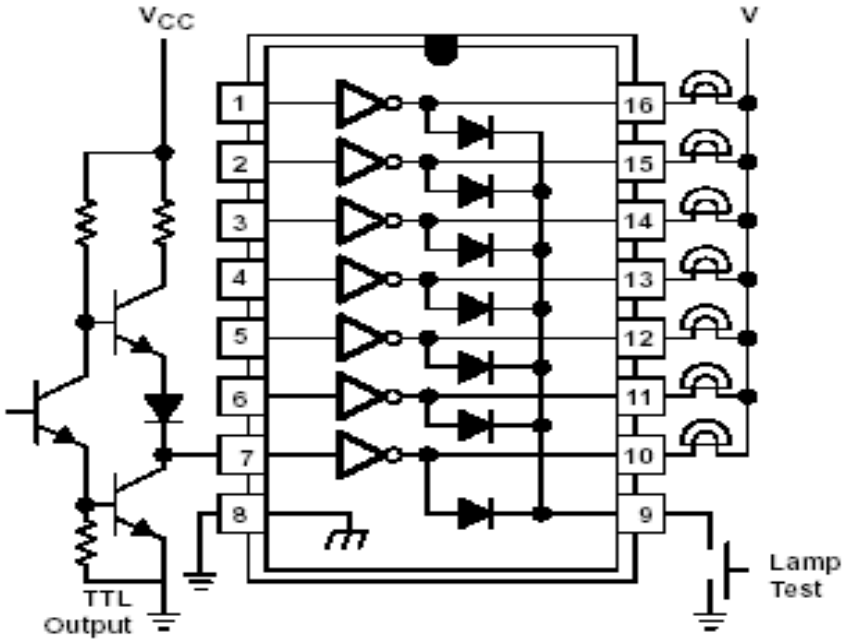


Figure 16. TTL to Load

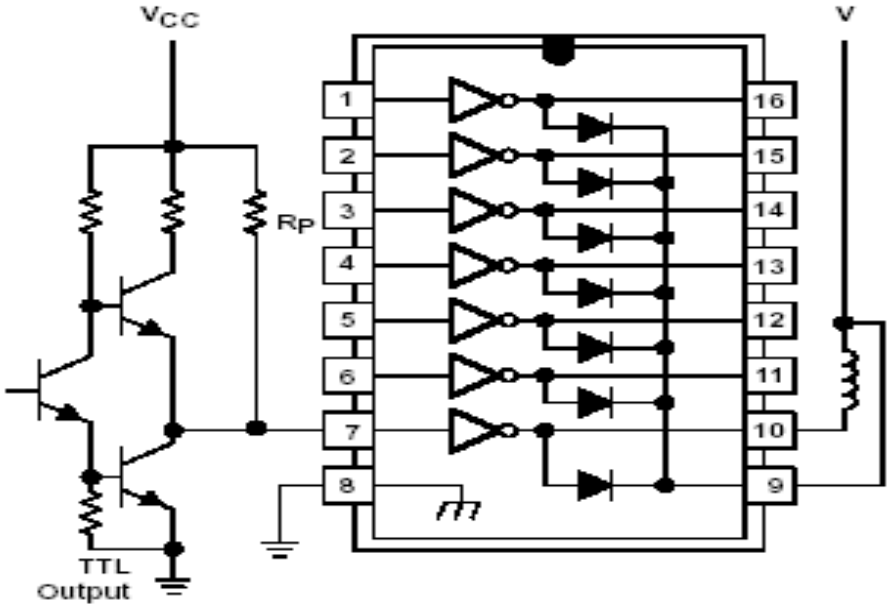
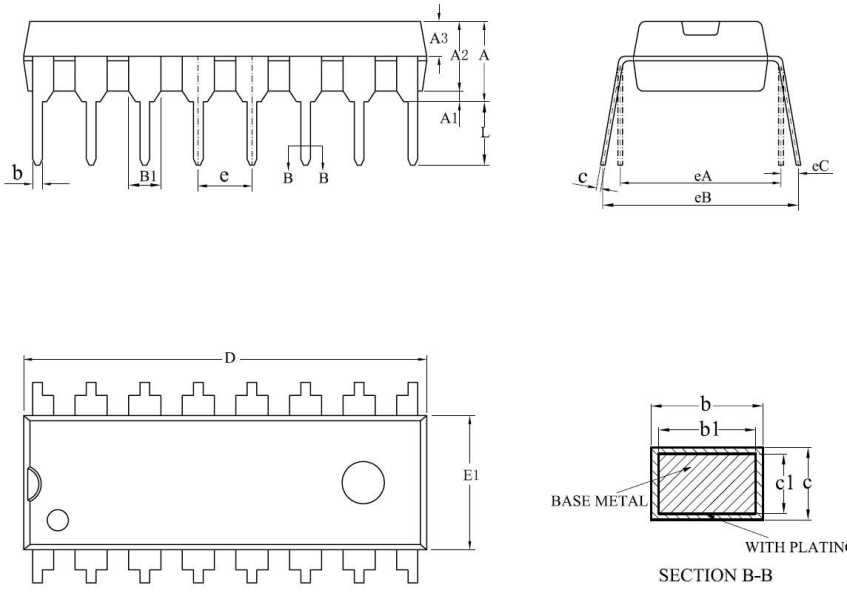


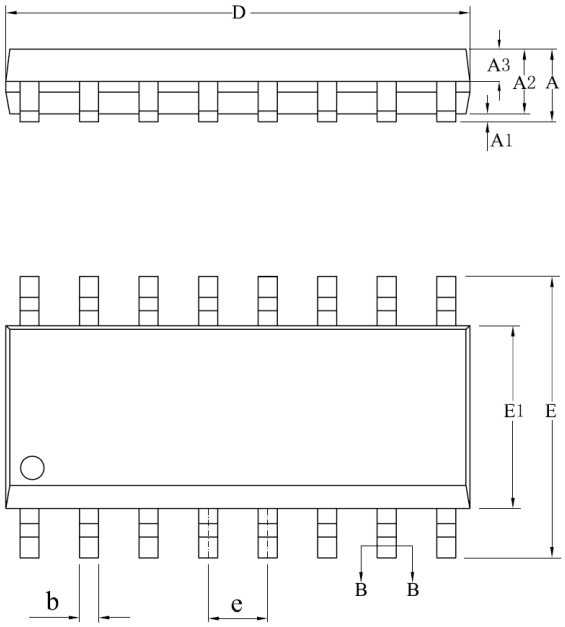
Figure 17. Use of Pullup Resistors to Increase Drive Current

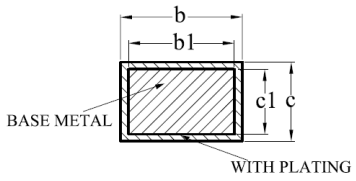
DIP-16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	3.60	3.80	4.00
A1	0.51	—	—
A2	3.10	3.30	3.50
A3	1.42	1.52	1.62
b	0.44	—	0.53
b1	0.43	0.46	0.48
B1	1.52BSC		
c	0.25	—	0.31
c1	0.24	0.25	0.26
D	18.90	19.10	19.30
E1	6.15	6.35	6.55
e	2.54BSC		
eA	7.62BSC		
eB	7.62	—	9.50
eC	0	—	0.94
L	3.00	—	—
L/F载体尺寸 (Mil)	80*80		
	110*140		
	140*170		

SOP-16





SECTION B-B

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.25
A2	1.35	1.40	1.45
A3	0.60	0.65	0.70
b	0.39	—	0.48
b1	0.38	0.41	0.43
c	0.21	—	0.26
c1	0.19	0.20	0.21
D	9.70	9.90	10.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
L	0.50	—	0.80
L1	1.05BSC		
θ	0	—	8°
L/F载体尺寸 (mil)	75*75		
	90*110		
	90*180		