

## 5 Port 10/100 Ethernet Integrated Switch (Policy-base QoS, Layer 2-4 MF Classifier, HW IGMP Snooping)

### Features

- Wide operating temperature range
  - IP175DLF (0°C to 70°C)
  - IP175DLFI (-40°C to 85°C)
- Built in 6 MAC and 5 PHY
- Each port can be configured to be 10Based-T, 100Base-TX
- Up to 2K MAC addresses
- Support auto-polarity for 10Mbps
- Broadcast storm protection
- Auto MDI-MDIX
- Support three MII/RMII ports
- Layer2-4 Multi-Field classifier
  - Support 8-MultiField entry
  - Support traffic policy
  - Support Multi-Filed filter
  - Support copy to mirror port
  - Support trap to CPU port
- Class of Service
  - Port based, MAC address, VID, VLAN priority, IPv4 ToS, IPv6 DSCP,TCP/UDP logical port and Multi-Field
- QoS
  - Support policy-based QoS
  - Support 4-level priority queues per port
  - WRR/WFQ/SP
- Support hardware IGMP v1,v2 snooping
- Support Port mirror
- Support 16 VLAN (IEEE Std 802.1q)
  - Port-based/tagged-based VLAN
  - Shared/Independent VLAN Learning
  - Support insert, remove tag
  - Support VLAN priority remarking
- Support STP, RSTP and MSTP
- Support port-based access control
- Supports rate control(WFQ)
  - In/Out port rate control
  - Traffic Policy
- Interrupt Pin
- Support special tag and QinQ header
- Support Link quality LED for 100Mbps
- Support direct, serial and dual color LED
- Built in Linear regulator control register
- **Support auto power saving mode**
- 0.16um, 128-pin PQFP Lead Free package

### General Description

IP175DLF integrates a 6-port switch controller, SSRAM, and 5 10/100 Ethernet transceivers. Each of the transceivers complies with the IEEE802.3, IEEE802.3u, and IEEE802.3x specifications. The DSP approach is utilized for designing transceivers with 0.16um technology; they have high noise immunity and robust performance.

IP175DLF operates in store and forward mode. IP175DLF have a lot of rich feature for different application, include router application, firewall, IEEE 802.1Q, IGMP snooping, policy-based QoS. It provides powerful QoS function, include traffic policy, traffic meter, and flexible queue scheduling (WRR/WFQ/SP). In virtual LAN, IP175DLF support port-based VLAN and IEEE 802.1Q tag-tagged VLAN (up to 16 VLAN groups).

IP175DLF support up to 2K MAC addresses, up to 16 VLANs and up to 8 Multi-Field entries. These tables are accessible through MII register. The address table can configure either "2K unicast addresses" or "1K unicast addresses and 1K multicast addresses". The Multi-Field classification is powerful classifier (layer2 to layer 4 packet headers) in packet classification. The classifier divides incoming packets into multiple classes based on prescribed rules. Each traffic class from classifier can drop out-of-profile packets, monitor traffic, specify forwarding behavior, and specify output queue.

Beside a 5-port switch application, IP175DLF supports three MII/RMII ports for router application, one WAN port and one HOME/PNA or Access point. The external MAC can monitor or configure IP175DLF by accessing MII registers through SMIO.

MII/RMII port also can be configured to be MAC mode. It is used to interface an external PHY to work as 5+1 switch. Through SMI1 IP175DLF can monitor and configure external PHY.

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## Revision History

| Revision #        | Change Description   |
|-------------------|--|
| IP175DLF-DS-R01   | Initial release  |
| IP175DLF-DS-R02   | Rearrange IP175DLF-DS-R01  |
| IP175DLF-DS-R03   | <ol style="list-style-type: none"> <li>1. Add GND PIN on page 35</li> <li>2. Add X1 Input Voltage on page 130</li> <li>3. Add Vrst Threshold Voltage to DC table on page 130</li> <li>4. Add Turbo MII AC timing on page 132 &amp; 133</li> <li>5. Modify PHY21 Reg0 on page 90</li> <li>6. Modify Absolute Maximum Rating on page 130</li> <li>7. Modify power on sequence on page 131</li> <li>8. Modify Dual color mode LED Link off status value on page 35</li> </ol> |
| IP175DLF-DS-R04   | <ol style="list-style-type: none"> <li>1. Add note on page 16 for pin 54</li> <li>2. Modify Operating Conditions table on page 130</li> </ol>  |
| IP175DLF-DS-R05   | <ol style="list-style-type: none"> <li>1. Modify X_EN description on page 13</li> <li>2. Modify MAC_X_EN description on page 16</li> </ol>   |
| IP175DLF-DS-R06   | <ol style="list-style-type: none"> <li>1. Modify double tag to QinQ on page 1</li> <li>2. Add enable disable setting value to IGMP base control register on page 95</li> <li>3. Modify VCC (AVCC) value on page 12 &amp; 35</li> <li>4. Add QinQ register note for KEEP_TAG register on page 107</li> </ol>  |
| IP175DLF-DS-R07   | <ol style="list-style-type: none"> <li>1. Add IC Junction Temperature for Absolute Maximum Rating on page 130</li> <li>2. Add Crystal Operating Temperature Range for IP175DLFI on page 129</li> <li>3. Modify VCC from 1.8V to 1.9V</li> </ol>  |
| IP175DLF-DS-R08   | <ol style="list-style-type: none"> <li>1. Modify Auto-Negotiation description on page 59</li> <li>2. Modify Auto MDI-MDIX description on page 67</li> </ol>  |
| IP175DLF-DS-R08.1 | 1. Modify VCC minimum from 1.85V to 1.7V   |
| IP175DLF-DS-R08.2 | 1. MDIO0 timing of output delay(5 == > 10ns) and hold timing (10ns == > 5ns)   |
| IP175DLF-DS-R08.3 | 1. Modify MDIO1 timing on page 137   |
| IP175DLF-DS-R08.4 | 1. Add PHY ID Map on page 58   |

## Disclaimer

This document probably contains the inaccurate data or typographic error. In order to keep this document correct, IC Plus reserves the right to change or improve the content of this document.

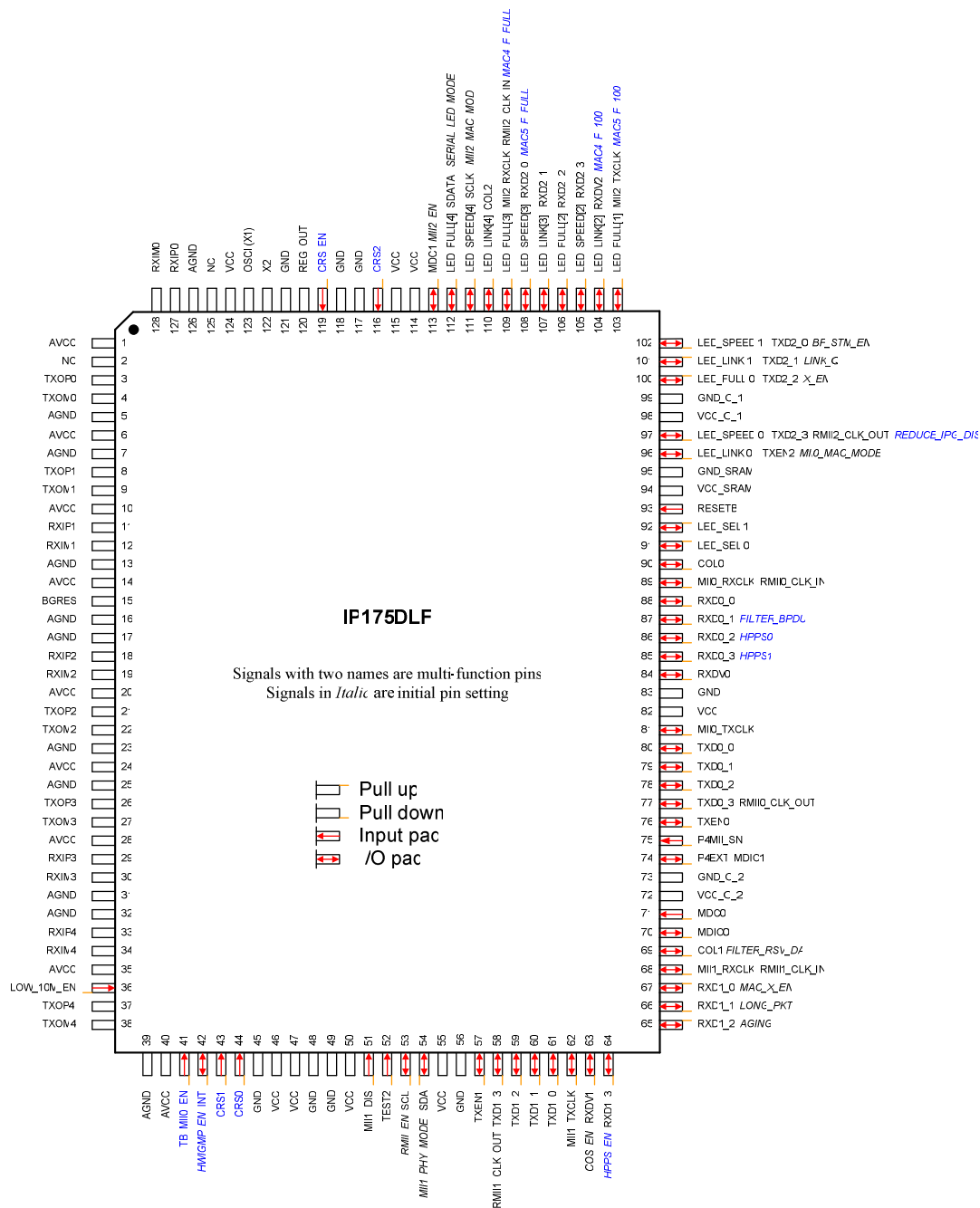
**Feature comparison between IP175C and IP175DLF**

|                         |                         |                           |                                  |
|-------------------------|-------------------------|---------------------------|----------------------------------|
| Product Name            |                         | IP175C                    | IP175DLF                         |
| Process                 |                         | 0.18um                    | 0.16um                           |
| Package Type            |                         | 128pin PQFP               | 128pin PQFP                      |
| Major Block             |                         | MAC/6ports+PHY/5ports     | MAC/6ports+PHY/5ports            |
| AUTO-MDI-MDIX           |                         | Yes                       | Yes                              |
| 100M Fiber (100BaseFX)  |                         | No (Yes for IP175CH only) | No                               |
| MAC Address             | Table Size              | 2K                        | 2K                               |
|                         | Hashing Algorithm       | 2-way Hashing Scheme      | 4-way Hashing Scheme             |
|                         | Address Type            | Individual MAC Address    | Individual/Multicast MAC Address |
|                         | Accessible              | No                        | Yes                              |
| IEEE802.1Q              | SVL/IVL                 | No                        | Yes                              |
|                         | Port-based VLAN         | 6 VLAN Group              | 6 VLAN Group                     |
|                         | IEEE 802.1Q VLAN Group  | 16 VLAN Group             | 16 VLAN Group                    |
|                         | Insert/Remove Tag       | Yes                       | Yes                              |
|                         | Ingress Filter          | No                        | Yes                              |
|                         | STP                     | Yes (CPU Assistance)      | Yes (CPU Assistance)             |
|                         | RSTP (802.1w)           | No                        | Yes (CPU Assistance)             |
|                         | MSTP (802.1s)           | No                        | 4 MSTP (CPU Assistance)          |
| Priority Classification | Port Based              | Yes                       | Yes                              |
|                         | VLAN Priority           | Yes                       | Yes                              |
|                         | ToS                     | Yes                       | Yes                              |
|                         | DSCP                    | Yes                       | Yes                              |
|                         | MAC Address             | No                        | Yes                              |
|                         | VID                     | No                        | Yes                              |
|                         | TCP/UDP port number     | No                        | Yes                              |
|                         | Special Tag             | No                        | Yes                              |
| QoS                     | Multi-Field             | No                        | Yes                              |
|                         | Queue Level             | 2-level Queue             | 4-level Queue                    |
|                         | Policy-based QoS        | No (Best Effort)          | Yes                              |
|                         | VLAN Priority Remarking | No                        | Yes                              |
| Firewall                | Scheduling              | WRR                       | WRR/WFQ/SP/BE                    |
|                         | Multi-Field Filter      | No                        | Yes                              |
|                         | SMAC/DMAC Filter        | No                        | Yes                              |
|                         | Unknown SMAC Filter     | No                        | Yes                              |



|                        |                                  |                      |   |
|------------------------|----------------------------------|----------------------|---|
|                        | TCP/UDP port Filter              | No                   | Yes   |
| Multi-Field Classifier | Classification                   | No                   | Yes (L2-L4 Multi-field Flow Classification) |
|                        | Filter                           | No                   | Yes   |
|                        | Policy                           | No                   | Yes   |
|                        | Priority Assignment              | No                   | Yes   |
|                        | Traffic Mirror                   | No                   | Yes   |
| IGMP Snooping          | IGMP Version                     | V1, V2               | V1, V2                                      |
|                        | Software                         | Yes (CPU Assistance) | Yes (CPU Assistance)                        |
|                        | Hardware                         | No                   | Yes   |
|                        | IGMP Membership Table            | No                   | Up to 1K                                    |
| Rate Control           | Ingress/Egress port Rate Control | Yes                  | Yes   |
|                        | Traffic Rate Control (Policy)    | No                   | Yes   |
|                        | WFQ                              | No                   | Yes   |
|                        | Range                            | 8-level              | 0-100Mbps                                   |
| IEEE 802.1x            | No                               | Yes (CPU Assistance) |   |
| Port Mirroring         | No                               | Yes                  |   |
| Aging Time             | Yes (300sec)                     | Yes (Programmable)   |   |
| Broadcast Storm        | Yes                              | Yes                  |   |
| Smart MAC              | Yes                              | Yes                  |   |
| External MII           | 3MII                             | 3MII                 |   |
| Interrupt              | No                               | Yes                  |   |
| Power Saving           | Yes                              | Yes                  |   |
| Loop Back Test         | Each port                        | Each port            |   |
| Link Quantity LED      | Yes                              | Yes                  |   |
| Power down             | Yes                              | Yes                  |   |
| Dual color mode LED    | Yes                              | Yes                  |   |

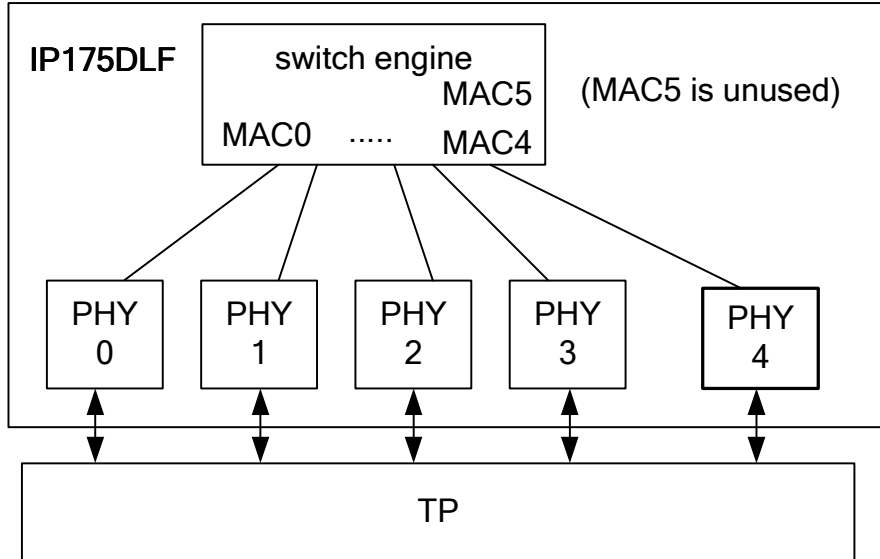
## 1 Pin Diagram





**5-port switch application**

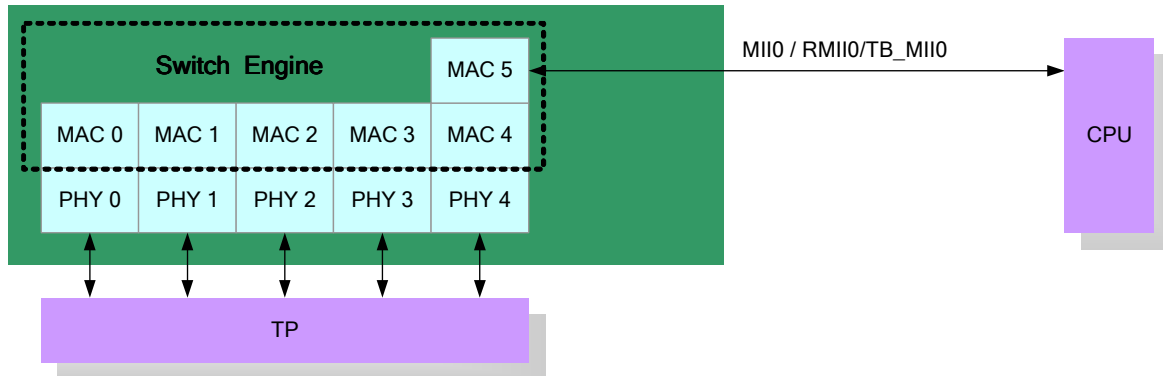
When pin 74 P4EXT is pulled low, all MII/RMII ports are disabled, and IP175DLF works as a 5-port switch. MAC5 is not used in this application.



**Router application using one MII/RMII port**

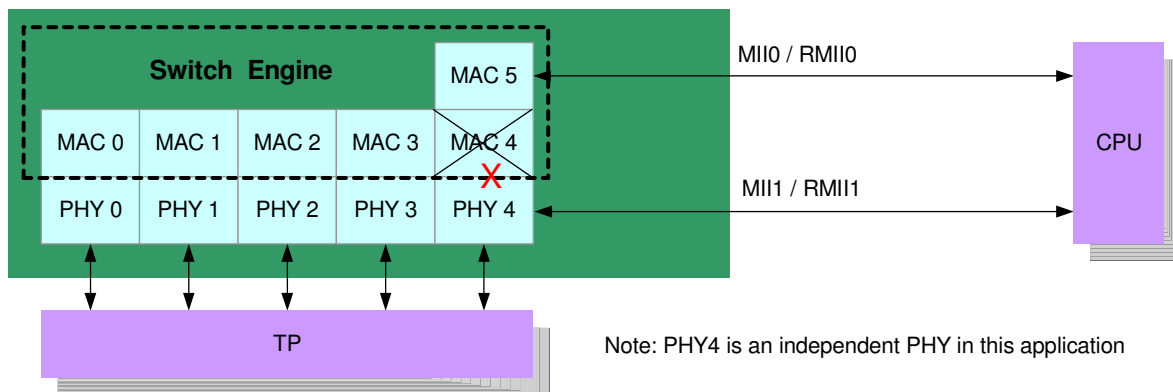
(can be configured to 4LAN+1WAN, 3LAN+2WAN, 2LAN+3WAN or 1LAN+4WAN)

| p4ext | mii1_dis | mii2_en | p4mii_sni | rmii_en | mii0_mac_mod | mii2_mac_mod | tb_mii0_en |
|-------|----------|---------|-----------|---------|--------------|--------------|------------|
| 1     | 1        | 0       | 0         | x       | 0            | x            | x          |



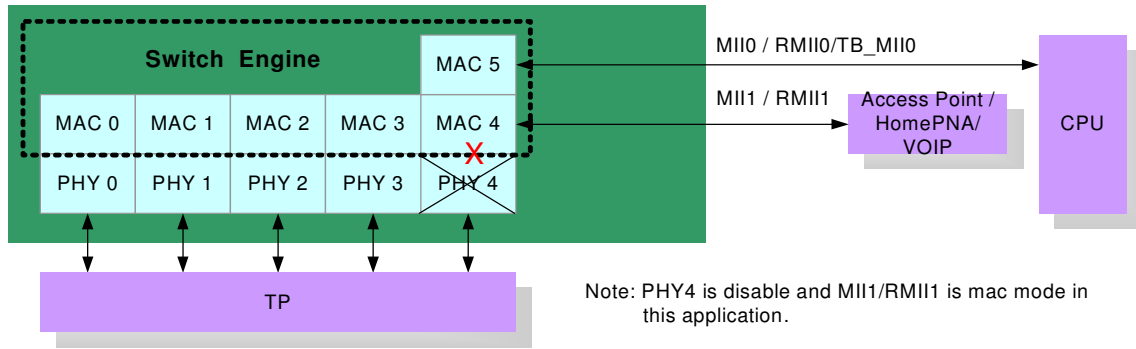
**Router application using two-MII/RMII ports**

| p4ext | mii1_dis | mii2_en | p4mii_sni | rmii_en | mii0_mac_mod | mii2_mac_mod | tb_mii0_en |
|-------|----------|---------|-----------|---------|--------------|--------------|------------|
| 1     | 0        | 0       | 0         | x       | 0            | x            | 0          |



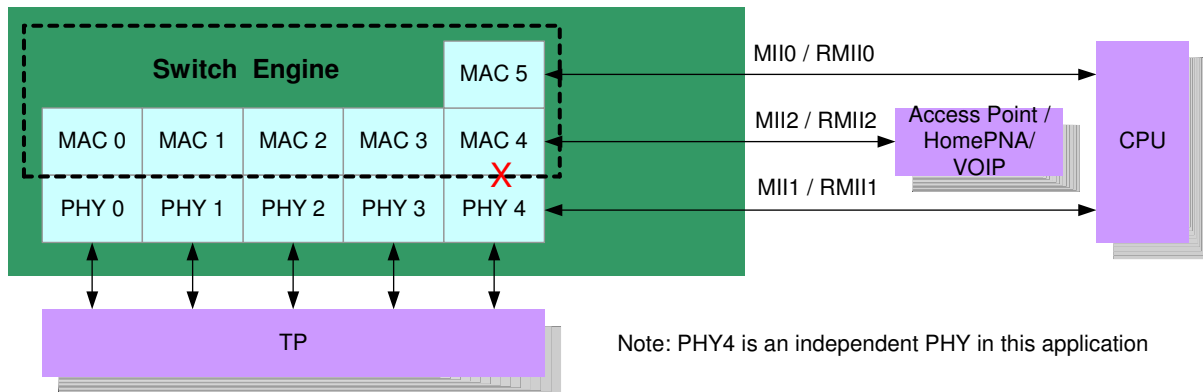
**Router application using two-MII/RMII ports (another option)**

| p4ext | mii1_dis | mii2_en | p4mii_sni | rmii_en | mii0_mac_mod | mii1_phy_mod | tb_mii0_en |
|-------|----------|---------|-----------|---------|--------------|--------------|------------|
| 1     | 0        | 0       | 0         | x       | 0            | 0            | x          |



**Router application using three-MII/RMII ports**

| p4ext | mii1_dis | mii2_en | p4mii_sni | rmii_en | mii0_mac_mod | mii2_mac_mod | tb_mii0_en |
|-------|----------|---------|-----------|---------|--------------|--------------|------------|
| 1     | 0        | 1       | 0         | x       | 0            | 0            | 0          |



## 2 Pin Description

| Type | Description                                |
|------|--|
| I    | Input pin                                  |
| O    | Output pin                                 |
| IPL  | Input pin with internal pull low 140k ohm  |
| IPH  | Input pin with internal pull high 222k ohm |

| Type | Description                                 |
|------|---|
| IPL1 | Input pin with internal pull low 31.6k ohm  |
| IPH1 | Input pin with internal pull high 31.6k ohm |
| IPL2 | Input pin with internal pull low 140k ohm   |
| IPH2 | Input pin with internal pull high 222k ohm  |

| Pin No.       | Label   | Type | Description  |
|---------------|---------|------|--|
| <b>Analog</b> |         |      |  |
| 120           | REG_OUT | O    | Regulator output.<br><br>The internal linear regulator uses this pin to control external transistor to generates a voltage source between 1.85v ~ 2.00v.<br><br>IP175DLF uses the DVCC/AVCC as feedback voltage. |

Pin description (continued)

| Pin No.  | Label           | Type | Description  |
|--|-----------------|------|--|
| <b>LED pins used as initial setting (the setting is latched at the end of reset)</b> |                 |      |  |
| 112  | SERIAL_LED_MODE | IPL1 | Serial led mode<br>1: supports link LED only<br>0: supports link, speed, and duplex LED (default)<br><br>When MII/RMII2 is enabled, there are not enough pins for LED and IP175DLF sends out LED information through pin 111 SCLK and pin 112 SDATA.   |
| 102  | BF_STM_EN       | IPL1 | Broadcast storm protection enable<br>1: enable<br>0: disable (default)<br><br>A port begins to drop incoming packets if it receives broadcast packets more than the threshold defined in MII register 20.17~20.19  |
| 101  | LINK_Q          | IPH1 | Link quality<br>1: enable (default)<br>0: disable<br><br>When the function is enabled, besides link on/off status, activity status, link LED shows link quality. The link LED will be flash (on: 2sec / off: 2sec) when the SNR of received signal is lower than the desired value for normal operation. |
| 100  | X_EN            | IPH1 | IEEE802.3X/ back pressure enable for PHY 0~4<br>1: enable (default)<br>0: disable  |
| 097  | REDUCE_IPG_DIS  | IPL1 | Reduce IPG function<br>1:disable reduce IPG function<br>0:enable reduce IPG function(default)<br><br>This function reduce the IPG by random from 0~20 PPM  |

Pin description (continued)

| Pin No.  | Label   | Type | Description  |             |   |        |        |        |          |        |          |        |        |
|--|---|------|--|-------------|---|--------|--------|--------|----------|--------|----------|--------|--------|
| <b>MII pins used as initial setting (the setting is latched at the end of reset)</b> |   |      |  |             |   |        |        |        |          |        |          |        |        |
| 87   | FILTER_BPDU   | IPL2 | Filter packets with reserved DA (0180c2000000)<br>1: Filter the packets<br>0: Forward the packets (default)<br><br>It is valid only if p4ext is pulled low.  |             |   |        |        |        |          |        |          |        |        |
| 69   | FILTER_RSV_DA                                       | IPL2 | Filter packets with reserved DA (0180c20002~f)<br>1: Filter the packets<br>0: Forward the packets (default)<br><br>It is valid only if p4ext is pulled low.  |             |   |        |        |        |          |        |          |        |        |
| 66   | LONG_PKT  | IPL2 | Max forwarded packet length<br>1: 1792 bytes<br>0: 1536 bytes (default)<br><br>It is valid only if p4ext is pulled low.  |             |   |        |        |        |          |        |          |        |        |
| 65   | AGING   | IPH2 | Address aging enable<br>1: enable, aging time is around 300s (default),<br>0: disable<br><br>It is valid only if p4ext is pulled low.  |             |   |        |        |        |          |        |          |        |        |
| 64   | HPPS_EN   | IPL2 | Port base priority setting enable<br>1:enable<br>0:disable (default)<br><br>It is valid only if p4ext is pulled low.   |             |   |        |        |        |          |        |          |        |        |
| 85,86  | HPPS1,HPPS0   | IPL2 | Port base priority setting bit[1:0]<br><br><table border="0" style="margin-left: 20px;"> <tr> <td>HPPS1,HPPS0</td> <td>Highest priority port<br/>(assign packet to queue 3)</td> </tr> <tr> <td>2'b00:</td> <td>port 4</td> </tr> <tr> <td>2'b01:</td> <td>port 0,1</td> </tr> <tr> <td>2'b10:</td> <td>port 3,4</td> </tr> <tr> <td>2'b11:</td> <td>port 0</td> </tr> </table><br>It is valid only if p4ext is pulled low and HPPS_EN is pulled high. | HPPS1,HPPS0 | Highest priority port<br>(assign packet to queue 3) | 2'b00: | port 4 | 2'b01: | port 0,1 | 2'b10: | port 3,4 | 2'b11: | port 0 |
| HPPS1,HPPS0  | Highest priority port<br>(assign packet to queue 3) |      |  |             |   |        |        |        |          |        |          |        |        |
| 2'b00:   | port 4  |      |  |             |   |        |        |        |          |        |          |        |        |
| 2'b01:   | port 0,1  |      |  |             |   |        |        |        |          |        |          |        |        |
| 2'b10:   | port 3,4  |      |  |             |   |        |        |        |          |        |          |        |        |
| 2'b11:   | port 0  |      |  |             |   |        |        |        |          |        |          |        |        |
| 63   | COS_EN  | IPL2 | Class of service enable<br>1: enable<br>0: disabled (default)<br><br>Priority classification is based on packet header.<br><br>It is valid only if p4ext is pulled low.  |             |   |        |        |        |          |        |          |        |        |

**Pin description (continued)**

| Pin No.                | Label      | Type | Description   |
|------------------------|------------|------|---|
| <b>Initial setting</b> |            |      |   |
| 36                     | LOW_10M_EN | IPL  | 10M low power mode enable<br>1: 10M low power mode, the transmit amplitude is depressed in 10M mode for power saving.<br>0: 10M normal mode (default)   |
| 41                     | TB_MII0_EN | IPL  | Turbo MII0 mode enable (pin setting only)<br>When Turbo MII0 mode enable, MII0CLK speed can be changed by programming MII register 21.22[2]. (50MHz or 31.25MHz)<br>1:enable<br>0:disable (default) |
| 42                     | HWIGMP_EN  | IPL2 | Hardware IGMP enable<br>1:enable<br>0:disable (default)   |
| 119                    | CRS_EN     | IPL  | CRS pin enable for external MII mode<br>1:enable<br>0:disable (default)   |

Pin description (continued)

| Pin No.   | Label        | Type | Description   |
|---|--------------|------|---|
| <b>External MII port setting (the setting is latched at the end of reset)</b> |              |      |   |
| 74  | P4EXT        | IPL2 | <p>External MII port enable<br/>1: MII interface configuration is enabled.<br/>0: External MII interface is disabled and IP175DLF works as a 5-port switch (default).</p> <p>The configuration function of pin FILTER_BPDU, FILTER_RSVD, MAC_X_EN, LONG_PKT, AGING, HPPS_EN, HPPSx and COS_EN are disabled when this pin is pulled high.</p>  |
| 53  | RMII_EN      | IPL2 | <p>RMII enable for all MII ports.<br/>1: All MII/RMII interfaces work in RMII mode<br/>0: All MII/RMII interfaces work in MII mode (default).</p> <p>It is valid only if P4EXT is pulled high.<br/>This pin defines the initial setting of all MII ports. Each port can be configured as MII or RMII by programming MII register 21.3[10:8].</p>  |
| 67  | MAC_X_EN     | IPH2 | <p>Flow control enable for external MII ports (MII0~2)<br/>1: enable (default),<br/>0: disable</p> <p>It is valid only if P4EXT is pulled low.</p>  |
| 96  | MII0_MAC_MOD | IPL1 | <p>External MII0 port MAC mode<br/>MII0 is connected to MAC5 of IP175DLF.<br/>1: MII0 works as a MAC and should be connected to an external PHY.<br/>0: MII0 works as a PHY and should be connected to an external MAC device (default).</p> <p>It is valid only if P4EXT is pulled high.</p>   |
| 54  | MII1_PHY_MOD | IPH2 | <p>External MII1 source port selection<br/>1: MII1 is connected to PHY4 of IP175DLF. It should be connected to an external MAC device.<br/>0: MII1 is connected to MAC4 of IP175DLF. It should be connected to an external PHY.</p> <p>It is valid only if P4EXT is pulled high and MII1_DIS is pulled low.</p> <p>Note:<br/>This pin can not be pulled low, when EEPROM interface is used.</p> |
| 111   | MII2_MAC_MOD | IPL1 | <p>External MII2 port MAC mode<br/>MII2 is connected to MAC4 of IP175DLF.<br/>1: MII2 works as a MAC and should be connected to an external PHY.<br/>0: MII2 works as a PHY and should be connected to an external MAC device (default).</p> <p>It is valid only if P4EXT is pulled high and MII2_EN is pulled high.</p>  |



|     |         |      |  |
|-----|---------|------|--|
| 113 | MII2_EN | IPL2 | <p>MII2 enable</p> <p>1: MII2 is enabled. It is note that LED is changed to serial mode automatically. User should not enable MII2 if pin 54 MII1_PHY_MOD is pulled low.</p> <p>0: MII2 is disabled (default).</p> <p>It is valid only if P4EXT is pulled high.<br/>The configuration function of pin MACx_F_FULL, MACx_F_100, BF_STM_EN, LINK_Q, X_EN, and MII0_MAC_MODE are disabled when this pin is pulled high.</p> <p>It becomes an output pin MDC1 after reset.</p> |
|-----|---------|------|--|

**Pin description (continued)**

| Pin No.                          | Label     | Type     | Description   |         |           |         |              |              |            |
|----------------------------------|-----------|----------|---|---------|-----------|---------|--------------|--------------|------------|
| <b>External MII port setting</b> |           |          |   |         |           |         |              |              |            |
| 75                               | P4MII_SNI | IPL      | SNI enable for MII0<br>1: SNI interface<br>0: MII interface (default).<br><br>It is valid only is P4EXT is pulled high and RMII_EN is pulled low.<br>It is valid for MII0 only.   |         |           |         |              |              |            |
| 51                               | MII1_DIS  | IPL      | Disable MII1<br>1: MII1 is disabled. It is for router application with one-MAC CPU.<br>0: MII1 is enabled. PHY4 is an independent PHY and can be access through MII1. It is for router application with two-MAC CPU (default).<br><br>It is valid only if P4EXT is pulled high. |         |           |         |              |              |            |
| <b>Configuration summary</b>     |           |          |   |         |           |         |              |              |            |
| mode                             | p4ext     | mii1_dis | mii1_phy_mod  | mii2_en | p4mii_sni | rmii_en | mii0_mac_mod | mii2_mac_mod | tb_mii0_en |
| <b>MII/RMII0</b>                 |           |          |   |         |           |         |              |              |            |
| TBMII/PHY mode                   | 1         | X        | X   | X       | 0         | 0       | 0            | X            | 1          |
| TBMII/MAC mode                   | 1         | X        | X   | X       | 0         | 0       | 1            | X            | 1          |
| MII/ PHY mode                    | 1         | X        | X   | X       | 0         | 0       | 0            | X            | 0          |
| MII/ MAC mode                    | 1         | X        | X   | X       | 0         | 0       | 1            | X            | 0          |
| RMII                             | 1         | X        | X   | X       | 0         | 1       | X            | X            | 0          |
| SNI/ PHY mode                    | 1         | X        | X   | X       | 1         | 0       | 0            | X            | 0          |
| SNI/ MAC mode                    | 1         | X        | X   | X       | 1         | 0       | 1            | X            | 0          |
| <b>MII/RMII1</b>                 |           |          |   |         |           |         |              |              |            |
| MII/ PHY mode                    | 1         | 0        | 1   | X       | X         | 0       | X            | X            | 0          |
| MII/ MAC mode                    | 1         | 0        | 0   | 0       | X         | 0       | X            | X            | 0          |
| RMII/PHY mode                    | 1         | 0        | 1   | X       | X         | 1       | X            | X            | 0          |
| RMII/MAC mode                    | 1         | 0        | 0   | 0       | X         | 1       | X            | X            | 0          |
| <b>MII/RMII2</b>                 |           |          |   |         |           |         |              |              |            |
| MII/ PHY mode                    | 1         | 0        | 1   | 1       | X         | 0       | X            | 0            | 0          |
| MII/ MAC mode                    | 1         | 0        | 1   | 1       | X         | 0       | X            | 1            | 0          |
| RMII                             | 1         | 0        | 1   | 1       | X         | 1       | X            | X            | 0          |

Note:

1. RMII\_EN takes precedence of P4MII\_SNI.
2. In MAC mode application, MII\_CLK must be provided before end of chip reset, otherwise must follow up a software-reset after MII\_CLK be provided.
3. In RMII mode application, RMII\_CLK must be provided before end of chip reset, otherwise must follow up a software-reset after RMII\_CLK be provided.

Pin description (continued)

| Pin No.  | Label                             | Type | Description  |
|--|-----------------------------------|------|--|
| <b>External MII0 interface (PHY mode, MII0_MAC_MOD=0, P4MII_SNI=0)</b> |                                   |      |  |
| 89   | MII0_RXCLK                        | O    | MII receive clock<br><br>MII0_RXCLK and MII0_TXCLK are the same clock source and in phase.                     |
| 81   | MII0_TXCLK                        | O    | MII transmit clock   |
| 80, 79,<br>78, 77  | TXD0_0, TXD0_1,<br>TXD0_2, TXD0_3 | I    | MII transmit data<br><br>It is sampled at the rising edge of MII0_TXCLK.                                       |
| 76   | TXEN0                             | I    | MII transmit enable<br><br>It is used to frame TXD0[3:0]. It is sampled at the rising edge of MII0_TXCLK.      |
| 90   | COL0                              | O    | MII collision<br><br>It is active when MII0 is half duplex and a collision event happens.                      |
| 84   | RXDV0                             | O    | MII receive data valid<br><br>It is used to frame RXD0[3:0]. It is sent out at the falling edge of MII0_RXCLK. |
| 88, 87,<br>86, 85  | RXD0_0, RXD0_1,<br>RXD0_2, RXD0_3 | O    | MII receive data<br><br>It is sent out at the falling edge of MII0_RXCLK.                                      |

**Pin description (continued)**

| Pin No.  | Label                             | Type | Description  |
|--|-----------------------------------|------|--|
| <b>External MII0 interface (MAC mode, MII0_MAC_MOD=1, P4MII_SNI=0)</b> |                                   |      |  |
| 81   | MII0_TXCLK                        | I    | MII transmit clock<br>It is an input clock and it is connected to MII_TXCLK of external PHY.   |
| 80, 79,<br>78, 77  | TXD0_0, TXD0_1,<br>TXD0_2, TXD0_3 | O    | MII transmit data<br>It is connected to MII_TXD of external PHY. It is sent out at the rising edge of MII0_TXCLK.                            |
| 76   | TXEN0                             | O    | MII transmit enable<br>It is an output signal and is connected to MII_TXEN of external PHY. It is sent out at the rising edge of MII0_TXCLK. |
| 90   | COL0                              | I    | MII collision<br>It is an input signal and is connected to the MII_COL of external PHY.  |
| 84   | RXDV0                             | I    | MII receive data valid<br>It is an input signal and is connected to the MII_RXDV of external PHY. RXDV0 is used to frame RXD0[3:0].          |
| 88, 87,<br>86, 85  | RXD0_0, RXD0_1,<br>RXD0_2, RXD0_3 | I    | Receive data<br>It is NRZ data and is connected MII_RXD[3:0] of external PHY. It is received at the rising edge of MII0_RXCLK.               |
| 89   | MII0_RXCLK                        | I    | MII receive clock  |

**Pin description (continued)**

| Pin No.  | Label                             | Type | Description  |
|--|-----------------------------------|------|--|
| <b>External MII1 interface (PHY mode, MII1_PHY_MOD=1, P4EXT=1)</b> |                                   |      |  |
| 62   | MII1_TXCLK                        | O    | MII Transmit clock   |
| 61, 60,<br>59, 58  | TXD1_0, TXD1_1,<br>TXD1_2, TXD1_3 | I    | MII transmit data<br><br>It is sampled at the rising edge of MII1_TXCLK.                                       |
| 57   | TXEN1                             | I    | MII transmit enable<br><br>It is used to frame TXD1[3:0]. It is sampled at the rising edge of MII1_TXCLK.      |
| 69   | COL1                              | O    | MII collision<br><br>It is active when MII1 is half duplex and a collision event happens.                      |
| 63   | RXDV1                             | O    | MII receive data valid<br><br>It is used to frame RXD1[3:0]. It is sent out at the falling edge of MII1_RXCLK. |
| 67, 66,<br>65, 64  | RXD1_0, RXD1_1,<br>RXD1_2, RXD1_3 | O    | MII receive data<br><br>It is sent out at the falling edge of MII1_RXCLK.                                      |
| 68   | MII1_RXCLK                        | O    | MII receive clock  |

**Pin description (continued)**

| Pin No.  | Label                          | Type | Description  |
|--|--------------------------------|------|--|
| <b>External MII1 interface (MAC mode, MII1_PHY_MOD=0, P4EXT=1)</b> |                                |      |  |
| 62   | MII1_TXCLK                     | I    | MII Transmit clock<br><br>It is an input clock and it is connected to MII_TXCLK of external PHY  |
| 61, 60, 59, 58   | TXD1_0, TXD1_1, TXD1_2, TXD1_3 | O    | MII transmit data<br><br>It is connected to MII_TXD of external PHY. It is sent out at the rising edge of MII1_TXCLK                             |
| 57   | TXEN1                          | O    | MII transmit enable<br><br>It is an output signal and is connected to MII_TXEN of external PHY. It is sent out at the rising edge of MII1_TXCLK. |
| 69   | COL1                           | I    | MII collision<br><br>It is an input signal and is connected to the MII_COL of external PHY.  |
| 63   | RXDV1                          | I    | MII receive data valid<br><br>It is an input signal and is connected to the MII_RXDV of external PHY. RXDV1 is used to frame RXD1[3:0]           |
| 67, 66, 65, 64   | RXD1_0, RXD1_1, RXD1_2, RXD1_3 | I    | MII receive data<br><br>It is NRZ data and is connected MII_RXD[3:0] of external PHY. It is received at the rising edge of MII1_RXCLK            |
| 68   | MII1_RXCLK                     | I    | MII receive clock  |

Pin description (continued)

| Pin No.  | Label                             | Type | Description  |
|--|-----------------------------------|------|--|
| <b>External MII2 interface (PHY mode, MII2_MAC_MOD=0, MII2_EN=1)</b> |                                   |      |  |
| 109  | MII2_RXCLK                        | O    | MII receive clock  |
| 103  | MII2_TXCLK                        | O    | MII transmit clock   |
| 102, 101,<br>100, 97   | TXD2_0, TXD2_1,<br>TXD2_2, TXD2_3 | I    | MII transmit data<br><br>It is sampled at the rising edge of MII2_TXCLK.                                       |
| 96   | TXEN2                             | I    | MII transmit enable<br><br>It is used to frame TXD0[3:0]. It is sampled at the rising edge of MII2_TXCLK.      |
| 110  | COL2                              | O    | MII collision<br><br>It is active when MII2 is half duplex and a collision event happens.                      |
| 104  | RXDV2                             | O    | MII receive data valid<br><br>It is used to frame RXD0[3:0]. It is sent out at the falling edge of MII2_RXCLK. |
| 108, 107,<br>106, 105  | RXD2_0, RXD2_1,<br>RXD2_2, RXD2_3 | O    | MII receive data<br><br>It is sent out at the falling edge of MII2_RXCLK.                                      |

**Pin description (continued)**

| Pin No.  | Label                             | Type | Description  |
|--|-----------------------------------|------|--|
| <b>External MII2 interface (MAC mode, MII2_MAC_MOD=1, MII2_EN=1)</b> |                                   |      |  |
| 103  | MII2_TXCLK                        | I    | MII transmit clock<br><br>It is an input clock and it is connected to MII_TXCLK of external PHY.   |
| 102, 101,<br>100, 97   | TXD2_0, TXD2_1,<br>TXD2_2, TXD2_3 | O    | MII transmit data<br><br>It is connected to MII_TXD of external PHY. It is sent out at the rising edge of MII2_TXCLK.                            |
| 96   | TXEN2                             | O    | MII transmit enable<br><br>It is an output signal and is connected to MII_TXEN of external PHY. It is sent out at the rising edge of MII2_TXCLK. |
| 110  | COL2                              | I    | MII collision<br><br>It is an input signal and is connected to the MII_COL of external PHY.  |
| 104  | RXDV2                             | I    | MII receive data valid<br><br>It is an input signal and is connected to the MII_RXDV of external PHY. RXDV2 is used to frame RXD2[3:0].          |
| 108, 107,<br>106, 105  | RXD2_0, RXD2_1,<br>RXD2_2, RXD2_3 | I    | Receive data<br><br>It is NRZ data and is connected MII_RXD[3:0] of external PHY. It is received at the rising edge of MII2_RXCLK.               |
| 109  | MII2_RXCLK                        | I    | MII receive clock  |



**Pin description (continued)**

| Pin No.  | Label          | Type | Description   |
|--|----------------|------|---|
| <b>External RMIIO interface (RMII_EN=1, P4EXT=1)</b> |                |      |   |
| 88, 87   | RXD0_0, RXD0_1 | I    | RMII receive data<br><br>It is connected RMII_RXD[1:0] of external PHY or RMII_TXD[1:0] of external MAC.  |
| 84   | RXDV0          | I    | RMII receive data valid<br><br>It is connected RMII_RXDV of external PHY or RMII_TXEN of external MAC.    |
| 80, 79   | TXD0_0, TXD0_1 | O    | RMII transmit data<br><br>It is connected RMII_RXD[1:0] of external MAC or RMII_TXD[1:0] of external PHY. |
| 76   | TXEN0          | O    | RMII transmit enable<br><br>It is connected RMII_RXDV of external MAC or RMII_TXEN of external PHY.       |
| 77   | RMII0_CLK_OUT  | O    | A 50Mhz reference clock output for other RMII devices   |
| 89   | RMII0_CLK_IN   | I    | 50Mhz RMII reference clock input  |

**Pin description (continued)**

| Pin No.  | Label             | Type | Description  |
|--|-------------------|------|--|
| <b>External RMII1 interface (RMII_EN=1, MII1_DIS=0, MII1_PHY_MOD=1, P4EXT=1)</b> |                   |      |  |
| 67, 66   | RXD1_0, RXD1_1    | O    | RMII receive data<br><br>It is connected to RMII_TXD[1:0] of external PHY or RMII_RXD[1:0] of external MAC.  |
| 63   | RXDV1             | O    | RMII receive data valid<br><br>It is connected to RMII_TXEN of external PHY or RMII_RXDV of external MAC.    |
| 61, 60   | TXD1_0, TXD1_1    | I    | RMII transmit data<br><br>It is connected to RMII_RXD[1:0] of external PHY or RMII_TXD[1:0] of external MAC. |
| 57   | TXEN1             | I    | RMII transmit enable<br><br>It is connected to RMII_RXDV of external PHY or RMII_TXEN of external MAC.       |
| 65   | RMII1_PHY_CLK_OUT | O    | A 50Mhz reference clock output for other RMII devices  |
| 59   | RMII1_PHY_CLK_IN  | I    | 50Mhz RMII reference clock input   |

**Pin description (continued)**

| Pin No.  | Label             | Type | Description  |
|--|-------------------|------|--|
| <b>External RMII1 interface (RMII_EN=1, MII1_DIS=0, MII1_PHY_MOD=0, P4EXT=1)</b> |                   |      |  |
| 67, 66   | RXD1_0, RXD1_1    | I    | RMII receive data<br><br>It is connected to RMII_RXD[1:0] of external PHY or RMII_TXD[1:0] of external MAC.  |
| 63   | RXDV1             | I    | RMII receive data valid<br><br>It is connected to RMII_RXDV of external PHY or RMII_TXEN of external MAC.    |
| 61, 60   | TXD1_0, TXD1_1    | O    | RMII transmit data<br><br>It is connected to RMII_RXD[1:0] of external MAC or RMII_TXD[1:0] of external PHY. |
| 57   | TXEN1             | O    | RMII transmit enable<br><br>It is connected to RMII_RXDV of external MAC or RMII_TXEN of external PHY.       |
| 58   | RMII1_MAC_CLK_OUT | O    | A 50Mhz reference clock output for other RMII devices  |
| 68   | RMII1_MAC_CLK_IN  | I    | 50Mhz RMII reference clock input   |

**Pin description (continued)**

| Pin No.   | Label          | Type | Description   |
|---|----------------|------|---|
| <b>External RMII2 interface (RMII_EN=1, MII2_EN=1, P4EXT=1)</b> |                |      |   |
| 108, 107  | RXD2_0, RXD2_1 | I    | RMII receive data<br><br>It is connected RMII_RXD[1:0] of external PHY or RMII_TXD[1:0] of external MAC.  |
| 104   | RXDV2          | I    | RMII receive data valid<br><br>It is connected RMII_RXDV of external PHY or RMII_TXEN of external MAC.    |
| 102, 101  | TXD2_0, TXD2_1 | O    | RMII transmit data<br><br>It is connected RMII_RXD[1:0] of external MAC or RMII_TXD[1:0] of external PHY. |
| 96  | TXEN2          | O    | RMII transmit enable<br><br>It is connected RMII_RXDV of external MAC or RMII_TXEN of external PHY.       |
| 97  | RMII2_CLK_OUT  | O    | A 50Mhz reference clock output for other RMII devices   |
| 109   | RMII2_CLK_IN   | I    | 50Mhz RMII reference clock input  |

**Pin description (continued)**

| Pin No.  | Label      | Type | Description   |
|--|------------|------|---|
| <b>Force mode (the setting is latched at the end of reset)</b> |            |      |   |
| 103  | MAC5_F_100 | IPL1 | Force MAC5 work at 100M or 10M.<br>1: force 100M<br>0: force 10M (default)<br><br>It is used to force speed of the sixth switch port (MAC5) if P4EXT is pulled high.<br>The configuration function is disabled when MII2_EN is pulled high. |
| 104  | MAC4_F_100 | IPL1 | Force MAC4 work at 100M or 10M.<br>1: force 100M<br>0: force 10M (default)<br><br>It is used to force speed of the fifth switch port (MAC4) if P4EXT is pulled high.<br>The configuration function is disabled when MII2_EN is pulled high. |

**Pin description (continued)**

| Pin No.  | Label       | Type | Description  |
|--|-------------|------|--|
| <b>Force mode (the setting is latched at the end of reset)</b> |             |      |  |
| 108  | MAC5_F_FULL | IPL1 | Force MAC5 at full duplex or half duplex<br>1: force full duplex<br>0: force half duplex (default)<br><br>It is used to force duplex of the sixth switch port (MAC5) if P4EXT is pulled high.<br>The configuration function is disabled when MII2_EN is pulled high. |
| 109  | MAC4_F_FULL | IPL1 | Force MAC4 at full duplex or half duplex<br>1: force full duplex<br>0: force half duplex (default)<br><br>It is used to force duplex of the fifth switch port (MAC4) if P4EXT is pulled high.<br>The configuration function is disabled when MII2_EN is pulled high. |



Pin description (continued)

| Pin No.  | Label  | Type | Description   |
|--|--|------|---|
| <b>Transceiver</b>                                   |  |      |   |
| 127, 128,<br>11, 12,<br>18, 19,<br>29, 30,<br>33, 34 | RXIP0, RXIM0,<br>RXIP1, RXIM1,<br>RXIP2, RXIM2,<br>RXIP3, RXIM3,<br>RXIP4, RXIM4 | I    | TP receive  |
| 3, 4,<br>8, 9,<br>21, 22,<br>26, 27,<br>37, 38       | TXOP0, TXOM0,<br>TXOP1, TXOM1,<br>TXOP2, TXOM2,<br>TXOP3, TXOM3,<br>TXOP4, TXOM4 | O    | TP transmit   |
| 15   | BGRES  | O    | Band gap resister.<br><br>It is connected to GND through a 6.19 k ohm resistor. Please refer to application circuit for more information. |
| 2,125  | NC   | I    |   |

**Pin description (continued)**

| Pin No.  | Label          | Type         | Description   |
|--|----------------|--------------|---|
| <b>Misc.</b>   |                |              |   |
| 123  | X1             | I            | System clock input or crystal input<br><br>It is recommended to connect X1 and X2 to a crystal. If the clock source is from another chip, the clock should be active at least for 1ms before pin 93 RESETB de-asserted.   |
| 122  | X2             | O            | Crystal output  |
| 93   | RESETB         | I            | Reset, low active   |
| 52   | TEST2          | IPL          | Test mode enable<br><br>It should be connected to GND for normal operation.   |
| 116  | CRS2           | IPL          | Carrier sense of MII2 (home plug application)<br><br>It is valid only if CRS_EN is pull high<br>It is an input signal and is connected to MII_CRS of external PHY.  |
| 43   | CRS1           | IPL          | Carrier sense of MII1 (home plug application)<br><br>It is valid only if CRS_EN is pull high<br>It is an input signal and is connected to MII_CRS of external PHY.  |
| 44   | CRS0           | IPL          | Carrier sense of MII0 (home plug application)<br><br>It is valid only if CRS_EN is pull high<br>It is an input signal and is connected to MII_CRS of external PHY.  |
| 42   | INT            | IPL2/<br>O   | Interrupt output<br><br>It can be either active low or high by writing MII register 21.20[15]   |
| <b>EEPROM (only 24C02, 24C04, 24C08 &amp; 24C16 supported)</b> |                |              |   |
| 53   | SCL            | IPL2/<br>O   | After reset, it is used as clock pin SCL of EEPROM. Its period is longer than 10us. IP175DLF stops reading EEPROM if it finds there is no 55AA pattern in address 0. After reading EEPROM, this pin becomes an input pin. |
| 54   | SDA            | IPH2/<br>O   | After reset, it is used as data pin SDA of EEPROM. After reading EEPROM, this pin becomes an input pin. It is pulled up in EEPROM application circuit.  |
| <b>SMI</b>   |                |              |   |
| 71,<br>70  | MDC0,<br>MDIO0 | IPL,<br>IPL2 | SMI0<br><br>The external MAC device uses the interface to access IP175DLF's MII registers.  |



|            |                |               |  |
|------------|----------------|---------------|--|
| 113,<br>74 | MDC1,<br>MDIO1 | IPL2,<br>IPL2 | <p>SMI1</p> <p>IP175DLF uses the interface to polling the MII registers of external PHY to get its status. It is active only if p4ext is pulled high.</p> <p>If the external PHY doesn't support SMI, the polling result will be 16'hFFFF, and IP175DLF suppose the link status is good.</p> |
|------------|----------------|---------------|--|

Pin description (continued)

| Pin No.                       | Label          | Type | Description  |
|-------------------------------|----------------|------|--|
| <b>LED</b>                    |                |      |  |
| 92, 91                        | LED_SEL[1:0]   | IPH2 | LED output mode selection.<br>LED_SEL[1:0]=00: LED mode 0,<br>LED_SEL[1:0]=01: LED mode 1, dual color mode<br>LED_SEL[1:0]=10: LED mode 2,<br>LED_SEL[1:0]=11: LED mode 3 (default)  |
| 110, 107,<br>104, 101,<br>96  | LED_LINK[4:0]  | O    | Link, Activity (output after reset)<br><br>LED mode0: 100M Link + Activity (same as mode 2)<br>LED mode1:<br>LED mode2, 100M Link + Activity<br>(1: 100M Link fail, 0: 100M Link ok and no activity, flash: 100M Link ok and TX/RX activity)<br>LED mode3: Link + Activity<br>(1: link fail, 0: link ok, flash: Link ok and TX/ RX activity) |
| 111, 108,<br>105, 102,<br>97  | LED_SPEED[4:0] | O    | Speed (output after reset)<br><br>LED mode0: (1: no collision, flash: collision) (note*)<br>LED mode1:<br>LED mode2: Full/half: (1: half, 0: full, flash: collision)<br>LED mode3: (1: speed=10M, 0: speed=100M)   |
| 112, 109,<br>106, 103,<br>100 | LED_FULL[4:0]  | O    | Full/half, Link (output after reset)<br><br>LED mode0, 10M Link + Activity (same as mode 2)<br>LED mode1, same as mode 3<br>LED mode2, 10M Link + Activity<br>(1: 10M Link fail, 0: 10M Link ok and no activity, flash: 10M Link ok and TX/RX activity)<br>LED mode3: Full/half: (1: half, 0: full, flash: collision)                        |

**Note:** LED\_SPEED[0] shows collision information for all ports. LED\_SPEED[4:1] is undefined.

Pin description (continued)

| Pin No.   | Label               | Type      | Description   |          |
|---|---------------------|-----------|---|----------|
| <b>Dual color mode LED (It is active when LED_SEL[1:0] is {0,1}.)</b> |                     |           |   |          |
| 110, 107,<br>104, 101,<br>96  | LED_LINK[4:0]       | O         | Application circuit<br>   |          |
| 111, 108,<br>105, 102,<br>97  | LED_SPEED[4:0]      | O         |   |          |
|   |                     | Type      |   | LED_LINK |
|   |                     | LED_SPEED |   |          |
| Link off  |                     | O         |   | 0        |
| 100M link   |                     | O         |   | 1        |
| 100M link/ Activity   |                     | O         | Flash   |          |
| 10M link  |                     | O         | 0   |          |
| 10M link/ Activity  |                     | O         | 0   |          |
| Flash   |                     |           |   |          |
| 112, 109,<br>106, 103,<br>100   | LED_FULL[4:0]       | O         | Full/half, Link (output after reset)<br>Full/half: (1: half, 0: full, flash: collision) |          |
| <b>Serial LED (MII2_EN=1)</b>   |                     |           |   |          |
| 112   | SDATA               | O         | LED serial data   |          |
| 111   | SCLK                | O         | LED serial clock<br>Normal mode: 312.5KHz, Speed_up mode: 10MHz                         |          |
| <b>Power</b>  |                     |           |   |          |
| 72, 98  | VCC_O_1,<br>VCC_O_2 |           | 3.3V PAD power  |          |
| 1,6,10,14,<br>20,24,28,<br>35,40                                      | AVCC                |           | 1.9v Analog power   |          |
| 46,47,50,<br>55,82,94,<br>114,115,<br>124                             | VCC                 |           | 1.9v Core power   |          |
| 73, 99  | GND_O_1,<br>GND_O_2 |           | PAD Ground  |          |
| 5,7,13,16,<br>17,23,25,<br>31,32,39,<br>126                           | AGND                |           | Analog Ground   |          |
| 45,48,49,<br>56,83,95,<br>117,118,<br>121                             | GND                 |           | Core Ground   |          |

### 3 Function Description

#### 3.1 Flow Control

IP175DLF supports the standard 802.3X flow control frames on both transmit and receive sides. On the receive side, if IP175DLF receives a pause control frame, the IP175DLF will defer transmitting next normal frame; on the transmit side, IP175DLF issues pause control frame to remote station when the output of the destination port is overflowed. The source address (SA) of pause control frame will be {IP175DLF OUI (0090C3), port number}. For example, the SA of port 1 pause control frame will be "00 90 C3 00 00 01".

When CoS is enabled, IP175DLF may disable the flow control function for a short term to guarantee the bandwidth of high priority packets. A port disables its flow control function for 2 ~ 3 seconds when it receives the highest priority packet. It doesn't transmit pause frame or jam pattern during the period but it still responses to pause frame or jam pattern.

IP175DLF's PHY 0~4 MII register 4.10 can not use to set flow control ability for each port. The flow control function can be only enabled by pulling up pin 100 (X\_EN) or by programming MII register 20.5[1].

#### 3.2 Broadcast Storm Protection

A port of IP175DLF begins to drops broadcast packets if the received broadcast packets are more than the threshold defined in MII register 20.17~20.19 bq\_stm\_thr\_sel [1:0] in 10ms (100Mbps) or 100ms (10Mbps).

The function can be enabled by pulling high pin 102 (BF\_STM\_EN) or programming MII register 20.16[13:8].

#### 3.3 Rate Control

The rate control is provided by applying to port rate control, Multi-Field traffic policy and WFQ scheduling. IP175DLF use token bucket to measure the traffic to against the traffic profile. The traffic profile is a predefine traffic rate which contain three parameters: timing interval<sup>1</sup>, credit size and burst size. User can configure desired rate from MII register 21.8-12, except for Multi-Field traffic policy. Configuring rate parameter of Multi-Field traffic policy is from MII register 26.16-17. When the rate has been configured, the meter measure the traffic and then against its predefined traffic profile. Switch passes in-of-profile packets and drop (or shape) out-of-profile packets in ingress (or egress).

---

<sup>1</sup> In ingress port rate control and Multi-Field traffic policy, timing interval parameter is fixed to 1ms.

The rate control equation that used in IP175DLF is illustrated below:

$$\text{TX or TX output queue number bandwidth (Byte per second)} = \frac{\text{credit\_size (byte)}}{\text{ti x 1ms}}$$

$$\text{RX or Multi-Field table ingress QoS bandwidth (Byte per second)} = \frac{\text{credit\_size (byte)}}{1\text{ms}}$$

**MBS:** max burst size is use as a compensation buffer during idle period.

bw\_mbs must be greater than bw\_credit\_size and max\_packet\_length  
( **bw\_mbs > bw\_credit\_size** and **bw\_mbs > max\_packet\_length** )

**CREDIT\_SIZE:** credit size that will add into bucket per time interval

**TI:** time interval (unit 1ms)

Example: TX Bandwidth 256kbps ( max\_packet\_length = 1518 byte = 16'h05EE )

$$256\text{kbps} = 32\text{kBps} = \frac{32}{1 \times 1\text{ms}}$$

1. bw\_credit\_size = 16'h0020
2. bw\_mbs = 16'h0700
3. bw\_ti = 16'h0001

Example: RX Bandwidth 512kbps (max\_packet\_length = 1518 byte = 16'h05EE)

$$512\text{kbps} = 64\text{kBps} = \frac{64}{1\text{ms}}$$

1. bw\_credit\_size = 16'h0040
2. bw\_mbs = 16'h0700

### 3.4 External MII

IP175DLF provides the ability of the connection to an external MAC or PHY. There are three MII interfaces allow to connect between the switch and external MAC (or PHY), and term as MII0, 1, and 2 respectively. These interfaces give a flexible application, such as HomePNA, SOHO router and gateway application. Each MII interface can be configured MAC mode or PHY mode without modify layout. In addition to be compatible with IEEE 802.3 MII interface, the interface also can configure RMII or SNI<sup>2</sup>. Figure 3-1 illustrates an external MII application example.

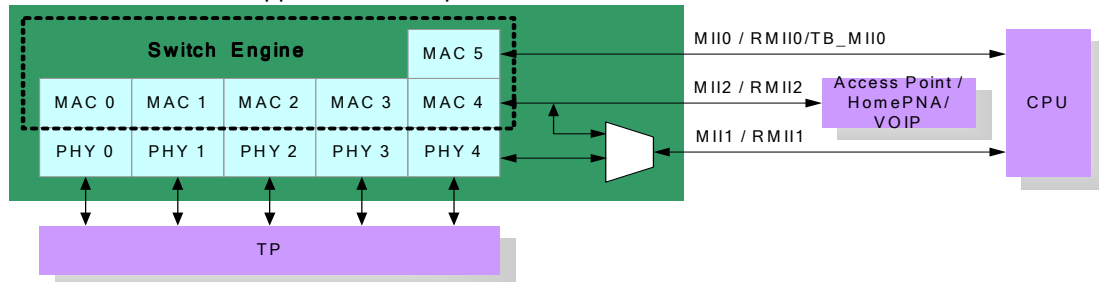


Figure 3-1 External MII application

| I/F                | mode                  | Int  | p4ext | mii1_dis | mii2_en | p4mii_sni <sup>3</sup> | rmii_en <sup>4</sup> | tb_mii_0_en | mii0_mac_mod | mii1_phy_mode | mii2_mac_mod |
|--------------------|-----------------------|------|-------|----------|---------|------------------------|----------------------|-------------|--------------|---------------|--------------|
| <b>MII0</b>        |                       |      |       |          |         |                        |                      |             |              |               |              |
| TBMII <sup>5</sup> | PHY mode              | MAC5 | 1     | X        | X       | 0                      | 0                    | 1           | 0            | X             | X            |
| TBMII              | MAC mode              | MAC5 | 1     | X        | X       | 0                      | 0                    | 1           | 1            | X             | X            |
| MII                | PHY mode              | MAC5 | 1     | X        | X       | 0                      | 0                    | 0           | 0            | X             | X            |
| MII                | MAC mode              | MAC5 | 1     | X        | X       | 0                      | 0                    | 0           | 1            | X             | X            |
| RMII               | MAC <sup>6</sup>      | MAC5 | 1     | X        | X       | 0                      | 1                    | 0           | X            | X             | X            |
| SNI                | PHY mode              | MAC5 | 1     | X        | X       | 1                      | 0                    | 0           | 0            | X             | X            |
| SNI                | MAC mode              | MAC5 | 1     | X        | X       | 1                      | 0                    | 0           | 1            | X             | X            |
| <b>MII1</b>        |                       |      |       |          |         |                        |                      |             |              |               |              |
| MII                | PHY mode              | PHY4 | 1     | 0        | X       | X                      | 0                    | 0           | X            | 1             | X            |
| MII                | MAC mode              | MAC4 | 1     | 0        | 0       | X                      | 0                    | 0           | X            | 0             | X            |
| RMII               | PHY mode              | PHY4 | 1     | 0        | X       | X                      | 1                    | 0           | X            | 1             | X            |
| RMII               | MAC mode              | MAC4 | 1     | 0        | 0       | X                      | 1                    | 0           | X            | 0             | X            |
| <b>MII2</b>        |                       |      |       |          |         |                        |                      |             |              |               |              |
| MII                | PHY mode              | MAC4 | 1     | X        | 1       | X                      | 0                    | 0           | X            | X             | 0            |
| MII                | MAC mode <sup>7</sup> | MAC4 | 1     | X        | 1       | X                      | 0                    | 0           | X            | X             | 1            |
| RMII               | MAC                   | MAC4 | 1     | X        | 1       | X                      | 1                    | 0           | X            | X             | X            |

<sup>2</sup> Only MII0 interface can set to SNI.

<sup>3</sup> RMII\_EN takes precedence of P4MII\_SNI.

<sup>4</sup> The rmii\_en is a global pin setting to enable RMII connector for MII0-2. User can also respectively set RMII connector from MII register 21\_3[10:8].

<sup>5</sup> The MII0 clock support speed up 50MHz to achieve the 200Mbps throughput.

<sup>6</sup> Whether RMII0 or RMII2 can also connects to external MAC or PHY device by swapping the data path layout.

<sup>7</sup> It is noted that MII2 and MII1 MAC mode can't be enabled at the same time. That is, user should not use MII2 if pin 54 MII1\_PHY\_MOD is pulled low.

Abbreviation:

I/F: the type of interface

Mode: the port works as a MAC or a PHY

Int: the internal block to which the MII port is connected

MAC4: the port 4 of switch engine

MAC5: the port 5 of switch engine

PHY4: the port 4 of PHY

### 3.4.1 To define the speed, duplex and pause of MII port

MII interface can be configured as either MAC mode or PHY mode. In MAC mode and PHY mode, the MII port's speed, duplex and pause ability can set through pin, EEPROM or MII register. In MAC mode it can also use polling PHY status to get PHY link capability. Therefore IP175DLF provide MDC1/MDIO1 for polling PHY status. The details are shown in the following tables.

#### MII0 PHY mode

|             | Pin         | EEPROM          |     | MII register    |     |      |
|-------------|-------------|-----------------|-----|-----------------|-----|------|
|             |             | Name            | Reg | Name            | Phy | Reg  |
| MII0 speed  | MAC5_F_100  | MAC5_FORCE_100  | 2.7 | MAC5_FORCE_100  | 20  | 4.15 |
| MII0 duplex | MAC5_F_FULL | MAC5_FORCE_FULL | 2.5 | MAC5_FORCE_FULL | 20  | 4.13 |
| MII0 pause  | --          | MAC_X_EN        | 3.0 | MAC_X_EN        | 20  | 5.0  |

**MII0 MAC mode:** There are two ways to set MII0 speed, duplex and pause.

1. Decided by reading the MII registers 0~5 of external PHY through MDC1, MDIO1.

|                                  |   |
|----------------------------------|---|
| MII0<br>Speed<br>Duplex<br>Pause | <ol style="list-style-type: none"> <li>1. IP175DLF polls the external PHY with address defined in MII register 21.1[4:0]. The default address value is 00000.</li> <li>2. After reset, IP175DLF writes the speed/duplex/pause capability to the external PHY using the content of MII register 21.1[12:8].</li> <li>3. IP175DLF reads MII register 0~5 of external PHY as MII0 speed, duplex and pause continuously.</li> </ol> |
|----------------------------------|---|

2. Force mode (MDC1 and MDIO1 are not connected to external PHY)

|             | Pin         | EEPROM          |     | MII register    |     |      |
|-------------|-------------|-----------------|-----|-----------------|-----|------|
|             |             | Name            | Reg | Name            | Phy | Reg  |
| MII0 speed  | MAC5_F_100  | MAC5_FORCE_100  | 2.7 | MAC5_FORCE_100  | 20  | 4.15 |
| MII0 duplex | MAC5_F_FULL | MAC5_FORCE_FULL | 2.5 | MAC5_FORCE_FULL | 20  | 4.13 |
| MII0 pause  | --          | MAC_X_EN        | 3.0 | MAC_X_EN        | 20  | 5.0  |

**MII1 PHY mode:** In MII1 PHY mode, the MII1 interface connects to 5<sup>th</sup> PHY in IP175DLF and this PHY address is 4. The external device can read this PHY's MII management registers via MID1/MDIO1.

|                         | Pin | EEPROM |     | MII register |     |     |
|-------------------------|-----|--------|-----|--------------|-----|-----|
|                         |     | Name   | Reg | Name         | Phy | Reg |
| MII1 speed/duplex/pause | --  | --     |     |              | 4   | 0~5 |

**MII1 MAC mode:** There are two ways to set MII1's speed, duplex and pause.

1. IP175DLF reads the MII registers 0~5 of external PHY through MDC1, MDIO1.

|                               |   |
|-------------------------------|---|
| MII1 Speed<br>Duplex<br>Pause | <ol style="list-style-type: none"> <li>1. IP175DLF polls the external PHY with address defined in MII register 21.2[4:0]. The default address value is 00001.</li> <li>2. After reset, IP175DLF writes the speed/duplex/pause capability to the external PHY using the content of MII register 21.2[12:8].</li> <li>3. IP175DLF reads MII register 0~5 of external PHY as MII1 speed, duplex and pause continuously.</li> </ol> |
|-------------------------------|---|

2. Force mode (MDC1 and MDIO1 are not connected to external PHY)

|             | Pin         | EEPROM          |     | MII register    |     |      |
|-------------|-------------|-----------------|-----|-----------------|-----|------|
|             |             | Name            | Reg | Name            | Phy | Reg  |
| MII1 speed  | MAC4_F_100  | MAC4_FORCE_100  | 2.6 | MAC4_FORCE_100  | 20  | 4.14 |
| MII1 duplex | MAC4_F_FULL | MAC4_FORCE_FULL | 2.4 | MAC4_FORCE_FULL | 20  | 4.12 |
| MII1 pause  | --          | MAC_X_EN        | 3.0 | MAC_X_EN        | 20  | 5.0  |



**MII2 PHY mode**

|             | Pin         | EEPROM          |     | MII register    |     |      |
|-------------|-------------|-----------------|-----|-----------------|-----|------|
|             |             | Name            | Reg | Name            | Phy | Reg  |
| MII2 speed  | MAC4_F_100  | MAC4_FORCE_100  | 2.6 | MAC4_FORCE_100  | 20  | 4.14 |
| MII2 duplex | MAC4_F_FULL | MAC4_FORCE_FULL | 2.4 | MAC4_FORCE_FULL | 20  | 4.12 |
| MII2 pause  | --          | MAC_X_EN        | 3.0 | MAC_X_EN        | 20  | 5.0  |

**MII2 MAC mode:** There are two ways to set MII2 speed, duplex and pause.

1. IP175DLF reads the MII registers 0~5 of external PHY through MDC1, MDIO1.

|                                  |   |
|----------------------------------|---|
| MII2<br>Speed<br>Duplex<br>Pause | <ol style="list-style-type: none"> <li>1. IP175DLF polls the external PHY with address defined in MII register 21.2[4:0]. The default address value is 00001.</li> <li>2. After reset, IP175DLF writes the speed/duplex/pause capability to the external PHY using the content of MII register 21.2[12:8].</li> <li>3. IP175DLF reads MII register 0~5 of external PHY as MII2 speed, duplex and pause continuously.</li> </ol> |
|----------------------------------|---|

2. Force mode (MDC1 and MDIO1 are not connected to external PHY)

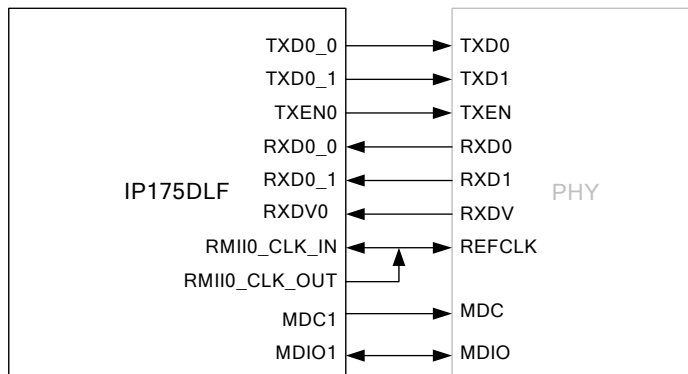
|             | Pin         | EEPROM          |     | MII register    |     |      |
|-------------|-------------|-----------------|-----|-----------------|-----|------|
|             |             | Name            | Reg | Name            | Phy | Reg  |
| MII2 speed  | MAC4_F_100  | MAC4_FORCE_100  | 2.6 | MAC4_FORCE_100  | 20  | 4.14 |
| MII2 duplex | MAC4_F_FULL | MAC4_FORCE_FULL | 2.4 | MAC4_FORCE_FULL | 20  | 4.12 |
| MII2 pause  | --          | MAC_X_EN        | 3.0 | MAC_X_EN        | 20  | 5.0  |

### 3.4.2 The Application Circuit of RMII

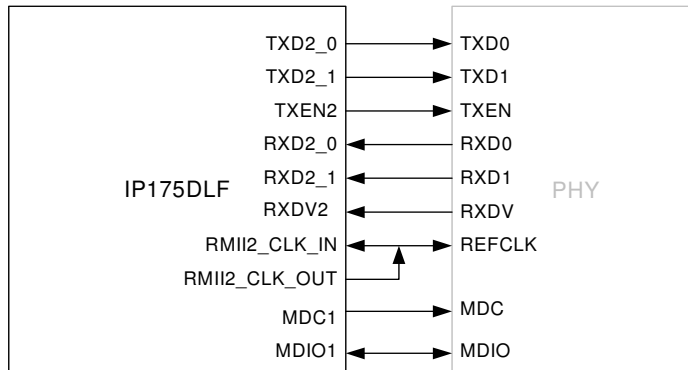
(P4EXT=1, P4MII\_SNI=0, RMII\_EN=1)

When RMII mode is enabled, IP175DLF supports reference clock RMII\_CLK\_OUT for each RMII port. The clock is used by the external PHY (or MAC) and 175D itself.

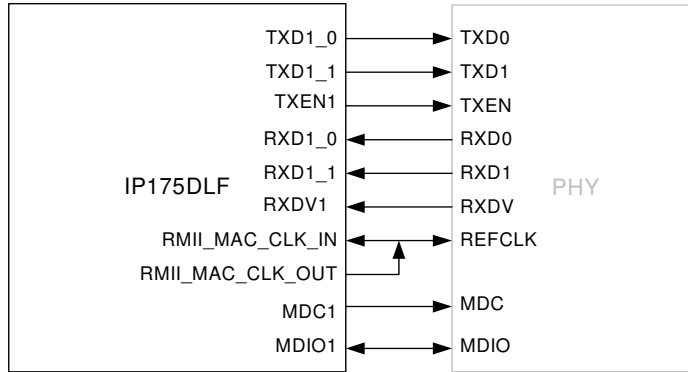
The following circuit diagram is the RMII circuit of MII0.



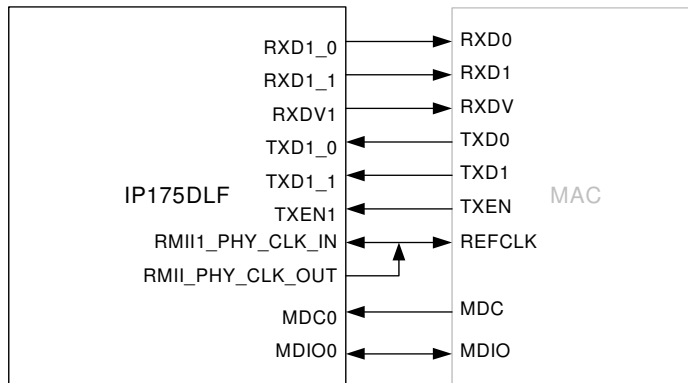
The following circuit diagram is the RMII circuit of MII2.



The following circuit diagram is the RMI1 circuit of MII1 MAC mode.



The following circuit is the RMI1 circuit of MII1 PHY mode.



### 3.5 Virtual LAN (VLAN)

IP175DLF is a VLAN aware-switch and support two classification rule: port-based VLAN and tag-based VLAN. Each port can configure its classification rule respectively. In tag-based VLAN the switch supports up to 16 VLAN groups. Two ingress VLAN rule and egress VLAN rule are provided. The ingress VLAN rule is used to discard packet that violate this rule. The egress rule checks VLAN member set and performs the determination of tagging or un-tagging. In learning process the switch supports shared and independent VLAN learning.

The VLAN table contains a set of match condition and their actions. Entry 0-5 firstly reserved for port-based VLAN if the corresponding port is set to port-based VLAN. For instance port 0 is set to port-based VLAN classification and then entry 0 is reserved for port 0. In port-based VLAN the match condition does not care and it is only used for tag-based VLAN. The context of VLAN table is placed in MII register 22.11-29 and 23.0-31.

|          | match condition |     |     |             | action  |            |           |            |         |           |        |                 |             |
|----------|-----------------|-----|-----|-------------|---------|------------|-----------|------------|---------|-----------|--------|-----------------|-------------|
|          | Valid           | VID | FID | VLAN_MEMBER | ADD_TAG | REMOVE_TAG | LEARN_DIS | STP_IDX_EN | STP_IDX | QU_NUM_EN | QU_NUM | REW_VLAN_PRI_EN | REW_VLAN_PR |
| Entry 0  |                 |     |     |             |         |            |           |            |         |           |        |                 |             |
| ...      |                 |     |     |             |         |            |           |            |         |           |        |                 |             |
| Entry 15 |                 |     |     |             |         |            |           |            |         |           |        |                 |             |

Figure 3-2 VLAN table

#### 3.5.1 Port-based VLAN

If any packet is received by a given port, the switch will perform VLAN table searching. User can use the VLAN Classification Register to set VLAN classification rule on each port. In port-based VLAN classification, frame is classified based on the port which it arrive. Once a port configures port-based VLAN, it will occupy the corresponding VLAN entry.

#### 3.5.2 Tag-based VLAN

In tag-based VLAN classification two modes are provided for applying VLAN classification: using VID to classify VLAN and using PVID to classify VLAN. Using VID to classify VLAN, VID searching is performed according to frame's VID. If any packets carrier no VID information, the VID searching is performed using PVID. In using PVID to classify VLAN the PVID for a given port is used for VID searching, whether VLAN tagged or untagged frames are received on this port.

#### 3.5.3 VLAN Ingress Filtering

IP175DLF specify a VLAN ingress rule in MII register 22.1. Any frames received on a port are discarded if it violates this rule.

#### 3.5.4 Shared and Independent VLAN Learning

The learning process supports shared and independent VLAN learning. In shared VLAN learning rule the learning information from a VLAN can make used by the others VLANs. In independent VLAN learning rule the learning information from a VLAN makes use only itself. This standard was specified in IEEE 802.1Q.

#### 3.5.5 The determination of the requirement to insert or remove tag

IP175DLF supports the ability of insertion and removal tag header. User can configure the set of ports that add or remove tag header for each VLAN through MII register 23.8-23. Table 1 is a combination of frame type and transmission port type.

| Frame type of the received packet | The operation of a port which forwards the packet |  |
|-----------------------------------|---|--|
|                                   | Forward to a untagged filed                       | Forward to a tagged field  |
| Untagged                          | Forward the packet without modification           | Insert a tag using the default VLAN tag value of the source port |
| Priority-tagged (VLAN ID=0)       | Strip tag   | Only Replace the VID with PVID of the source port                |
| VLAN-tagged                       | Strip tag   | Forward the packet without modification                          |

**Table 1 Determination of insertion and removal tag**

### 3.6 Quality of Service (QoS)

IP175DLF uses a combination of traffic policy, priority classification and output queue scheduling to achieve policy-based QoS. Since current internet carrier different type services, such as file transfer, email, video, voice and Web. Because the switch offers a limited resource, it can not assure any resource guarantees to applications or users. Traffic policy can aggregate traffic flow and police against its traffic profile. This way can restrain the traffics from entering the switch effectively. Finally, packets will place into appropriate output queue based on priority classification.

#### 3.6.1 Traffic Policy

In IP175DLF traffic policy is a consisting of classifier, meter and dropper. The classifier separate received packets into different traffic stream based on matched condition. IP175DLF provides 8 Multi-Field entries, each entry is a combination of one or more layer 2-4 header. Multi-Field classification can classify packets into traffic classes and traffic flows. For instance an end-to-end flow is recognized using five-tuple. Each Multi-Field contains a meter for measuring the traffic. The meter passes the in-of-profile packets for forwarding and put out-of-profile packets into dropper for dropping. User can configure the parameters of traffic policy from MII register 26.0-23.

Each entry associated with Multi-Field counter is in order to monitor traffic rate by user (or CPU). The counter value is represented in byte units. The user (or CPU) can monitor the traffic rate to periodically read the value of multi-field counter through MII register.

#### 3.6.2 Priority Classification

Priority classification is used to separate packets into four priority levels. In IP175DLF packet classification can categorize packets based on port-based classification and frame-based classification. Port-based classification, packets coming from the same port have a fixed priority level. Frame-based classification, frame categorization is based on one header filed or a combination of more header fields. In frame-based classification has a flexible packet classification to classify priority level and the following header fields are provided by determining the priority.

- Special tag
- Source MAC address
- Destination MAC address
- VID
- VLAN priority
- IPv4 ToS/IPv6 DSCP
- TCP/UDP logical port
- Layer 2-4 Multi-Field

Figure 3-3 illustrates the priority classification flow chart.

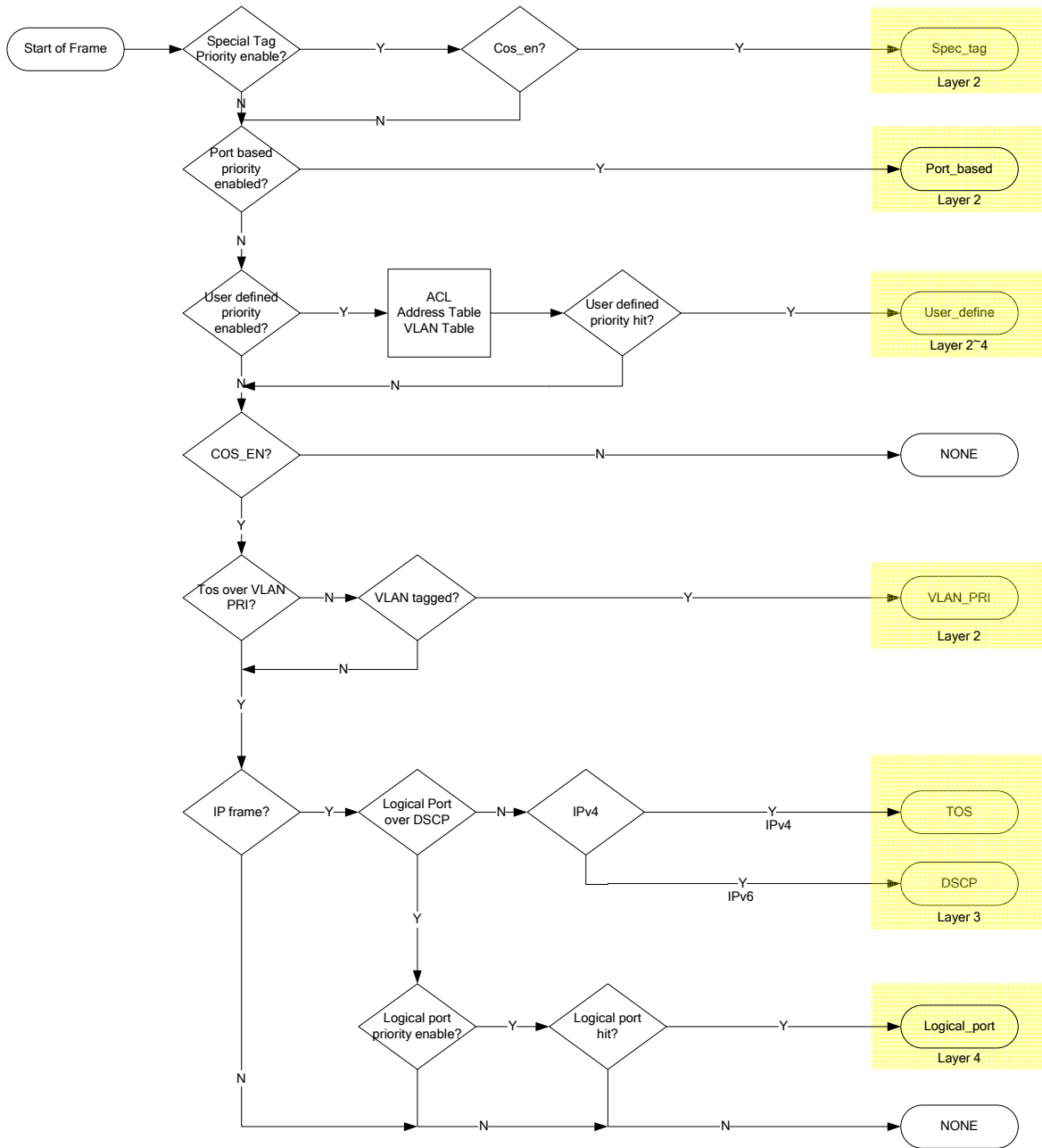


Figure 3-3 Priority classification flow chart

### 3.6.3 Output Queue Scheduling

IP175DLF support four scheduling modes and list in Table 2.

| Mode # | Q3  | Q2  | Q1  | Q0      |
|--------|-----|-----|-----|---------|
| Mode 0 | WRR | WRR | WRR | WRR     |
| Mode 1 | WFQ | WFQ | WFQ | WFQ(BE) |
| Mode 2 | SP  | WFQ | WFQ | BE      |
| Mode 3 | SP  | SP  | SP  | SP      |

SP: Strictly Priority; WRR: Weight Round Robin; WFQ: Weight Fair Queuing; BE: Best Effort

**Table 2 Queue scheduling**

**SP:**

In strictly priority, the packets in a queue will go first till its queue is empty.

**WRR:**

User can control the number of packet transmission on an output queue by setting its weight.

**WFQ:**

User can allocate a bandwidth on an output queue by setting its rate. Configuring WFQ bandwidth can be through MII register 21.8-12.

### 3.7 Port mirror

There are some circumstances that the network administrator requires to monitor the network status. The port mirroring function can help the network administrator diagnose the network.

A port mirroring function can be accomplished by assigning a monitored port and a snooping port. The IP175DLF supports four kinds of monitoring methods: source port, destination port, one port of source and destination, source-destination pair. This function can be enabled by programming the corresponding bit in MII registers 20.20~20.21.

In addition to monitor a physical port, it can monitor traffic based on layer 2-4 Multi-Field packet header or MAC address

### 3.8 Layer 2-4 Multi-Field Classification

IP175DLF support 8 Multi-Field entries. The Multi-Field table consists of a set of classification rules and actions. This Multi-Field classification is a combination of one or more layer 2-4 packet header. The classifier can classify incoming traffic to traffic class and traffic flow. The traffic class is a collection with the same conditions. For example the classifier aggregates a collection of packet with the same DSCP. Traffic flow can identify end-to-end traffic flow by using five-tuple (source IP, destination IP, protocol, source port and destination port).

When packets are received by a port, the switch will search Multi-Field table. If incoming packets match a predefined Multi-Field entry, the corresponding action is performed. The action consists of six parameters: drop packet, limits incoming traffic bandwidth, monitor traffic bandwidth, forward to CPU, copy to mirror port and queue number assignment. It is possible to match multiple entries for an incoming packet and then the first matching entry is effective.

Each entry includes a counter called Multi-Field counter. This counter is useful for monitoring propose. A counter keeps track of the number of bytes match predefined Multi-Filed condition. User also can periodically read a Multi-Field to monitor a specific traffic rate.

### 3.9 MAC Address Table

P175D support 2K MAC addresses. The address table can configure either 2K unicast address or 1K unicast address/1K multicast address. The multicast table occupies the MAC table from 0x400 to 0x7FF if the AT\_STR bit (reg 20.13.3) set to high. The MAC table is organized as hash table which consist of 512

buckets with four entries in each bucket. Each bucket is located through its respective hash key, calculated from MAC and FID by using XOR algorithm. It is possible that multiple MAC addresses index to the same bucket, term as collision. IP175DLF provides four entries within each buck for reducing collision rate. Finally, the 11-bit hash index mapping to MAC table consist of three parameters: multicast address bit, hash key and entry number. The MSB of hash index distinguishes multicast address from MAC addresses. The least two significant bit in hash index indicates entry number. The other bit is hash key which calculated from MAC and FID using XOR algorithm. In IP175DLF the formula of hash index is computed based on table structure. The user can set AT\_STR bit to configure table structure. The 11-bit hash index is computed as following:

**AT\_STR=0 (2K unicast table)**

Hash Index = { XOR( {2'b00,FID,MAC[47:45]}, MAC[44:36], MAC[35:27], MAC[26:18], MAC[17:9], MAC[8:0] ), Entry Number }

**AT\_STR=1 (1K unicast table and 1K multicast table)**

Hash Index = {Multicast Address Bit, XOR( {4'h0,FID}, MAC[47:40], MAC[39:32], MAC[31:24], MAC[23:16], MAC[15:8], MAC[7:0] ), Entry Number }

**3.9.1 Entry Content**

Entry content in MAC table contains the forwarding information for a specific MAC address. This table content is automatically updated by learning process and can directly access from the CPU through Address Table Access register (see MII register 21.14-19).

The contents are described in Table 3, Table 4 and Table 5.

| MII Register | Name            | Description   |
|--------------|-----------------|---|
| 21.15        | MAC_ADDR[15:0]  | MAC address[15:0]   |
| 21.16        | MAC_ADDR[31:16] | MAC address[31:16]  |
| 21.17        | MAC_ADDR[47:32] | MAC address[47:32]  |
| 21.18[15:14] | FILTER_INFO     | Filter information: <ul style="list-style-type: none"> <li>- 2'b00: reserved</li> <li>- 2'b01: discard frame if frame's SMAC match MAC address</li> <li>- 2'b10: ignore VLAN member set</li> <li>- 2'b11: copy frame to mirror port if frame's DMAC match MAC address</li> </ul>  |
| 21.18[13:10] | PRI_INFO        | Priority information: To assign queue number for frames with match MAC table entry. The information is divided two parts: match condition and its action. <p><b>Match Condition (21.18[13:12]):</b></p> <ul style="list-style-type: none"> <li>- 2'b00: reserved</li> <li>- 2'b01: match DMAC (Destination MAC Address)</li> <li>- 2'b10: match SMAC (Source MAC Address)</li> <li>- 2'b11: match DMAC or SMAC</li> </ul> <p><b>Action (21.18[11:10]):</b></p> <ul style="list-style-type: none"> <li>- Assign to Queue 0</li> <li>- Assign to Queue 1</li> <li>- Assign to Queue 2</li> <li>- Assign to Queue 3</li> </ul> |
| 21.18[9:6]   | FID             | 4-bit FID   |
| 21.18[5:3]   | PORT_ID         | Port ID: <ul style="list-style-type: none"> <li>- 3'b000: discard frame if frame's DMAC match MAC address</li> <li>- 3'b001- 3'b110: port ID</li> <li>- 3'b111: reserved</li> </ul>   |
| 21.18[2:0]   | AGE             | Age time: If this field is set all zero, it indicates the corresponding   |



|         |          |  |
|---------|----------|--|
|         |          | entry is aged out. It means entry is invalid.  |
| 21.19.0 | Reserved | Reserved   |
| 21.19.1 | STATIC   | Static entry: this entry is not aged out by aging process or overwritten by learning process |

**Table 3 Entry content for unicast MAC address**

| MII Register | Name            | Description   |
|--------------|-----------------|---|
| 21.15        | MAC_ADDR[15:0]  | MAC address[15:0]   |
| 21.16        | MAC_ADDR[31:16] | MAC address[31:16]  |
| 21.17        | MAC_ADDR[47:32] | MAC address[47:32]  |
| 21.18[15:14] | FILTER_INFO     | Filter information: <ul style="list-style-type: none"> <li>- 2'b00: reserved</li> <li>- 2'b01: discard frame if frame's SMAC match MAC address</li> <li>- 2'b10: ignore VLAN member set</li> <li>- 2'b11: copy frame to mirror port if frame's DMAC match MAC address</li> </ul>  |
| 21.18[13:10] | PRI_INFO        | Priority information: To assign queue number for frames with match MAC table entry. The information is divided two parts: match condition and its action. <p><b>Match Condition (21.18[13:12]):</b></p> <ul style="list-style-type: none"> <li>- 2'b00: reserved</li> <li>- 2'b01: match DMAC (Destination MAC Address)</li> <li>- 2'b10: match SMAC (Source MAC Address)</li> <li>- 2'b11: match DMAC or SMAC</li> </ul> <p><b>Action (21.18[11:10]):</b></p> <ul style="list-style-type: none"> <li>- Assign to Queue 0</li> <li>- Assign to Queue 1</li> <li>- Assign to Queue 2</li> <li>- Assign to Queue 3</li> </ul> |
| 21.18[9:6]   | FID             | 4-bit FID   |
| 21.18[5:0]   | PORT_MAP        | Port Map: <ul style="list-style-type: none"> <li>- 0x00: discard frame if frame's DMAC match MAC address</li> <li>- 0x01 to 0x3F: destination port map</li> </ul>   |
| 21.19.0      | IGMP            | IGMP entry indicator: This bit shall set to zero  |
| 21.19.1      | Valid           | Entry is valid  |

**Table 4 Entry content for multicast MAC address**

| MII Register               | Name            | Description  |
|----------------------------|-----------------|--|
| 21.15                      | MAC_ADDR[15:0]  | MAC address[15:0]  |
| 21.16[6:0]                 | MAC_ADDR[22:16] | MAC address[22:16]   |
| 21.16.7                    | MAC_ADDR[23]    | This bit shall be set to zero  |
| 21.16[10:8]                | TIMEOUT_P0      | Port 0 timeout: If this field is set all zero, it indicates the corresponding port is timeout. |
| 21.16[13:11]               | TIMEOUT_P1      | Port 1 timeout   |
| {21.17.0,<br>21.16[15:14]} | TIMEOUT_P2      | Port 2 timeout   |
| 21.17[3:1]                 | TIMEOUT_P3      | Port 3 timeout   |
| 21.17[6:4]                 | TIMEOUT_P4      | Port 4 timeout   |
| 21.17[9:7]                 | TIMEOUT_P5      | Port 5 timeout   |
| 21.17[15:0]                | Reserved        | Reserved   |
| 21.18[15:14]               | FILTER_INFO     | Filter information:  |

|              |          |  |
|--------------|----------|--|
|              |          | <ul style="list-style-type: none"> <li>- 2'b00: reserved</li> <li>- 2'b01: discard frame if frame's SMAC match MAC address</li> <li>- 2'b10: ignore VLAN member set</li> <li>- 2'b11: copy frame to mirror port if frame's DMAC match MAC address</li> </ul>   |
| 21.18[13:10] | PRI_INFO | <p>Priority information: To assign queue number for frames with match MAC table entry. The information is divided two parts: match condition and its action.</p> <p><b>Match Condition (21.18[13:12]):</b></p> <ul style="list-style-type: none"> <li>- 2'b00: reserved</li> <li>- 2'b01: match DMAC (Destination MAC Address)</li> <li>- 2'b10: match SMAC (Source MAC Address)</li> <li>- 2'b11: match DMAC or SMAC</li> </ul> <p><b>Action (21.18[11:10]):</b></p> <ul style="list-style-type: none"> <li>- Assign to Queue 0</li> <li>- Assign to Queue 1</li> <li>- Assign to Queue 2</li> <li>- Assign to Queue 3</li> </ul> |
| 21.18[9:6]   | FID      | 4-bit FID  |
| 21.18[5:0]   | PORT_MAP | <p>Port Map:</p> <ul style="list-style-type: none"> <li>- 0x00: discard frame if frame's DMAC match MAC address</li> <li>- 0x01 to 0x3F: destination port map</li> </ul>   |
| 21.19.0      | IGMP     | IGMP entry indicator: This bit shall set to one  |
| 21.19.1      | Valid    | Entry is valid   |

**Table 5 Entry content for IP multicast address**

### 3.9.2 Accessing MAC Table

The MAC table can be accessed by through MII register 21.14-19. IP175DLF provides two access commands: single read and single write. A single read or write transfer only executes a single I/O operation and user only can access a particular memory address. When a given MAC+FID read from (or write to) MAC table, the MAC+FID is used to compute hash index for mapping to MAC table.

#### Single Read

The single read process is described as following steps:

Step 1 – Set hash index in reg 21.14[10:0]

Step 2 – Set single read command in reg 21.14[12:11]

Step 3 – Set START bit in reg 21.14.15 to initiate read command

Step 4 – check DATA\_VALID bit in reg 21.14.13 to determine if data is valid. If this bit is set to high, enter to step 5

Step 5 – read data from data buffer register (reg 21.15-19). User must read data buffer register from reg 21.15 to reg 21.19 in regular order.

#### Single Write

The single write process is described as following steps:

Step 1 – Write desired data to data buffer register (reg 21.15-19)

Step 2 – Set hash index in reg 21.14[10:0]

Step 3 – Set single write command in reg 21.14[12:11]

Step 4 – Set START bit in reg 21.14.15 to initiate read command

### 3.10 CPU Interrupt Control

IP175DLF uses interrupt to notify CPU of switch status. Each interrupt can be individually enabled by interrupt enable register. User can decide interrupt signal is active high or low.

### 3.11 IGMP Snooping

IP175DLF support IGMP v1 and v2 snooping specified in RFC 1112 and RFC 2236 respectively. Because IGMP is used between hosts and neighboring multicast routers, IP175DLF listen the IGMP message communication between router and host to establish multicast group membership. Based on the group membership information, IP175DLF forwards IP multicast data to its membership which registered in group table. For hardware IGMP snooping timeout mechanism is provided by applying the hosts silently leave a specific multicast group. "Silently Leave" means that a host does not respond to query message when it want to leaves group. Except for hardware IGMP snooping, IP175DLF also support software IGMP snooping and IGMP snooping with CPU assistance. Software IGMP snooping imply that software must handle IP multicast traffic which include IGMP packet, IP multicast control packet and IP multicast data packet and then forward it to proper output port after processing done. For IGMP snooping with CPU assistance, it separate two parts: hardware supporting and software supporting. In hardware supporting, the switch directly forward IGMP packets and IP multicast control packets to CPU for further processing. Then software must process these packets and forward to proper output port. The external CPU also must maintain the table of multicast group. When IP multicast data packet is received by a port, the switch forward it according to this table.

IP175DLF supports not only IGMP snooping but also MLD snooping. MLD snooping does not support hardware MLD snooping. It only supports software MLD and MLD snooping with CPU assistance. For MLD snooping with CPU assistance, IP175DLF trap MLD packets to CPU for further processing and then forward these packets to proper ports. CPU shall update the table of multicast group according to MLD message. When IPv6 multicast packet is coming, it will be forwarded based on this table. For software MLD snooping IP175DLF traps MLD and IPv6 multicast packet to CPU. CPU shall process these packets and forward to proper ports.

### 3.12 Security Filtering

IP175DLF provides flexible security configuration to protect against attacks and filter suspicious traffics. These packets can be programmed to drop or forward to CPU for further processing. The IP175DLF provides packet filtering based on physical port, MAC address, logical port and layer 2-4 Multi-Field packet headers.

#### 3.12.1 Physical Port Filtering

A port can be disabled the forwarding and learning ability respectively. For instance a host connects to a physical port directly. The security rule is that everyone shall be authenticated by an authenticating server or administrator if he wants to access network. Administrator (or CPU) can disable forwarding and learning ability on a given port, if a host is in unauthorized state.

#### 3.12.2 MAC Address Filtering

The feature of MAC address filtering can be configured by two ways: specific MAC address filtering and unknown MAC address filtering. Specific MAC address filtering allows to drop packets with specific either source MAC address or destination. Specific MAC address filtering can also drop packet on per VLAN group. Configuring contexts of the specific MAC address filtering is through "Address Table Access Register". Unknown MAC address filtering only allows that packets with registered SMAC (source MAC address) can access network.

#### 3.12.3 Logical Port Filtering

IP175DLF support discard packets based on logical port. The logical port can define a particular port number or a range port number. If the source's logical port or the destination's logical port in the incoming

packet match any of the pre-defined logical ports, the incoming frame will be discarded.

### 3.12.4 Layer 2-4 Multi-Field Filtering

IP175DLF support discard packets based on a combination of layer 2-4 Multi-Field packet headers.

### 3.13 IEEE 802.1x

IP175DLF support IEEE 802.1x security. The EAPOL is used by authentication process. EAPOL is detected by checking destination MAC address defined in 01:80:C2:00:00:03 and then trap to CPU for further processing. Eventually, CPU determines whether the port configures in authorized state or not. CPU can also determine whether the requestor is qualified or not based on source MAC address. When the switch is a VLAN-aware switch, CPU can determine whether the port (or SMAC) is placed in the authorized state per VLAN.

### 3.14 Spanning Tree

In IP175DLF spanning tree operation separate into software implement and hardware implement. In software implement CPU must process BPDU packet and configure the state of each port. In hardware implement the switch trap BPDU to CPU. The following table describes how to configure the state of each port in IP175DLF.

| State      | Fwd BPDU packet to CPU | Fwd BPDU packet from CPU | Address learning | Fwd all packet normally | (Forward enable, Learning enable) <sup>8</sup> |
|------------|------------------------|--------------------------|------------------|-------------------------|--|
| Disable    | X (note 2)             | X (note 2)               | X                | X                       | (0,0)  |
| Blocking   | O                      | X (note 3)               | X                | X                       | (0,0)  |
| Listening  | O                      | O                        | X                | X                       | (0,0)  |
| Learning   | O                      | O                        | O                | X                       | (0,1)  |
| Forwarding | O                      | O                        | O                | O                       | (1,1)  |

**Note1:** O: enabled, X: disabled

**Note2:** CPU should not send packets to IP175DLF and should discard packets from IP175DLF.

**Note3:** CPU should not send packets to IP175DLF.

**Table 6 Configuring port state**

IP175DLF Support fast aging function for RSTP, User can configure the parameter from MII register 20.14[6:5] and 20.14[4:0].

IP175DLF support 4 multiple spanning tree VLAN table which contains the VLAN-dependent port state. MSTP allows users to map many VLANs to a spanning tree group, each with its own topology.

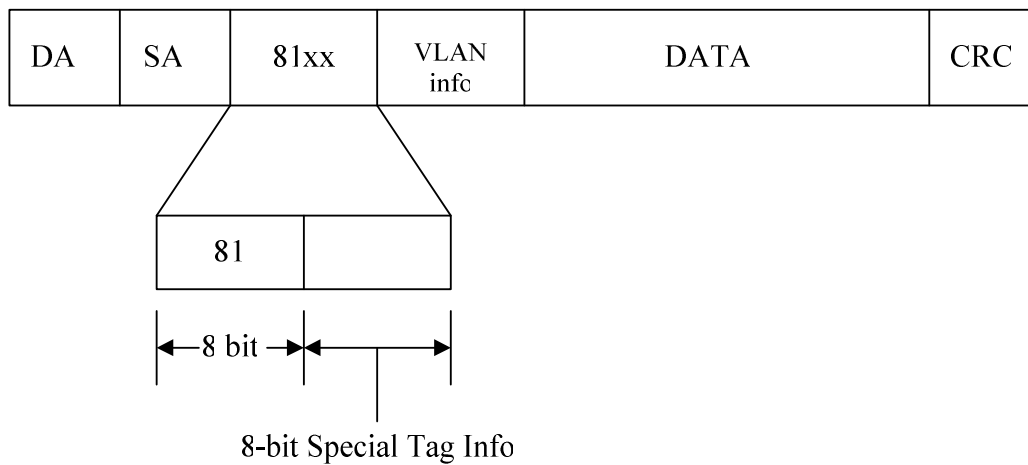
### 3.15 Special Tag

The purpose of special tag is:

- To allow a frame (IP175DLF to CPU) to carrier ingress port number and violation event.
- To allow a frame (CPU to switch) to indicate the output port mask and output queue number carrier in special tag header

The VLAN TPID is represented in two octets, the hexadecimal value 8100. The octets display from left to right, the left octet is 0x80 and the right octet is 0x00. Special tag information appears in the right octet whose value is not a zero.

<sup>8</sup> The forwarding and learning ability of each port are configured in MII register 20.6. For MSTP the forwarding and learning ability of each port are configured in MII register 24.0-3.



**Figure 3-4 Special tag format**

There are two formats of special tag, depending on the frame direction. The special tag format is defined as following.

**1. Special Tag for RX (switch to CPU)**

Frame direction is from switch to CPU. The special tag information consists of ingress port number and violation event. Ingress port number is where did the frame come from? Violation event is an event vector consisting of security violation, VLAN violation and miss address table.

Security violation: IP175DLF support unknown SMAC filtering and user can enable it from MII register 20.12. Unknown SMAC means source MAC address of the received frame is not found in address table. When this function is enabled, the received frames with unknown SMAC is marked “illegal SMAC”. IP175DLF discard the frame with illegal SMAC. A register bit is provided to allow this frame forward to CPU. Except to trap illegal frame to CPU, the IP175DLF also can mark this frame as security violation frame. Therefore CPU receive a frame whose security violation bit is marked, it will know source MAC address of this frame is not registered in address table.

VLAN violation: If a VLAN table searching results in a miss, this bit is set.

Miss address table: If an address table searching results in a miss, this bit is set.

| Special Tagged Information | Description   |
|----------------------------|---|
| Bit 7-3                    | Packet Information <ul style="list-style-type: none"> <li>- bit 4: Reserved</li> <li>- bit 3: Reserved</li> <li>- bit 2: Miss address table</li> <li>- bit 1: Security violation</li> <li>- bit 0: VLAN violation</li> </ul>                          |
| Bit 2-0                    | Ingress Port number <ul style="list-style-type: none"> <li>- 3'b000: Disabled</li> <li>- 3'b001: Port 0</li> <li>- 3'b010: Port 1</li> <li>- 3'b011: Port 2</li> <li>- 3'b100: Port 3</li> <li>- 3'b101: Port 4</li> <li>- Other: Reserved</li> </ul> |

## 2. Special Tag for TX (From CPU to switch)

Frame direction is from CPU to switch. This function provides for forwarding decision, priority assign and learning disable. These parameter embedded in special tag header can be set by CPU.

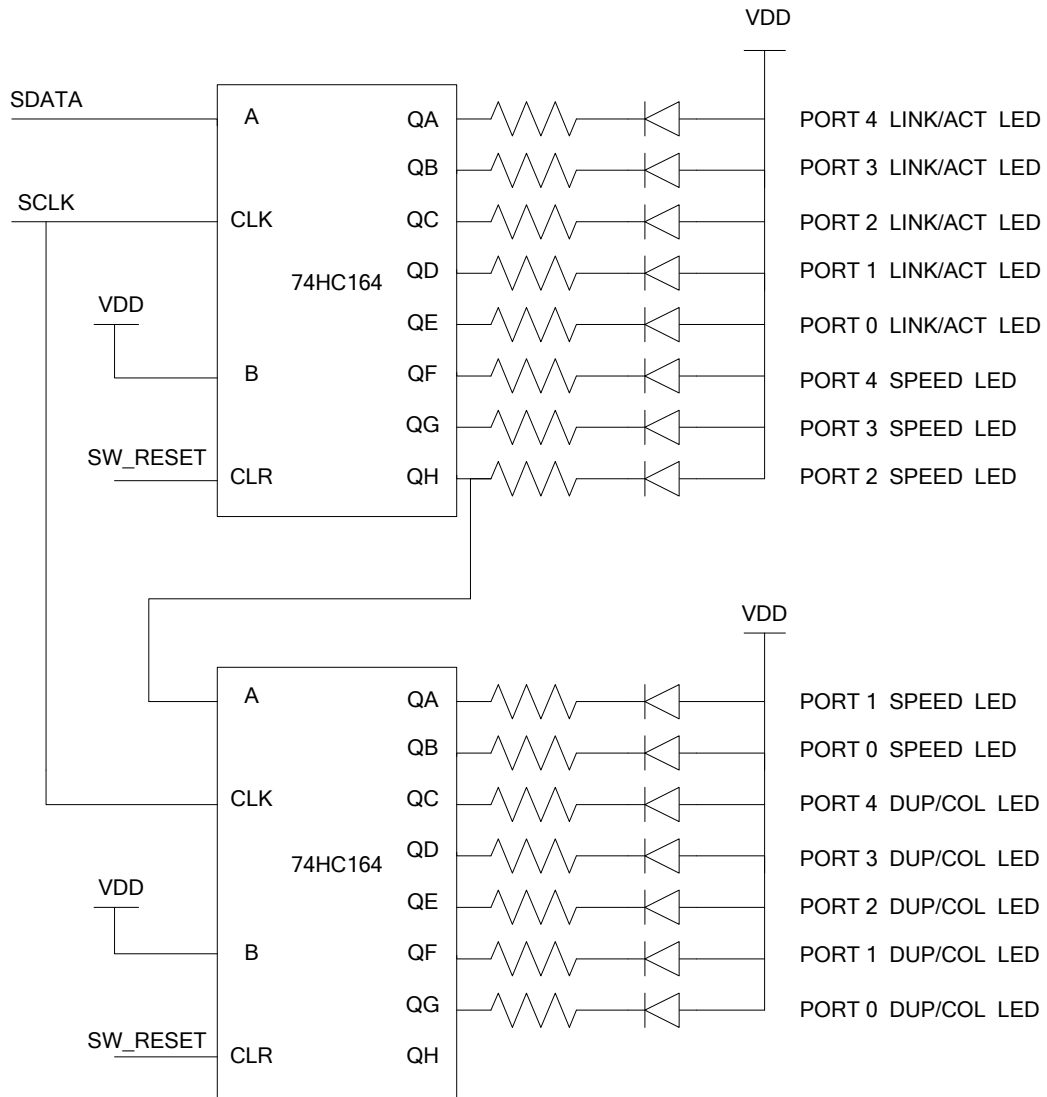
| Special Tagged Information | Description   |
|----------------------------|---|
| Bit 7                      | 0: Learn Enable<br>1: Learn Disable   |
| Bit 6-5                    | Priority Assignment<br>- 2'b00: Disabled<br>- 2'b01: Queue 1<br>- 2'b10: Queue 2<br>- 2'b11: Queue 3            |
| Bit 4-0                    | Output Port Mask<br>- bit 4: port 4<br>- bit 3: port 3<br>- bit 2: port 2<br>- bit 1: port 1<br>- bit 0: port 0 |

### 3.16 Serial Mode LED

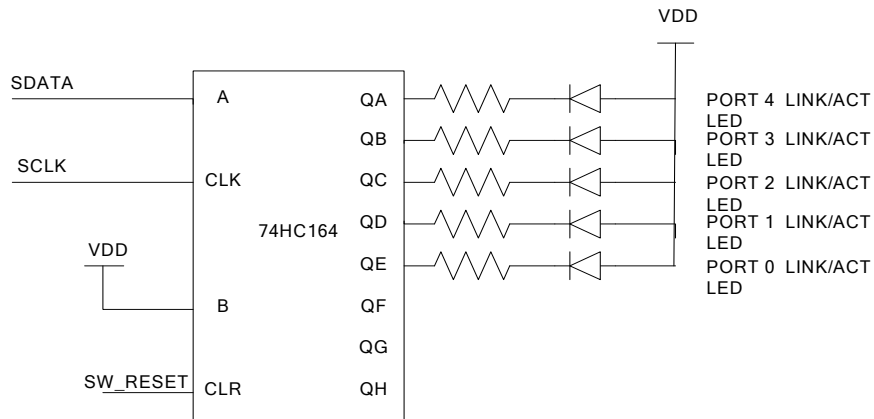
When MII/RMII2 is enabled, there are no enough pins for LED and IP175DLF sends out LED information through pin 111 (SCLK) and pin112 (SDATA). It is necessary to use TTL chip to decode and drive LED. The application circuit is shown below.

IP175DLF supports two types of serial led mode and can be setting by pin112 or MII register 20.24[2]. The default value is 0 (SERIAL\_LED\_MODE = 0) and can be setting to 1 by pull up pin112 (4.7K) or writing 1 to MII register 20.24[2].

(SERIAL\_LED\_MODE=0, IP175DLF supports link, speed, and duplex LED)



(SERIAL\_LED\_MODE= 1, IP175DLF supports link LED only.)



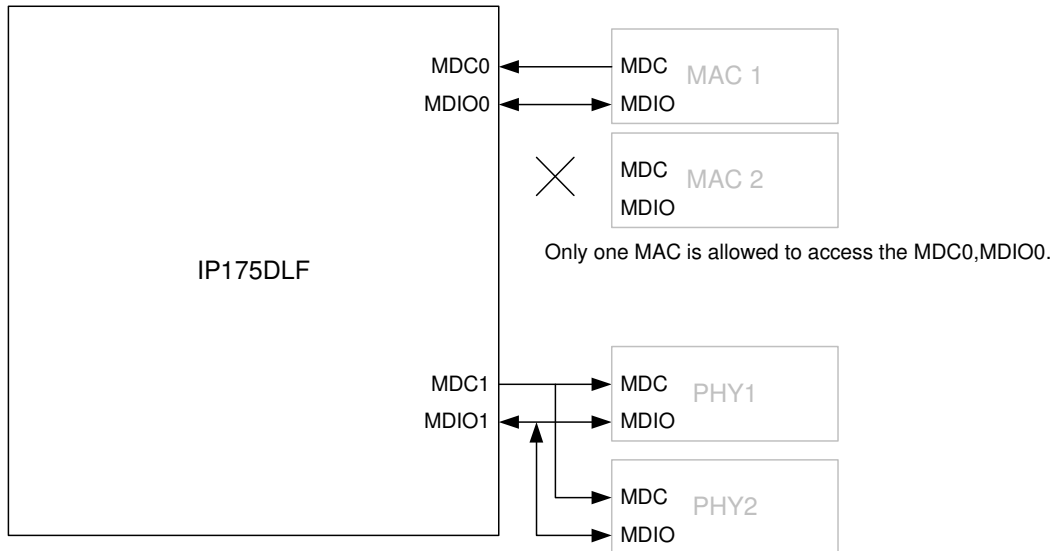
### 3.17 LED Blink Timing

| LED mode                         | Blinking speed                               |
|----------------------------------|--|
| Serial mode update period        | 22 ms (44ms/2)                               |
| Active led blink                 | On -> Off 44ms -> On 176ms -> Off 44ms ...   |
| Collision led blink              | Off -> On 176ms -> Off 44ms -> On 176ms ...  |
| Link quality fail blink          | On 2s -> Off 2s -> On 2s -> Off 2s ...       |
| Neon like LED(initial setup LED) | On 286ms -> Off 2s -> On 286ms -> Off 2s ... |





**The application of SMI**



All PHY can be accessed via the MDC1, MDIO1.

**3.19 Reset**

The IP175DLF supports three kinds of reset function.

**1. Hardware Reset:** Pin 93 RESETB should be asserted LOW at least for 5ms to reset IP175DLF.

The IP175DLF gets initial values from pins and EEPROM after reset

**2. Software Reset:** After Hardware Reset, user can write 16'h175D to PHY 20 Register 2 via SMI to reset IP175DLF. The IP175DLF resets all of PHY's and switch Engine, but IP175DLF does not load initial values from pins and EEPROM

**3. PHY Reset:** Please write "1" to bit 15 of MII register 0 to reset the PHY. The PHY address is from 0 to 4 for port 0~4 respectively.

**4 PHY Register**

**4.1 PHY ID Map**

| PHY ID | Description                 | Default | Note |
|--------|-----------------------------|---------|------|
| 0      | Port 0 PHY                  |         |      |
| 1      | Port 1 PHY                  |         |      |
| 2      | Port 2 PHY                  |         |      |
| 3      | Port 3 PHY                  |         |      |
| 4      | Port 4 PHY or MII1 PHY mode |         |      |
| 5      | MII0 PHY mode               |         |      |
| 6      | MII2 PHY mode               |         |      |
| 20~27  | Switch Registers            |         |      |

**4.2 PHY 0~4 Register Map**

| Register | Description | Default | Note |
|----------|-------------|---------|------|
|----------|-------------|---------|------|



|    |  |  |    |
|----|--|--|----|
| 0  | Control Register                               |  | X5 |
| 1  | Status Register                                |  | X5 |
| 2  | PHY Identifier 1 Register                      |  | X1 |
| 3  | PHY Identifier 2 Register                      |  | X1 |
| 4  | Auto-Negotiation Advertisement Register        |  | X5 |
| 5  | Auto-Negotiation Link Partner Ability Register |  | X5 |
| 6  | Auto-Negotiation Expansion Registers           |  | X5 |
| 16 | Special Control Register (APS)                 |  | X1 |
| 18 | Special Status Register                        |  | X5 |
| 22 | MDI-MDIX Control Register                      |  | X1 |

X1: 5 ports share the register

X5: Each port has its individual register

R/W = Read/Write, SC = Self-Clearing, RO = Read Only, LL = Latching Low, LH = Latching High.

### 4.3 MII Register 0 of PHY0~4

(Each PHY has its own MII register 0 with different PHY address)

| PHY                     | MI     | ROM | R/W       | Description  | Default |
|-------------------------|--------|-----|-----------|--|---------|
| <b>Control register</b> |        |     |           |  |         |
| 4~0                     | 0.15   | --  | RW/<br>SC | Reset<br>The PHY is reset if user write "1" to this bit. The reset period is around 2ms. User has to wait for at least 2ms to access IP175DLF.   | 0       |
| 4~0                     | 0.14   | --  | R/W       | Loop back<br>1 = Loop back mode<br>0 = normal operation<br>When this bit set, IP175DLF will be isolated from the network media, that is, the assertion of TXEN at the MII will not transmit data on the network. All MII transmission data will be returned to MII receive data path in response to the assertion of TXEN. Bit 0.12 is cleared automatically, if this bit is set. User has to program bit 0.12 again after loop back test. | 0       |
| 4~0                     | 0.13   | --  | RW        | Speed Selection<br>1 = 100Mbps<br>0 = 10Mbps<br>It is valid only if bit 0.12 is set to be 0.   | 1       |
| 4~0                     | 0.12   | --  | RW        | Auto-Negotiation Enable<br>1 = Auto-Negotiation Enable<br>0 = Auto-Negotiation Disable<br>MII register 4~0.22 Auto MDI-MDIX should be disabled if Auto-Negotiation is disabled.  | 1       |
| 4~0                     | 0.11   | --  | R/W       | Power Down<br>1: power down mode<br>0: normal operation  | 0       |
| 4~0                     | 0.10   | --  |           | Isolate<br>IP175DLF doesn't support this function.   | 0       |
| 4~0                     | 0.9    | --  | RW<br>SC  | Restart Auto- Negotiation<br>1 = re-starting Auto-Negotiation<br>0 = Auto-Negotiation re-start complete<br>Setting this bit to logic high will cause IP175DLF to restart an Auto-Negotiation cycle, but depending on the value of bit 0.12 (Auto-Negotiation Enable). If bit 0.12 is cleared then this bit has no effect, and it is Read Only. This bit is self-clearing after Auto-Negotiation process is completed.                      | 0       |
| 4~0                     | 0.8    | --  | R/W       | Duplex mode<br>1 = full duplex<br>0 = half duplex<br>It is valid only if bit 0.12 is set to be 0.  | 0       |
| 4~0                     | 0.7    | --  | R/W       | Collision test   | 0       |
| 4~0                     | 0[6:0] | --  | RO        | Reserved   | 0       |

#### 4.4 MII Register 1 of PHY0~4

(Each PHY has its own MII register 1 with different PHY address)

| PHY                    | MII     | ROM | R/W      | Description   | Default |
|------------------------|---------|-----|----------|---|---------|
| <b>Status register</b> |         |     |          |   |         |
| 4~0                    | 1.15    | --  | RO       | 100Base-T4 capable<br>1 = 100Base-T4 capable<br>0 = not 100Base-T4 capable<br>IP175DLF does not support 100Base-T4. This bit is fixed to be 0.  | 0       |
| 4~0                    | 1.14    | --  | RO       | 100Base-X full duplex Capable<br>1 = 100Base-X full duplex capable<br>0 = not 100Base-X full duplex capable   | 1       |
| 4~0                    | 1.13    | --  | RO       | 100Base-X half duplex Capable<br>1 = 100Base-X half duplex capable<br>0 = not 100Base-X half duplex capable   | 1       |
| 4~0                    | 1.12    | --  | RO       | 10Base-T full duplex Capable<br>1 = 10Base-T full duplex capable<br>0 = not 10Base-T full duplex capable  | 1       |
| 4~0                    | 1.11    | --  | RO       | 10Base-T half duplex Capable<br>1 = 10Base-T half duplex capable<br>0 = not 10Base-T half duplex capable  | 1       |
| 4~0                    | 1[10:7] | --  | RO       | Reserved  | 0       |
| 4~0                    | 1.6     | --  | RO       | MF preamble Suppression<br>1 = preamble may be suppressed<br>0 = preamble always required   | 1       |
| 4~0                    | 1.5     | --  | RO       | Auto-Negotiation Complete<br>1 = Auto-Negotiation complete<br>0 = Auto-Negotiation in progress<br>When read as logic 1, indicates that the Auto-Negotiation process has been completed, and the contents of register 4 and 5 are valid. When read as logic 0, indicates that the Auto-Negotiation process has not been completed, and the contents of register 4 and 5 are meaningless. If Auto-Negotiation is disabled (bit 0.12 set to logic 0), then this bit will always read as logic 0. | 0       |
| 4~0                    | 1.4     | --  | RO<br>LH | Remote fault<br>1 = remote fault detected<br>0 = not remote fault detected<br>When read as logic 1, indicates that IP175DLF has detected a remote fault condition. This bit is set until remote fault condition gone and before reading the contents of the register. This bit is cleared after IP175DLF reset.   | 0       |
| 4~0                    | 1.3     | --  | RO       | Auto-Negotiation Ability<br>1 = Auto-Negotiation capable<br>0 = not Auto-Negotiation capable<br>When read as logic 1, indicates that IP175DLF has the ability to perform Auto-Negotiation.  | 1       |



| PHY                    | MII | ROM | R/W      | Description  | Default |
|------------------------|-----|-----|----------|--|---------|
| <b>Status register</b> |     |     |          |  |         |
| 4~0                    | 1.2 | --  | RO<br>LL | Link Status<br>1 = Link Pass<br>0 = Link Fail<br>When read as logic 1, indicates that IP175DLF has determined a valid link has been established. When read as logic 0, indicates the link is not valid. This bit is cleared until a valid link has been established and before reading the contents of this registers.   | 0       |
| 4~0                    | 1.1 | --  |          | Jabber Detect<br>1 = jabber condition detected<br>0 = no jabber condition detected<br>When read as logic 1, indicates that IP175DLF has detected a jabber condition. This bit is always 0 for 100Mbps operation and is cleared after IP175DLF reset. When the duration of TXEN exceeds the jabber timer (21ms), the transmission and loop back functions will be disabled and the COL is active. After TXEN goes low for more than 500 ms, the transmitter will be re-enabled. | 0       |
| 4~0                    | 1.0 | --  | RO       | Extended capability<br>1 = Extended register capabilities<br>0 = No extended register capabilities<br>IP175DLF has extended register capabilities.   | 1       |

**4.5 MII Register 2 of PHY0~4 (5 PHYs share the MII register)**

| PHY                              | MII | ROM | R/W | Description  | Default  |
|----------------------------------|-----|-----|-----|--|----------|
| <b>PHY Identifier 1 register</b> |     |     |     |  |          |
| 4~0                              | 2   | --  | RO  | IP175DLF OUI (Organizationally Unique Identifier) ID, the msb is 3 <sup>rd</sup> bit of IP175DLF OUI ID, and the lsb is 18 <sup>th</sup> bit of IP175DLF OUI ID. IP175DLF OUI is 0090C3. | 16'h0243 |

**4.6 MII Register 3 of PHY0~4 (5 PHYs share the MII register)**

| PHY                              | MII      | ROM | R/W | Description  | Default |
|----------------------------------|----------|-----|-----|--|---------|
| <b>PHY Identifier 2 register</b> |          |     |     |  |         |
| 4~0                              | 3[15:10] | --  | RO  | PHY identifier<br>IP175DLF OUI ID, the msb is 19 <sup>th</sup> bit of IP175DLF OUI ID, and lsb is 24 <sup>th</sup> bit of IP175DLF OUI ID. | 6'h03   |
| 4~0                              | 3[9:4]   | --  | RO  | Manufacture's Model Number<br>IP175DLF model number  | 6'h18   |
| 4~0                              | 3[3:0]   | --  | RO  | Revision Number<br>IP175DLF revision number  | 0       |

#### 4.7 MII Register 4 of PHY0~4

(Each PHY has its own MII register 4 with different PHY address)

| PHY  | MII      | ROM | R/W | Description  | Default     |            |            |         |
|--|----------|-----|-----|--|-------------|------------|------------|---------|
| <b>Auto-Negotiation Advertisement register</b> |          |     |     |  |             |            |            |         |
| 4~0  | 4.15     | --  | RO  | Next Page<br>Not supported. This bit is fixed to be 0.   | 0           |            |            |         |
| 4~0  | 4.14     | --  | RO  | Reserved by IEEE, write as 0, ignore on read   | 0           |            |            |         |
| 4~0  | 4.13     | --  | R/W | Remote Fault<br>1: Advertises that this port has detected a remote fault.<br>0: There is no remote fault.        | 0           |            |            |         |
| 4~0  | 4[12:11] | --  | RO  | Reserved for future IEEE use, write as 0, ignore on read   | 0           |            |            |         |
| 4~0  | 4.10     | --  | RW  | Pause<br>1 = Advertises that this port has implemented pause function<br>0 = No pause function supported         | Set by X_EN |            |            |         |
| 4~0  | 4.9      | --  | RO  | 100BASE-T4 Not supported   | 0           |            |            |         |
| 4~0  | 4.8      | --  | R/W | 100BASE-TX full duplex<br>1 = 100BASE-TX full duplex is supported<br>0 = 100BASE-TX full duplex is not supported | *<br>-      |            |            |         |
|  |          |     |     | FORCE  |             | FORCE100   | FORCE_FULL | Default |
|  |          |     |     | 0  |             | Don't care | Don't care | 1       |
|  |          |     |     | 1  |             | 0          | 0          | 0       |
|  |          |     |     | 1  |             | 0          | 1          | 0       |
|  |          |     |     | 1  |             | 1          | 0          | 0       |
| 4~0  | 4.7      | --  | R/W | 100BASE-TX<br>1 = 100BASE-TX is supported<br>0 = 100BASE-TX is not supported                                     | *<br>-      |            |            |         |
|  |          |     |     | FORCE  |             | FORCE100   | FORCE FULL | Default |
|  |          |     |     | 0  |             | Don't care | Don't care | 1       |
|  |          |     |     | 1  |             | 0          | 0          | 0       |
|  |          |     |     | 1  |             | 0          | 1          | 0       |
|  |          |     |     | 1  |             | 1          | 0          | 1       |
| 4~0  | 4.6      | --  | R/W | 10BASE-T full duplex<br>1 = 10BASE-T full duplex is supported<br>0 = 10BASE-T full duplex is not supported       | *<br>-      |            |            |         |
|  |          |     |     | FORCE  |             | FORCE100   | FORCE FULL | Default |
|  |          |     |     | 0  |             | Don't care | Don't care | 1       |
|  |          |     |     | 1  |             | 0          | 0          | 0       |
|  |          |     |     | 1  |             | 0          | 1          | 1       |
|  |          |     |     | 1  |             | 1          | 0          | 0       |
| 4~0  | 4.5      | --  | R/W | 10BASE-T<br>1 = 10BASE-T is supported<br>0 = 10BASE-T is not supported   | <u>1</u>    |            |            |         |





| PHY | MII    | ROM | R/W | Description   | Default  |
|-----|--------|-----|-----|---|----------|
| 4~0 | 4[4:0] | --  | RO  | Selector Field<br>Use to identify the type of message being sent by Auto-Negotiation. | 5'b00001 |

#### 4.8 MII Register 5 of PHY0~4

(Each PHY has its own MII register 5 with different PHY address)

| PHY   | MII      | ROM | R/W | Description  | Default  |
|---|----------|-----|-----|--|----------|
| <b>Auto-Negotiation Link Partner Ability register</b> |          |     |     |  |          |
| 4~0   | 5.15     |     | RO  | Next Page<br>1 = Next Page ability is supported by link partner<br>0 = Next Page ability does not supported by link partner  | 0        |
| 4~0   | 5.14     |     | RO  | Acknowledge<br>1 = Link partner has received the ability data word<br>0 = Not acknowledge  | 0        |
| 4~0   | 5.13     |     | RO  | Remote Fault<br>1 = Link partner indicates a remote fault<br>0 = No remote fault indicate by link partner<br>If this bit is set to logic 1, then bit 1.4 (Remote fault) will set to logic 1.   | 0        |
| 4~0   | 5[12:11] | --  | RO  | Reserved by IEEE for future use, write as 0, read as 0.  | 0        |
| 4~0   | 5.10     | --  | RW  | Pause<br>1 = Link partner support IEEE802.3x<br>0 = Link partner does not support IEEE802.3x<br>When Nway enabled, this bit reflects link partner ability. (read only)<br>When Nway disabled, this bit can be set by SMI. (read/write)<br>When in 100FX, this bit is set by X_EN or SMI. | 0        |
| 4~0   | 5.9      | --  | RO  | 100BASE-T4<br>1 = Link partner support 100BASE-T4<br>0 = Link partner does not support 100BASE-T4  | 0        |
| 4~0   | 5.8      | --  | RO  | 100BASE-TX full duplex<br>1 = Link partner support 100BASE-TX full duplex<br>0 = Link partner does not support 100BASE-TX full duplex  | 0        |
| 4~0   | 5.7      | --  | RO  | 100BASE-TX<br>1 = Link partner support 100BASE-TX<br>0 = Link partner does not support 100BASE-TX<br>For 100FX mode, this bit is set. When Nway is disabled, this bit is set if register 0.13=1.   | 0        |
| 4~0   | 5.6      | --  | RO  | 10BASE-T full duplex<br>1 = Link partner support 10BASE-T full duplex<br>0 = Link partner does not support 10BASE-T full duplex  | 0        |
| 4~0   | 5.5      | --  | RO  | 10BASE-T<br>1 = Link partner support 10BASE-T<br>0 = Link partner does not support 10BASE-T<br>When Nway is disabled, this bit is set if register 0.13=0   | 0        |
| 4~0   | 5[4:0]   | --  | RO  | Selector Field<br>Protocol selector of the link partner  | 5'b00000 |

#### 4.9 MII Register 6 of PHY0~4

(Each PHY has its own MII register 6 with different PHY address)

| PHY  | MII     | ROM | R/W       | Description   | Default                |
|--|---------|-----|-----------|---|------------------------|
| <b>Auto-Negotiation Expansion register</b> |         |     |           |   |                        |
| 4~0  | 6[15:5] | --  | RO        | Reserved  | 0                      |
| 4~0  | 6.4     | --  | RO        | 1: a fault has been detected via parallel detection function.<br>0: a fault has not been detected via parallel detection function.  | 0                      |
| 4~0  | 6.3     | --  | RO        | 1= Link partner is next page able.<br>0= Link partner is not next page able.  | 0                      |
| 4~0  | 6.2     | --  | RO        | 1: IP175DLF next page able.<br>0: IP175DLF is not next page able.<br>This bit is fixed to be "0" in IP175DLF  | 0                      |
| 4~0  | 6.1     | --  | RO/<br>LH | 1: A new page has been received.<br>0: A new page has not been received.  | 0                      |
| 4~0  | 6.0     | --  | RO        | If Nway is enabled, this bit means:<br>1: Link partner is Auto-Negotiation able.<br>0: Link partner is not Auto-Negotiation able.<br>In 100FX or Nway disabled, this bit always =0. | 0<br>(Nway)<br>(100FX) |

#### 4.10 MII Register 16 of PHY0~4 (5 PHYs share the MII register)

| PHY                             | MII  | ROM | R/W | Description   | Default |
|---------------------------------|------|-----|-----|---|---------|
| <b>Special Control register</b> |      |     |     |   |         |
| 4~0                             | 16.7 | --  | RW  | Auto power saving mode<br>1 = Enable APS mode<br>0 = Disable APS mode | 1       |

#### 4.11 MII Register 18 of PHY0~4

(Each PHY has its own MII register 18 with different PHY address)

| PHY                            | MII   | ROM | R/W | Description                                       | Default |
|--------------------------------|-------|-----|-----|---|---------|
| <b>Special Status register</b> |       |     |     |   |         |
| 4~0                            | 18.11 | --  | RO  | Speed Mode<br>1 = 100 Mbps<br>0 = 10 Mbps         | 1       |
| 4~0                            | 18.10 | --  | RO  | Duplex Mode<br>1 = Full Duplex<br>0 = Half Duplex | 0       |

#### 4.12 MII Register 22 of PHY0~4 (5 PHYs share the MII register)

| PHY                              | MII  | ROM | R/W | Description  | Default |
|----------------------------------|------|-----|-----|--|---------|
| <b>MDI-MDIX Control register</b> |      |     |     |  |         |
| 4~0                              | 22.9 | --  | RW  | PHY4 Auto MDI-MDIX Enable<br>1 = Enable Auto MDI-MDIX<br>0 = Disable Auto MDI-MDIX<br>It should be disabled if MII register 4.0.12 Auto-Negotiation is disabled. | 1       |
| 4~0                              | 22.8 |     | RW  | PHY3 Auto MDI-MDIX Enable<br>1 = Enable Auto MDI-MDIX<br>0 = Disable Auto MDI-MDIX<br>It should be disabled if MII register 3.0.12 Auto-Negotiation is disabled. | 1       |
| 4~0                              | 22.7 |     | RW  | PHY2 Auto MDI-MDIX Enable<br>1 = Enable Auto MDI-MDIX<br>0 = Disable Auto MDI-MDIX<br>It should be disabled if MII register 2.0.12 Auto-Negotiation is disabled. | 1       |
| 4~0                              | 22.6 |     | RW  | PHY1 Auto MDI-MDIX Enable<br>1 = Enable Auto MDI-MDIX<br>0 = Disable Auto MDI-MDIX<br>It should be disabled if MII register 1.0.12 Auto-Negotiation is disabled. | 1       |
| 4~0                              | 22.5 |     | RW  | PHY0 Auto MDI-MDIX Enable<br>1 = Enable Auto MDI-MDIX<br>0 = Disable Auto MDI-MDIX<br>It should be disabled if MII register 0.0.12 Auto-Negotiation is disabled. | 1       |
| 4~0                              | 22.4 |     | RW  | PHY4 MDI-MDIX Selection (only available when 22.9 = 0)<br>1 = MDIX mode<br>0 = MDI mode  | 0       |
| 4~0                              | 22.3 |     | RW  | PHY3 MDI-MDIX Selection (only available when 22.8 = 0)<br>1 = MDIX mode<br>0 = MDI mode  | 0       |
| 4~0                              | 22.2 |     | RW  | PHY2 MDI-MDIX Selection (only available when 22.7 = 0)<br>1 = MDIX mode<br>0 = MDI mode  | 0       |
| 4~0                              | 22.1 |     | RW  | PHY1 MDI-MDIX Selection (only available when 22.6 = 0)<br>1 = MDIX mode<br>0 = MDI mode  | 0       |
| 4~0                              | 22.0 |     | RW  | PHY0 MDI-MDIX Selection (only available when 22.5 = 0)<br>1 = MDIX mode<br>0 = MDI mode  | 0       |

## 5 Switch Register

The IP175DLF can be configured via external EEPROM interface at boot time. During operation, IP175DLF registers are accessible via MDC0/MDIO0 interface.

### 5.1 Switch Register Map

| REG NUM | Description                |
|---------|----------------------------|
| C       | Chip identification        |
| 1       | Reserved                   |
| 2       | System Reset               |
| 3       |                            |
| 4       | Force Mode                 |
| 5       | Congestion Contro          |
| 6       | Port State                 |
| 7       | Illegal Frame Filter       |
| 8       | Packet Identifier          |
| 9       |                            |
| 1C      |                            |
| 11      |                            |
| 12      | Network Security           |
| 13      | Learning Control Register  |
| 14      | Ageing Time Parameter      |
| 15      |                            |
| 16      |                            |
| 17      |                            |
| 18      | Broadcast Storm Protection |
| 19      |                            |
| 20      |                            |
| 21      | Port Mirror                |
| 22      | Source Block Protection    |
| 23      | Reserved                   |
| 24      | LED Control Register       |
| 25      | Reserved                   |
| 26      |                            |
| 27      |                            |
| 28      | Reserved                   |
| 29      |                            |
| 30      |                            |
| 31      |                            |

PHY 20

| REG NUM | Description                    |
|---------|--------------------------------|
| C       | External MII Configuration     |
| 1       |                                |
| 2       |                                |
| 3       |                                |
| 4       | IGMP Control Register          |
| 5       |                                |
| 6       |                                |
| 7       | Rate Control                   |
| 8       |                                |
| 9       |                                |
| 1C      | Reserved                       |
| 11      |                                |
| 12      | Rate Control                   |
| 13      | Reserved                       |
| 14      | Address Table Access Register  |
| 15      |                                |
| 16      |                                |
| 17      |                                |
| 18      |                                |
| 19      | CPU Interrupt                  |
| 20      |                                |
| 21      | Miscellaneous Control Register |
| 22      |                                |
| 23      |                                |
| 24      | CRC Counter                    |
| 25      |                                |
| 26      | Reserved                       |
| 27      |                                |
| 28      |                                |
| 29      |                                |
| 30      |                                |
| 31      |                                |

PHY 21

| REG NUM | Description           |
|---------|-----------------------|
| C       | VLAN Control Register |
| 1       |                       |
| 2       |                       |
| 3       |                       |
| 4       |                       |
| 5       |                       |
| 6       |                       |
| 7       |                       |
| 8       |                       |
| 9       |                       |
| 10      |                       |
| 11      | VLAN Table            |
| 12      |                       |
| 13      |                       |
| 14      |                       |
| 15      |                       |
| 16      |                       |
| 17      |                       |
| 18      |                       |
| 19      |                       |
| 20      |                       |
| 21      |                       |
| 22      |                       |
| 23      |                       |
| 24      |                       |
| 25      |                       |
| 26      |                       |
| 27      |                       |
| 28      |                       |
| 29      |                       |
| 30      | Reserved              |
| 31      |                       |

PHY 22

| REG NUM | Description |
|---------|-------------|
| C       |             |
| 1       |             |
| 2       |             |
| 3       |             |
| 4       |             |
| 5       |             |
| 6       |             |
| 7       |             |
| 8       |             |
| 9       |             |
| 10      |             |
| 11      | VLAN Table  |
| 12      |             |
| 13      |             |
| 14      |             |
| 15      |             |
| 16      |             |
| 17      |             |
| 18      |             |
| 19      |             |
| 20      |             |
| 21      |             |
| 22      |             |
| 23      |             |
| 24      |             |
| 25      |             |
| 26      |             |
| 27      |             |
| 28      |             |
| 29      |             |
| 30      |             |
| 31      |             |

PHY 23

| REG NUM | Description |
|---------|-------------|
| 0       | VLAN Table  |
| 1       |             |
| 2       |             |
| 3       |             |
| 4       | Reserved    |
| 5       |             |
| 6       |             |
| 7       |             |
| 8       |             |
| 9       |             |
| 10      |             |
| 11      |             |
| 12      |             |
| 13      |             |
| 14      |             |
| 15      |             |
| 16      |             |
| 17      |             |
| 18      |             |
| 19      |             |
| 20      |             |
| 21      |             |
| 22      |             |
| 23      |             |
| 24      |             |
| 25      |             |
| 26      |             |
| 27      |             |
| 28      |             |
| 29      |             |
| 30      |             |
| 31      |             |

PHY 24

| REG NUM | Description             |
|---------|-------------------------|
| 0       | Priority Classification |
| 1       |                         |
| 2       |                         |
| 3       |                         |
| 4       |                         |
| 5       |                         |
| 6       |                         |
| 7       |                         |
| 8       |                         |
| 9       |                         |
| 10      |                         |
| 11      |                         |
| 12      |                         |
| 13      |                         |
| 14      |                         |
| 15      |                         |
| 16      |                         |
| 17      |                         |
| 18      |                         |
| 19      |                         |
| 20      |                         |
| 21      |                         |
| 22      | Queue Scheduling        |
| 23      | Reserved                |
| 24      |                         |
| 25      |                         |
| 26      |                         |
| 27      |                         |
| 28      |                         |
| 29      |                         |
| 30      |                         |
| 31      |                         |

PHY 25

| REG NUM | Description |
|---------|-------------|
| 0       |             |
| 1       |             |
| 2       |             |
| 3       |             |
| 4       |             |
| 5       |             |
| 6       |             |
| 7       |             |
| 8       |             |
| 9       |             |
| 10      |             |
| 11      |             |
| 12      | MF          |
| 13      |             |
| 14      |             |
| 15      |             |
| 16      |             |
| 17      |             |
| 18      |             |
| 19      |             |
| 20      |             |
| 21      |             |
| 22      |             |
| 23      |             |
| 24      | Reserved    |
| 25      |             |
| 26      |             |
| 27      |             |
| 28      |             |
| 29      |             |
| 30      |             |
| 31      |             |

PHY 26



## 5.2 Switch Register EEPROM Map

|       | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|---|---|---|---|---|---|---|---|
| 0~1   | Load eeprom (55AA)                          |   |   |   |   |   |   |   |
| 2     | MII force mode                              |   |   |   |   |   |   |   |
| 3     | Congestion control                          |   |   |   |   |   |   |   |
| 4~5   | Port state                                  |   |   |   |   |   |   |   |
| 6     | Illegal frame filter                        |   |   |   |   |   |   |   |
| 7~9   | Reserved address                            |   |   |   |   |   |   |   |
| 10~12 | Miscellaneous special packet identification |   |   |   |   |   |   |   |
| 13~14 | Network security                            |   |   |   |   |   |   |   |
| 15~16 | Learning control                            |   |   |   |   |   |   |   |
| 17~19 | Aging time parameter                        |   |   |   |   |   |   |   |
| 20~27 | Broadcast storm protection                  |   |   |   |   |   |   |   |
| 28~30 | Port mirror                                 |   |   |   |   |   |   |   |
| 31    | Source block protection                     |   |   |   |   |   |   |   |
| 32    | Reserved                                    |   |   |   |   |   |   |   |
| 33    | LED control                                 |   |   |   |   |   |   |   |
| 34~39 | Reserved                                    |   |   |   |   |   |   |   |
| 40~45 | External MII setting                        |   |   |   |   |   |   |   |
| 46    | IGMP control                                |   |   |   |   |   |   |   |
| 47~48 | Router port timeout                         |   |   |   |   |   |   |   |
| 49    | IGMP group timeout                          |   |   |   |   |   |   |   |
| 50~51 | Miscellaneous control                       |   |   |   |   |   |   |   |
| 52~53 | Reserved                                    |   |   |   |   |   |   |   |

|         | 7                        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------------------------|---|---|---|---|---|---|---|
| 54      | Miscellaneous control    |   |   |   |   |   |   |   |
| 55~56   | VLAN classification      |   |   |   |   |   |   |   |
| 57~58   | VLAN ingress rule        |   |   |   |   |   |   |   |
| 59~60   | VLAN egress rule         |   |   |   |   |   |   |   |
| 61~74   | Default VLAN information |   |   |   |   |   |   |   |
| 75~82   | VLAN control             |   |   |   |   |   |   |   |
| 83~114  | VLAN identifier          |   |   |   |   |   |   |   |
| 115~130 | VLAN member              |   |   |   |   |   |   |   |
| 131~146 | Add tag control          |   |   |   |   |   |   |   |
| 147~162 | Remove tag control       |   |   |   |   |   |   |   |
| 163~178 | VLAN miscellaneous       |   |   |   |   |   |   |   |
| 179~186 | Spanning tree table      |   |   |   |   |   |   |   |
| 187~188 | Priority base control    |   |   |   |   |   |   |   |
| 189~190 | Port priority map        |   |   |   |   |   |   |   |
| 191~192 | VLAN priority            |   |   |   |   |   |   |   |
| 193~208 | TOS/DSCP priority map    |   |   |   |   |   |   |   |
| 209~228 | TCP/UDP port priority    |   |   |   |   |   |   |   |
| 229~232 | Queue scheduling control |   |   |   |   |   |   |   |

### 5.3 Switch Control Register

R/W = Read/Write, SC = Self-Clearing, RO = Read Only

#### 5.3.1 Chip Identification

| PHY | MII     | ROM | R/W | Description                | Default      |
|-----|---------|-----|-----|----------------------------|--------------|
| 20  | 0[15:0] | --  | RO  | PART_NUM<br>Part ID number | 16'h<br>175D |

#### 5.3.2 Software Reset Register

| PHY | MII     | ROM | R/W | Description  | Default |
|-----|---------|-----|-----|--|---------|
| 20  | 2[15:0] | --  | R/W | SOFT_RESET[15:0]<br>Software reset register<br>IP175DLF is reset if uses write "175D" to this register. It is self-cleared. The reset period is around 2ms. User has to wait for at least 2 ms to access IP175DLF.<br><br>When read this register, it shows the internal status of IP175DLF. | 16'h00  |
|     | 3[1:0]  | --  | R/W | TABLE_LOCK[1:0]<br>Lock content of table.<br>Bit[1]: Multi-Field table<br>Bit[0]: Address table  | 2'b00   |

5.3.3 MII Force Mode

| PHY | MII  | ROM  | R/W | Description   | Default |           |            |
|-----|------|------|-----|---|---------|-----------|------------|
| 20  | 4.15 | 2[7] | R/W | MAC5_FORCE_100<br>1: force MAC5 to be 100M<br>0: force MAC5 to be 10M                 | *       |           |            |
|     |      |      |     | Default Value   |         |           |            |
|     |      |      |     | P4EXT=0   |         | P4EXT=1   |            |
|     |      |      |     | 0   |         | MII2_EN=1 | MII2_EN=0  |
|     |      |      |     | 0   |         | 0         | Pin103 (0) |
| 20  | 4.14 | 2[6] | R/W | MAC4_FORCE_100<br>1: force MAC4 to be 100M<br>0: force MAC4 to be 10M                 | *       |           |            |
|     |      |      |     | Default Value   |         |           |            |
|     |      |      |     | P4EXT=0   |         | P4EXT=1   |            |
|     |      |      |     | 0   |         | MII2_EN=1 | MII2_EN=0  |
|     |      |      |     | 0   |         | 0         | Pin104 (0) |
| 20  | 4.13 | 2[5] | R/W | MAC5_FORCE_FULL<br>1: force MAC5 to be full duplex<br>0: force MAC5 to be half duplex | *       |           |            |
|     |      |      |     | Default Value   |         |           |            |
|     |      |      |     | P4EXT=0   |         | P4EXT=1   |            |
|     |      |      |     | 0   |         | MII2_EN=1 | MII2_EN=0  |
|     |      |      |     | 0   |         | 0         | Pin108 (0) |
| 20  | 4.12 | 2[4] | R/W | MAC4_FORCE_FULL<br>1: force MAC4 to be full duplex<br>0: force MAC4 to be half duplex | *       |           |            |
|     |      |      |     | Default Value   |         |           |            |
|     |      |      |     | TEST2=0   |         | TEST2=1   |            |
|     |      |      |     | P4EXT=0   |         | P4EXT=1   | 0          |
|     |      |      |     | 0   |         | MII2_EN=1 | MII2_EN=0  |
|     |      |      |     | 0   |         | 0         | Pin109(0)  |

5.3.4 Congestion Control Register

| PHY | MII     | ROM  | R/W | Description  | Default |
|-----|---------|------|-----|--|---------|
| 20  | 5[15:9] |      |     | RESERVED   |         |
|     | 5[8]    | 2[0] | R/W | CONT_PAUSE<br>To continuously send pause packet<br>1:enable<br>0:disable                     | 1'b0    |
|     | 5[7]    | 3[7] | R/W | MOD_CARRIER_ALGORITHM<br>Modified carrier based collision algorithm<br>1:enable<br>0:disable | 1'b0    |
|     | 5[6]    | 3[6] | R/W | INPUT_FILTER<br>1: enable<br>0: disable  | 1'b0    |
|     | 5[5]    | 3[5] | R/W | DROP16<br>Drop input packet after 16 times collision in succession.                          | 1'b0    |

|      |                 |     |   |      |                    |   |
|------|-----------------|-----|---|------|--------------------|---|
| 5[4] | 3[4]            | R/W | MODBCK<br>Modified backoff collision algorithm  | 1'b1 |                    |   |
| 5[3] | 3[3]            | R/W | BP_KIND<br>Backpressure Kind<br>0: carrier based<br>1: collision based  | 1'b0 |                    |   |
| 5[2] | 3[2]            | R/W | BK_EN<br>Backpressure enable<br>1: enable (default), 0: disable   | *    |                    |   |
|      |                 |     | Default Value   |      |                    |   |
|      |                 |     | TEST2=0   |      | TEST2=1            |   |
|      |                 |     | Pin113 MII2_EN=1  |      | Pin113 MII2_EN=0   | 1 |
|      |                 |     | 1   |      | Pin100 X_EN (1)    |   |
| 5[1] | 3[1]            | R/W | X_EN<br>IEEE 802.3x flow control enable (5 ports share the register)<br>1: enable (default), 0:disable                        | *    |                    |   |
|      |                 |     | If modify this register, a software reset (MII register 20.2) must be generated to notify PHY for flow control status change. |      |                    |   |
|      |                 |     | Default Value   |      |                    |   |
|      |                 |     | TEST2=0   |      | TEST2=1            |   |
|      |                 |     | Pin113 MII2_EN=1  |      | Pin113 MII2_EN=0   | 1 |
| 1    | Pin100 X_EN (1) |     |   |      |                    |   |
| 5[0] | 3[0]            | R/W | MAC_X_EN<br>Flow control enable of MII0-2<br>1: enable (default)<br>0: disable  | *    |                    |   |
|      |                 |     | Default Value   |      |                    |   |
|      |                 |     | TEST2=0   |      | TEST2=1            |   |
|      |                 |     | Pin74 P4EXT=1   |      | Pin74 P4EXT=0      | 0 |
|      |                 |     | 1   |      | Pin67 MAC_X_EN (1) |   |

### 5.3.5 Port State

| PHY | MII     | ROM    | R/W | Description  | Default |   |
|-----|---------|--------|-----|--|---------|---|
| 20  | 6[13:8] | 4[5:0] | R/W | FORWARD_EN[5:0]<br>Frame forwarding capability enable for each port      | 6'h3F   |   |
|     |         |        |     | bit 5  |         | 1: enable frame forwarding capability of port 5<br>0: disable frame forwarding capability of port 5 |
|     |         |        |     | bit 4  |         | 1: enable frame forwarding capability of port 4<br>0: disable frame forwarding capability of port 4 |
|     |         |        |     | bit 3  |         | 1: enable frame forwarding capability of port 3<br>0: disable frame forwarding capability of port 3 |
|     |         |        |     | bit 2  |         | 1: enable frame forwarding capability of port 2<br>0: disable frame forwarding capability of port 2 |
|     |         |        |     | bit 1  |         | 1: enable frame forwarding capability of port 1<br>0: disable frame forwarding capability of port 1 |
|     |         |        |     | bit 0  |         | 1: enable frame forwarding capability of port 0<br>0: disable frame forwarding capability of port 0 |
|     | 6[5:0]  | 5[5:0] | R/W | LEARNING_EN[5:0]<br>MAC address Learning capability enable for each port | 6'h3F   |   |
|     |         |        |     | bit 5  |         | 1: enable address learning capability of port 5<br>0: disable address learning capability of port 5 |
|     |         |        |     | bit 4  |         | 1: enable address learning capability of port 4<br>0: disable address learning capability of port 4 |
|     |         |        |     | bit 3  |         | 1: enable address learning capability of port 3<br>0: disable address learning capability of port 3 |
|     |         |        |     | bit 2  |         | 1: enable address learning capability of port 2<br>0: disable address learning capability of port 2 |
|     |         |        |     | bit 1  |         | 1: enable address learning capability of port 1<br>0: disable address learning capability of port 1 |
|     |         |        |     | bit 0  |         | 1: enable address learning capability of port 0<br>0: disable address learning capability of port 0 |

### 5.3.6 Illegal Frame Filter

| PHY | MII     | ROM    | R/W | Description  | Default |  |       |
|-----|---------|--------|-----|--|---------|--|-------|
| 20  | 7[15:5] |        |     | RESERVED   |         |  |       |
|     | 7[4:3]  | 6[4:3] | R/W | LONG_FRM[1:0]<br>Max forwarded packet length<br>00: 1536 bytes (default)<br>01: 1552 bytes<br>10: 1792 bytes<br>11: reserved | *       |  |       |
|     |         |        |     | Default Value  |         |  |       |
|     |         |        |     | TEST2=0  |         | TEST2=1                                |       |
|     |         |        |     | P4EXT=1  |         | P4EXT=0                                | 2'b00 |
|     |         |        |     | 2'b00  |         | Pin 066(2'b00)<br>0: 2'b00<br>1: 2'b10 |       |

| PHY | MII  | ROM  | R/W | Description  | Default |
|-----|------|------|-----|--|---------|
|     | 7[2] | 6[2] | R/W | MC_SMC<br>Filter Frame with multicast source MAC address             | 1'b0    |
|     | 7[1] | 6[1] | R/W | NULL_MAC<br>Filter Frame with null source or destination MAC address | 1'b0    |
|     | 7[0] | 6[0] | R/W | CRC_ERROR<br>Filter CRC Frame  | 1'b1    |

### 5.3.7 Special Packet Identification

#### 5.3.7.1 Reserved Address 01-80-C2-00-00-00 to 01-80-C2-00-00-1F

| PHY     | MII                                    | ROM    | R/W | Description   | Default |         |       |  |   |
|---------|--|--------|-----|---|---------|---------|-------|--|---|
| 20      | 8[15:14]                               | 7[7:6] | R/W | TRAP_RSVD_ADDR1[1:0]<br>Reserved address range 1<br>Reserved MAC address is from<br>01:80:C2:00:00:11 to 01:80:C2:00:00:1F<br><br>00: forward (default)<br>01: forward to CPU<br>10: discard<br>11: reserved  | 2'b00   |         |       |  |   |
|         | 8[13:12]                               | 7[5:4] | R/W | TRAP_ABM[1:0]<br>All Bridges Multicast address defined by IEEE 802.1D<br>Reserved MAC address is 01:80:C2:00:00:10<br><br>00: forward (default)<br>01: forward to CPU<br>10: discard<br>11: reserved  | 2'b00   |         |       |  |   |
|         | 8[11:10]                               | 7[3:2] | R/W | TRAP_RSVD_ADDR0[1:0]<br>Reserved address range 0<br>Reserved MAC address is from<br>01:80:C2:00:00:04 to 01:80:C2:00:00:0D, 01:80:C2:00:00:0F<br><br>00: forward (default)<br>01: forward to CPU<br>10: discard<br>11: reserved<br><br>Default Value<br><table border="1" data-bbox="561 1585 1283 1715"> <tr> <td>P4EXT=1</td> <td>P4EXT=0</td> </tr> <tr> <td>2'b00</td> <td>Pin_069(2'b00)<br/>0: 2'b00<br/>1: 2'b10</td> </tr> </table> | P4EXT=1 | P4EXT=0 | 2'b00 | Pin_069(2'b00)<br>0: 2'b00<br>1: 2'b10 | * |
| P4EXT=1 | P4EXT=0                                |        |     |   |         |         |       |  |   |
| 2'b00   | Pin_069(2'b00)<br>0: 2'b00<br>1: 2'b10 |        |     |   |         |         |       |  |   |

| PHY | MII    | ROM    | R/W | Description  | Default |
|-----|--------|--------|-----|--|---------|
|     | 8[9:8] | 7[1:0] | R/W | TRAP_LLDP[1:0]<br>Link Layer Discovery Protocol<br>Reserved MAC address is 01:80:C2:00:00:0E<br>LLDP Data Units (LLDPDUs) encoded with an Ethertype value of 0x88CC.<br><br>00: forward (default)<br>01: forward to CPU<br>10: discard<br>11: reserved<br><br>Default Value<br>P4EXT=1                      P4EXT=0<br>2'b00                              Pin_069(2'b00)<br>0: 2'b00<br>1: 2'b10 | *       |
| 20  | 8[7:6] | 8[7:6] | R/W | TRAP_802P1X[1:0]<br>IEEE 802.1X Port-Based Network Access Control<br>Reserved MAC address is 01:80:C2:00:00:03<br><br>00: forward (default)<br>01: forward to CPU<br>10: discard<br>11: reserved<br><br>Default Value<br>P4EXT=1                      P4EXT=0<br>2'b00                              Pin_069(2'b00)<br>0: 2'b00<br>1: 2'b10   | *       |
|     | 8[5:4] | 8[5:4] | R/W | TRAP_SP[1:0]<br>IEEE 802 standard protocol – Slow Protocols<br>Reserved MAC address is 01:80:C2:00:00:02<br><br>00: forward (default)<br>01: forward to CPU<br>10: discard<br>11: reserved<br><br>Default Value<br>P4EXT=1                      P4EXT=0<br>2'b00                              Pin_069(2'b00)<br>0: 2'b00<br>1: 2'b10   | *       |
|     | 8[3]   |        |     | RESERVED   |         |
|     | 8[2]   | 8[2]   | R/W | TRAP_PAUSE<br>Point-to-Point Pause function<br>Reserved MAC address is 01:80:C2:00:00:01<br><br>1: forward<br>0: discard (default)   | 1'b0    |

| PHY | MII    | ROM    | R/W | Description  | Default |
|-----|--------|--------|-----|--|---------|
|     | 8[1:0] | 8[1:0] | R/W | TRAP_BPDU[1:0]<br>Standard Spanning Tree Protocol<br>Reserved MAC address is 01:80:C2:00:00:00<br><br>00: forward (default)<br>01: forward to CPU<br>10: discard<br>11: reserved<br><br>Default Value<br><br>P4EXT=1                      P4EXT=0<br><br>2'b00                              Pin_087(2'b00)<br>0: 2'b00<br>1: 2'b10 | *       |

5.3.8



5.3.8.1 Reserved Address 01-80-C2-00-00-20 to 01-80-C2-00-00-FF

| PHY | MII     | ROM    | R/W | Description  | Default |
|-----|---------|--------|-----|--|---------|
| 20  | 9[15:8] |        |     | RESERVED   |         |
|     | 9[7:6]  | 9[7:6] | R/W | TRAP_RSVD_ADDR3[1:0]<br>Reserved address range 3<br>Reserved MAC address is from<br>01:80:C2:00:00:30 to 01:80:C2:00:00:FF<br><br>00: forward (default)<br>01: forward to CPU<br>10: discard<br>11: reserved | 2'b00   |
|     | 9[5:4]  | 9[5:4] | R/W | TRAP_RSVD_ADDR2[1:0]<br>Reserved address range 2<br>Reserved MAC address is from<br>01:80:C2:00:00:22 to 01:80:C2:00:00:2F<br><br>00: forward (default)<br>01: forward to CPU<br>10: discard<br>11: reserved | 2'b00   |
|     | 9[3:2]  | 9[3:2] | R/W | TRAP_GVRP[1:0]<br>GVRP Address: 01-80-C2-00-00-21<br>00: forward (default)<br>01: forward to CPU<br>10: discard<br>11: reserved  | 2'b00   |
|     | 9[1:0]  | 9[1:0] | R/W | TRAP_GMRP[1:0]<br>GMRP Address: 01-80-C2-00-00-20<br>00: forward (default)<br>01: forward to CPU<br>10: discard<br>11: reserved  | 2'b00   |

5.3.8.2 Miscellaneous Special Packet Identification

| PHY | MII       | ROM     | R/W | Description   | Default |
|-----|-----------|---------|-----|---|---------|
| 20  | 10[15:14] | 10[7:6] | R/W | TRAP_ICMP<br>Internet Control Message Protocol<br>ICMPv4: TYPE=0x0800 and Protocol=1<br>ICMPv6: TYPE=0x86DD and Protocol=58<br><br>00: forward (default)<br>01: forward to CPU<br>10: discard<br>11: reserved | 2'b00   |

| PHY | MII       | ROM     | R/W | Description   | Default |
|-----|-----------|---------|-----|---|---------|
|     | 10[13:12] | 10[5:4] | R/W | TRAP_MLD_CTRL<br>MLD Control Packet<br>DMAC=33-33-XX-XX-XX-XX<br>EtherType=0x86DD<br>Version=6<br>Next Header=58<br><br>00: forward (default)<br>01: forward to CPU<br>10: discard<br>11: reserved  | 2'b00   |
|     | 10[11:10] | 10[3:2] | R/W | TRAP_MLD<br>Multicast Listener Discovery<br>DMAC=33-33-XX-XX-XX-XX<br>EtherType=0x86DD<br>Version=6<br><br>00: forward (default)<br>01: forward to CPU<br>10: discard<br>11: reserved   | 2'b00   |
|     | 10[9:8]   | 10[1:0] | R/W | TRAP_IPM_DATA<br>IP Multicast Data Packet<br>DMAC=01-00-5E-XX-XX-XX<br>EtherType=0x0800<br>Version=4<br>DIP=224.0.1.0~239.225.225.225<br>Protocol is not IGMP<br><br>00: forward (default)<br>01: forward to CPU<br>10: discard<br>11: reserved | 2'b00   |
|     | 10[7:6]   | 11[7:6] | R/W | TRAP_IPM_CTRL<br>IP Multicast Control Packet<br>DMAC=01-00-5E-XX-XX-XX<br>EtherType=0x0800<br>Version=4<br>DIP=224.0.0.x<br>Protocol is not IGMP<br><br>00: forward (default)<br>01: forward to CPU<br>10: discard<br>11: reserved              | 2'b00   |

| PHY | MII     | ROM     | R/W | Description  | Default |
|-----|---------|---------|-----|--|---------|
|     | 10[5:4] | 11[5:4] | R/W | TRAP_IGMP<br>Internet Group Management Protocol<br>DMAC=01-00-5E-XX-XX-XX<br>EtherType=0x0800<br>Version=4<br>Protocol=2(IGMP)<br><br>00: forward (default)<br>01: forward to CPU<br>10: discard<br>11: reserved                   | 2'b00   |
|     | 10[3:2] | 11[3:2] | R/W | TRAP_RARP[1:0]<br>Reverse Address Resolution Protocol<br>The destination MAC address is FF: FF: FF: FF: FF: FF<br>and Ether-Type field is 0x8035<br><br>00: forward (default)<br>01: forward to CPU<br>10: discard<br>11: reserved | 2'b00   |
|     | 10[1:0] | 11[1:0] | R/W | TRAP_ARP[1:0]<br>Address Resolution Protocol<br>The destination MAC address is FF: FF: FF: FF: FF: FF<br>and Ether-Type field is 0x0806<br><br>00: forward (default)<br>01: forward to CPU<br>10: discard<br>11: reserved          | 2'b00   |

| PHY | MII      | ROM     | R/W | Description  | Default |
|-----|----------|---------|-----|--|---------|
| 20  | 11[15:4] |         |     | RESERVED   |         |
|     | 11[3:2]  | 12[3:2] | R/W | TRAP_BOOTP<br>Bootstrap Protocol<br>Port Number=16'd67 or 16'd68<br><br>00: forward (default)<br>01: forward to CPU<br>10: discard<br>11: reserved                   | 2'b00   |
|     | 11[1:0]  | 12[1:0] | R/W | TRAP_PPPOE<br>Point-to-Point Protocol over Ethernet<br>Ether-Type=0x8863 or 0x8864<br><br>00: forward (default)<br>01: forward to CPU<br>10: discard<br>11: reserved | 2'b00   |

### 5.3.9 Network Security

| PHY | MII      | ROM     | R/W | Description   | Default       |
|-----|----------|---------|-----|---|---------------|
| 20  | 12[14]   | 13[6]   | R/W | ILL_SMAC_2CPU<br>Illegal SMAC to CPU<br>0: If frame with illegal SMAC, discard it.<br>1: If frame with illegal SMAC, forward it to CPU.   | 1'b0          |
|     | 12[13:8] | 13[5:0] | R/W | ILL_SMAC_PROT[5:0]<br>Illegal source MAC address protection<br>0: disable<br>1: enable.<br>Bit[0]: port 0<br>Bit[1]: port 1<br>Bit[2]: port 2<br>Bit[3]: port 3<br>Bit[4]: port 4<br>Bit[5]: port 5   | 6'h00         |
|     | 12[7:6]  |         |     | RESERVED  |               |
|     | 12[5:0]  | 14[5:0] | R/W | CHK_PORT[5:0]<br>The frame is examined based on the combination of SMAC and ingress port number in address table.<br>Bit[0]: port 0<br>Bit[1]: port 1<br>Bit[2]: port 2<br>Bit[3]: port 3<br>Bit[4]: port 4<br>Bit[5]: port 5<br><br>It is valid only if the corresponding ILL_SMAC_PROT bit is enabled | 6'b11111<br>1 |

### 5.3.10 Learning Control Register

| PHY | MII       | ROM     | R/W | Description   | Default |
|-----|-----------|---------|-----|---|---------|
| 20  | 13[15:10] |         |     | RESERVED  |         |
|     | 13[9:8]   | 15[7:6] | R/W | FILTER_MDMAC<br>Filter unknown multicast DMAC<br><br>2'b00 : Flooding<br>2'b01 : Forward to CPU<br>2'b10 : Discard<br>2'b11 : Reserved<br>Note : Multicast DMAC does not include broadcast DMAC | 2'b00   |
|     | 13[7:6]   | 15[5:4] | R/W | FILTER_UDMAC<br>Filter unknown unicast DMAC<br><br>2'b00 : Flooding<br>2'b01 : Forward to CPU<br>2'b10 : Discard<br>2'b11 : Reserved  | 2'b00   |
|     | 13[5]     | 16[5]   | R/W | LEARN_DIS_PAUSE<br>Learning disable because of PAUSE frame  | 1'b1    |



| PHY | MII   | ROM   | R/W | Description  | Default       |
|-----|-------|-------|-----|--|---------------|
|     | 13[4] | 16[4] | R/W | RESERVED   |               |
|     | 13[3] | 16[3] | R/W | AT_STR<br>Address Table Structure<br><br>0: 2K Address Table for unicast frame (default)<br>1: 1K Address Table for unicast frame and 1K Address Table for multicast frame<br>Note – We recommend clear address table once this bit is modified. | pin_42<br>(0) |
|     | 13[2] |       |     | RESERVED   |               |
|     | 13[1] | 16[1] | R/W | IGMP_OVER_VLAN<br>0 : Disable<br>1 : Enable<br>It is valid only for LEARN_CONSTRAIN is enabled   | pin_42<br>(0) |
|     | 13[0] | 16[0] | R/W | LEARN_CONSTRAIN<br>Learning Constraint<br>0 : VLAN information(FID) is not used to create a hash key<br>1 : VLAN information(FID) is used to create a hash key<br><br>Note – We recommend clear address table once this bit is modified.         | 1'b0          |

5.3.11 Aging Time Parameter

| PHY     | MII      | ROM     | R/W  | Description   | Default |               |       |
|---------|----------|---------|--|---|---------|---------------|-------|
| 20      | 14[15:7] |         |  | RESERVED  |         |               |       |
|         | 14[6:5]  | 17[6:5] | R/W  | AGE_TIME_UNIT<br><br>2'b00 : 1 minutes<br>2'b01 : 1 second<br>2'b10 : 10 ms<br>2'b11 : fast mode. This mode will age out whole table in 1~2 ms. For some special application (ex. RSTP) need to clear table ASAP.<br>Independent with AGE_TIME_VLE. | 2'b00   |               |       |
|         | 14[4:0]  | 17[4:0] | R/W  | AGE_TIME_VLE<br>Age Time Value.<br><br>5'h00: no aging<br>AGE_TIME= AGE_TIME_UNIT * AGE_TIME_VLE  | *       |               |       |
|         |          |         |  | Default Value   |         |               |       |
|         |          |         |  | TEST2=0   |         | TEST2=1       |       |
|         |          |         |  | Pin74 P4EXT=1   |         | Pin74 P4EXT=0 | 5'h05 |
|         |          |         |  | 5'h05   |         | Pin65(5'h05)  |       |
|         | 15[15:9] |         |  | RESERVED  |         |               |       |
|         | 15[8]    | 18[3]   | R/W  | PID_EN<br><br>If set, the aging module ages entries whose Port ID matches PID_VAL   | 1'b0    |               |       |
|         | 15[7:5]  | 18[2:0] | R/W  | PID_VAL[2:0]<br>Port ID Value<br><br>3'b000 : reserved (default)<br>3'b001 : port 0<br>3'b010 : port 1<br>3'b011 : port 2<br>3'b100 : port 3<br>3'b101 : port 4<br>3'b110 : port 5 (cpu port)<br>other : reserved                                   | 3'b000  |               |       |
| 15[4]   | 19[4]    | R/W     | FID_EN<br><br>If set, the aging module ages entries whose FID matches FID_VAL<br>0: Disable<br>1: Enable | 1'b0  |         |               |       |
| 15[3:0] | 19[3:0]  | R/W     | FID_VAL[3:0]<br>FID Value  | 4'h0  |         |               |       |

5.3.12 Broadcast Storm Protection

| PHY | MII       | ROM     | R/W | Description   | Default |
|-----|-----------|---------|-----|---|---------|
| 20  | 16[15:14] |         |     | RESERVED  |         |
|     | 16[13:8]  | 20[5:0] | R/W | BF_STM_EN[5:0]<br>Broadcast storm enable<br>1: enable<br>Drop the incoming packet if the number of queued broadcast packet is over the threshold. The threshold is defined in MII register 20.17~20.19<br>0: disable (default)<br>Default Value<br>TEST2=0<br>TEST2=1<br>Pin113 MII2_EN=1      Pin113 MII2_EN=0      6'h0<br>6'h0      Pin102 BF_STM_EN (6'h0)  | *       |
|     | 16[7:6]   |         |     | RESERVED  |         |
|     | 16[5:0]   | 21[5:0] | R/W | BF_FFFF_ONLY[5:0]<br>Multicast broadcast storm protection disable<br>1: "Broadcast storm protection" does not include multicast packets. IP175DLF drops the packets with DA equals to 0xFFFFFFFF only when the broadcast threshold is reached (default),<br>0: "Broadcast storm protection" includes multicast packets. IP175DLF drops the packets with DA equals to 0xFFFFFFFF, or multi-cast address when the broadcast threshold is reached.<br>"Broadcast storm protection" does not drop packets due to not learned address. | 6'h3f   |
|     | 17[15:8]  | 23[7:0] | R/W | BF_STM_THR_1[7:0]<br>Broadcast storm threshold setting for port 1   | 8'h08   |
|     | 17[7:0]   | 22[7:0] | R/W | BF_STM_THR_0[7:0]<br>Broadcast storm threshold setting for port 0<br>Threshold setting range is from 1 to 255 packets/10ms for 100Mbps connection or 1 to 255 packets/100ms for 10Mbps connection   | 8'h08   |
|     | 18[15:8]  | 25[7:0] | R/W | BF_STM_THR_3[7:0]<br>Broadcast storm threshold setting for port 3   | 8'h08   |
|     | 18[7:0]   | 24[7:0] | R/W | BF_STM_THR_2[7:0]<br>Broadcast storm threshold setting for port 2   | 8'h08   |
|     | 19[15:8]  | 27[7:0] | R/W | BF_STM_THR_5[7:0]<br>Broadcast storm threshold setting for port 5   | 8'h08   |
|     | 19[7:0]   | 26[7:0] | R/W | BF_STM_THR_4[7:0]<br>Broadcast storm threshold setting for port 4   | 8'h08   |

### 5.3.13 Port Mirror

| PHY | MII       | ROM     | R/W | Description   | Default |
|-----|-----------|---------|-----|---|---------|
| 20  | 20[15]    | 28[7]   | R/W | PORT_MIRROR_EN  | 1'b0    |
|     | 20[14:13] | 28[6:5] | R/W | PORT_MIRROR_MODE[1:0]<br>Select a mirror mode to monitor<br>2'b00: mirror one port of RX (default)<br>2'b01: mirror one port of TX<br>2'b10: mirror source-destination pair<br>(port of TX and RX must be the different)<br>2'b11: mirror one port of TX and RX<br>(port of TX and RX must be the same) | 2'b00   |
|     | 20[12:6]  |         |     | RESERVED  |         |
|     | 20[5:0]   | 29[5:0] | R/W | SEL_RX_PORT_MIRROR[5:0]<br>Select the source (receive) port to be mirrored<br>6'b00_0000: reserved (default)<br>6'b00_0001: port 0<br>6'b00_0010: port 1<br>6'b00_0100: port 2<br>6'b00_1000: port 3<br>6'b01_0000: port 4<br>6'b10_0000: port 5 (MII0)<br>other: reserved                              | 6'h00   |
|     | 21[15]    |         |     | RESERVED  |         |
|     | 21[14:12] | 28[4:2] | R/W | SEL_MIRROR_PORT[2:0]<br>Select a mirror port to monitor any other port<br>3'b000: port 0<br>3'b001: port 1<br>3'b010: port 2<br>3'b011: port 3<br>3'b100: port 4<br>3'b101: port 5 (MII0)(default)<br>other: reserved   | 3'b101  |
|     | 21[11:6]  |         |     | RESERVED  |         |
|     | 21[5:0]   | 30[5:0] | R/W | SEL_TX_PORT_MIRROR[5:0]<br>Select the destination (transmit) port to be mirrored<br>6'b00_0000: reserved (default)<br>6'b00_0001: port 0<br>6'b00_0010: port 1<br>6'b00_0100: port 2<br>6'b00_1000: port 3<br>6'b01_0000: port 4<br>6'b10_0000: port 5 (MII0)<br>other: reserved                        | 6'h00   |



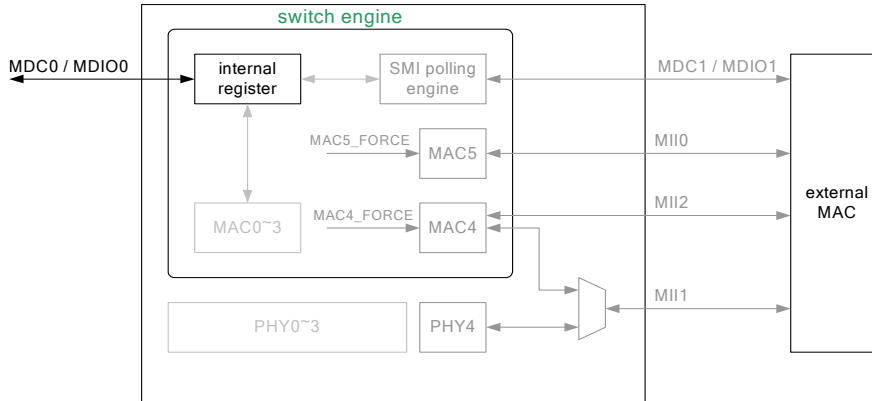
5.3.14 Source Block Protection

| PHY | MII      | ROM   | R/W       | Description  | Default |
|-----|----------|-------|-----------|--|---------|
| 20  | 22[15:7] |       |           | RESERVED   |         |
|     | 22[6]    | 31[6] | R/W       | SBP_EN<br>Source Block Protection Enable   | 1'b0    |
|     | 22[5:0]  |       | R<br>(SC) | SBP_STATUS[5:0]<br>Source Block Protection Status<br><br>Bit[0]: port 0<br>Bit[1]: port 1<br>Bit[2]: port 2<br>Bit[3]: port 3<br>Bit[4]: port 4<br>Bit[5]: port 5<br>Self-clear after read | 6'h00   |

5.3.15 LED Control Register

| PHY | MII     | ROM     | R/W | Description  | Default                      |
|-----|---------|---------|-----|--|------------------------------|
| 20  | 24[2]   | 33[2]   | R/W | SERIAL_LED_MODE<br>If MII2_EN is enabled, then it will turn to serial LED mode directly.<br>1: supports link LED only<br>0: supports link, speed, and duplex LED (default)   | pin 112<br>(0)               |
|     | 24[1:0] | 33[1:0] | R/W | LED_SEL[1:0]<br>LED output mode selection.<br>LED_SEL[1:0]=2'b00: LED mode 0,<br>LED_SEL[1:0]=2'b01: LED mode 1,<br>LED_SEL[1:0]=2'b10: LED mode 2,<br>LED_SEL[1:0]=2'b11: LED mode 3 (default)<br><br>It is for debug only. User should not update the setting of LED_SEL pins by writing this registers. | pin 92,<br>pin 91<br>(2'b11) |

## 5.4 External MII Control Register



### 5.4.1 External MII Status Report Register

| PHY | MII   | ROM | R/W | Description   | Default |
|-----|-------|-----|-----|---|---------|
| 21  | 0[15] | --  | RO  | MII1_FULL<br>1: full, 0: half                                   | 1'b1    |
|     | 0[14] | --  | RO  | MII1_SPEED10<br>1: 10M, 0: 100M                                 | 1'b0    |
|     | 0[13] | --  | RO  | MII1_FLOW<br>MII1 flow control ability<br>1: enable, 0: disable | 1'b1    |
|     | 0[7]  | --  | RO  | MII0_FULL<br>1: full, 0: half                                   | 1'b1    |
|     | 0[6]  | --  | RO  | MII0_SPEED10<br>1: 10M, 0: 100M                                 | 1'b0    |
|     | 0[5]  | --  | RO  | MII0_FLOW<br>MII0 flow control ability<br>1: enable, 0: disable | 1'b1    |

5.4.2 MII0 MAC Mode Register

| PHY | MII     | ROM     | R/W | Description   | Default      |
|-----|---------|---------|-----|---|--------------|
| 21  | 1[15]   | --      | RO  | MAC_XCTRLLEN[0]<br>Flow control capability of the link partner of external PHY on MII0<br>1: link partner supports flow control,<br>0: link partner does not support flow control       | 1'b1         |
|     | 1[14]   | --      | RO  | MAC_FORCE[0]<br>1: MII0's speed and duplex are forced because IP175DLF finds external PHY doesn't support SMI<br>0: MII0 polls external PHY through SMI to decide its speed and duplex. | 1'b0         |
|     | 1[13]   | --      | RO  | MII0_link<br>1: link ok, 0: un-link   | 1'b1         |
|     | 1[12:8] | 40[4:0] | R/W | Capability of external PHY on MII0<br>bit12: flow control ability,<br>bit11: 100M full duplex,<br>bit10 : 100M half duplex,<br>bit9 : 10M full duplex,<br>bit8: 10M half duplex         | 5'b<br>11111 |
|     | 1[7]    | --      | RO  | Speed of external PHY on MII0<br>1: 10M,<br>0: 100M   | 1'b0         |
|     | 1[6]    | --      | RO  | Duplex of external PHY on MII0<br>1: full duplex,<br>0: half duplex   | 1'b1         |
|     | 1[5]    | --      | RO  | Link status of external PHY on MII0<br>1: link on,<br>0: link off   | 1'b1         |
|     | 1[4:0]  | 41[4:0] | R/W | MII0_MAC_PHY_ADDR[4:0]  | 5'b<br>00000 |

### 5.4.3 MII1 MAC Mode or MII2 MAC Mode Register

(Only one is active at the same time.)

| PHY | MII     | ROM     | R/W | Description   | Default      |
|-----|---------|---------|-----|---|--------------|
| 21  | 2[15]   | --      | RO  | MAC_XCTRLLEN[1]<br>Flow control capability of the link partner of external PHY on MII1 MAC or MII2 MAC<br>1: link partner supports flow control,<br>0: link partner does not support flow control   | 1'b1         |
|     | 2[14]   | --      | RO  | MAC_FORCE[1]<br>1: MII1orMII2's speed and duplex are forced because IP175DLF finds external PHY doesn't support SMI<br>0: MII1orMII2 polls external PHY through SMI to decide its speed and duplex. | 1'b0         |
|     | 2[13]   | --      | RO  | MII1ORMII2_LINK (MII1_LINK)<br>1: link ok, 0: un-link   | 1'b1         |
|     | 2[12:8] | 42[4:0] | R/W | Capability of external PHY on MII1 MAC or MII2 MAC<br>bit 12: flow control ability,<br>bit 11: 100M full duplex,<br>bit 10: 100M half duplex,<br>bit 9: 10M full duplex,<br>bit 8: 10M half duplex  | 5'b<br>11111 |
|     | 2[7]    | --      | RO  | Speed of external PHY on MII1 MAC or MII2 MAC<br>1: 10M,<br>0: 100M   | 1'b0         |
|     | 2[6]    | --      | RO  | Duplex of external PHY on MII1 MAC or MII2 MAC<br>1: full duplex,<br>0: half duplex   | 1'b1         |
|     | 2[5]    | --      | RO  | Link status of external PHY on MII1 MAC or MII2 MAC<br>1: link on,<br>0: link off   | 1'b1         |
|     | 2[4:0]  | 43[4:0] | R/W | MII1orMII2_MAC_PHY_ADDR[4:0]  | 5'b<br>00001 |

5.4.4 MII0, MII1 and MII2 Control Register 1

| PHY                 | MII   | ROM   | R/W   | Description   | Default       |                         |
|---------------------|-------|-------|---|---|---------------|-------------------------|
| 21                  | 3[15] | 44[7] | R/W   | P4EXT<br>1: enable<br>0: disable (default)  | pin 74<br>(0) |                         |
|                     | 3[14] | --    | RO  | SMI0_POLLING<br>1: MII0 MAC mode<br>0: MII0 PHY mode  | 1'b0          |                         |
|                     | 3[13] | --    | RO  | SMI1_POLLING<br>1: MII1 MAC mode<br>0: MII1 PHY mode  | 1'b0          |                         |
|                     | 3[12] | 44[6] | R/W   | MII1_PHY_MODE<br>1: MII1 is connected to PHY4.0: MII1 is connected to MAC4.   | pin 54<br>(1) |                         |
|                     | 3[11] | 44[5] | R/W   | MII0_MAC_MODE_EN<br>External MII0 port MAC mode<br>1: MII0 works as a MAC and should be connected to an external PHY.<br>0: MII0 works as a PHY and should be connected to an external MAC device (default).<br>This bit does not affect MII1 port. | *             |                         |
|                     |       |       |   | Default Value   |               |                         |
|                     |       |       |   | MII2_EN=1   |               | MII2_EN=0               |
|                     |       |       |   | 0   |               | Pin96 MII0_MAC_MODE (0) |
|                     | 3[10] | 44[4] | R/W   | MII0_RMII_EN (RMII_EN)<br>1: MII0 RMII interface enabled<br>0: MII0 RMII interface disabled (default).  | pin 53<br>(0) |                         |
|                     |       |       |   | Default Value   |               |                         |
| P4EXT=1 & RMII_EN=1 |       |       |   | Others  |               |                         |
| 1                   |       |       |   | 0   |               |                         |
| 3[9]                | 44[3] | R/W   | MII2_RMII_EN (MII1OR2_RMII_EN)<br>1: MII2 RMII interface enabled<br>0: MII2 RMII interface disabled (default).                  | *   |               |                         |
|                     |       |       | Default Value   |   |               |                         |
|                     |       |       | P4EXT=1 & RMII_EN=1 & MII2_EN=1   |   | Others        |                         |
|                     |       |       | 1   |   | 0             |                         |
| 3[8]                | 44[2] | R/W   | MII1_RMII_EN (PHY4_RMII_EN)<br>1: MII1 RMII interface enabled<br>0: MII1 RMII interface disabled (default).                     | *   |               |                         |
|                     |       |       | Default Value   |   |               |                         |
|                     |       |       | P4EXT=1 & RMII_EN=1 & MII1_DIS=0  |   | Others        |                         |
|                     |       |       | 1   |   | 0             |                         |
| 3[7]                | 44[1] | R/W   | MII1OR2_MAC_REPEATER<br>1: external PHY 's TXEN does not loop back to CRS (default)<br>0: external PHY 's TXEN loop back to CRS | 1'b1  |               |                         |
| 3[6]                | 44[0] | R/W   | MII0_MAC_REPEATER<br>1: external PHY 's TXEN does not loop back to CRS (default)<br>0: external PHY 's TXEN loop back to CRS    | 1'b1  |               |                         |



| PHY | MII  | ROM   | R/W | Description   | Default       |
|-----|------|-------|-----|---|---------------|
|     | 3[5] | 45[7] | R/W | MII2_PHY_COL_DELAY<br>0: no delay,<br>1: collision delay 24 clocks (default)<br>It is valid only if MII2 is enabled and it works at PHY mode. | 1'b1          |
| 21  | 3[4] | 45[6] | R/W | MII0_PHY_COL_DELAY<br>0: no delay,<br>1: collision delay 24 clocks (default)<br>It is valid only if MII0 is enabled and it works at PHY mode. | 1'b1          |
|     | 3[2] | 45[5] | R/W | MII2_EN<br>1: enable, 0: disable (default)  | Pin113<br>(0) |
|     | 3[0] | 45[4] | R/W | MII2_MAC_MOD<br>1: MII2 works in MAC mode<br>0: MII2 works in PHY mode (default)  | Pin111<br>(0) |

#### 5.4.5 MII0, MII1 and MII2 Control Register 2

| PHY | MII  | ROM   | R/W | Description  | Default |
|-----|------|-------|-----|--|---------|
| 21  | 4[2] | 45[3] | R/W | MII12_CHK_CRC<br>Examine CRC filed of every incoming frame of MII 1 or MII 2 port. | 1'b1    |
|     | 4[1] | 45[2] | R/W | MII0_CHK_CRC<br>Examine CRC filed of every incoming frame of MII 0 port.           | 1'b1    |

### 5.5 IGMP Control Register

#### 5.5.1 Base Control Register

| PHY | MII      | ROM     | R/W | Description   | Default |
|-----|----------|---------|-----|---|---------|
| 21  | 5[15:11] |         |     | RESERVED  |         |
|     | 5[10]    | 50[6]   | R/W | FAST_LEAVE  | 1'b1    |
|     | 5[9]     | 45[1]   | R/W | MG_INCLUDE_RP<br>Multicast group include router port<br>0:Disabled<br>1:Enabled   | 1'b0    |
|     | 5[8]     | 45[0]   | R/W | FLOOD_UNIGMP<br>Flood Unknown IGMP<br><br>Unknown IGMP is not one of following:<br>1. General Query<br>2. Group-Specific Query<br>3. IGMP Report<br>4. IGMP Leave   | 1'b0    |
|     | 5[7]     | 46[7]   | R/W | FLOOD_IPM_CTRL<br>Flood IP Multicast Control Packet<br>0:Disabled<br>1:Enabled<br>Note – IP multicast control packet: DMAC=01-00-5e-xx-xx-xx, DIP= 224.0.0.x and non-IGMP   | 1'b0    |
|     | 5[6:5]   | 46[6:5] | R/W | UNIPM_MODE[1:0]<br>Unknown IP Multicast Data Mode<br>2'b00 : discard<br>2'b01 : forward to CPU<br>2'b10 : flood packet<br>2'b11 : forward to router port<br>Note – IP multicast data packet: DMAC=01-00-5e-xx-xx-xx and DIP=outside 224.0.0.x | 2'b11   |
|     | 5[4]     | 46[4]   | R/W | DISCARD_LEAVE<br>Discard IGMP leave message<br>0:Disabled<br>1:Enabled  | 1'b0    |
|     | 5[3]     | 46[3]   | R/W | FLOOD_RPT<br>Flood report message to other ports<br>0:Disabled<br>1:Enabled   | 1'b0    |



| PHY | MII  | ROM   | R/W | Description  | Default       |
|-----|------|-------|-----|--|---------------|
|     | 5[2] | 46[2] | R/W | LRP_NULL_SIP<br>Learn router port even if source IP address is 0.0.0.0<br>0:Disable<br>1:Enable<br>It is valid only if LEARN_RP is enabled | 1'b0          |
|     | 5[1] | 46[1] | R/W | LEARN_RP<br>Learn Router Port<br>0: Disable (default)<br>1: Enable   | pin_42<br>(0) |
|     | 5[0] | 46[0] | R/W | HW_IGMP_EN<br>Hardware IGMP Enable<br>0:Disable (default)<br>1:Enable  | pin_42<br>(0) |

### 5.5.2 Router Port Timeout

| PHY | MII     | ROM     | R/W | Description  | Default       |              |
|-----|---------|---------|-----|--|---------------|--------------|
| 21  | 6[15:8] | 47[7:0] | R/W | ROUTER_TIMEOUT_VLE[7:0]<br>Router Timeout Value<br>Router Timeout = ROUTER_TIMEOUT_UNIT *<br>ROUTER_TIMEOUT_VLE          | *             |              |
|     |         |         |     | Default Value  |               |              |
|     |         |         |     | HW_IGMP_EN=1   |               | HW_IGMP_EN=0 |
|     |         |         |     | 8'h96  |               | 8'h00        |
|     | 6[7:6]  | 48[7:6] | R/W | ROUTER_TIMEOUT_UNIT[1:0]<br>2'b00: 1 second<br>2'b01: 2 second<br>2'b10: 4 second<br>2'b11: 8 second                     | *             |              |
|     |         |         |     | Default Value  |               |              |
|     |         |         |     | HW_IGMP_EN=1   |               | HW_IGMP_EN=0 |
|     |         |         |     | 2'b01  |               | 2'b00        |
|     | 6[5:0]  | 48[5:0] | R/W | DEFAULT_ROUTER_PORT[5:0]<br>bit0: port 0<br>bit1: port 1<br>bit2: port 2<br>bit3: port 3<br>bit4: port 4<br>bit5: port 5 | 6'b00000<br>0 |              |

5.5.3 IGMP Group Timeout

| PHY    | MII     | ROM     | R/W  | Description  | Default      |              |
|--------|---------|---------|--|--|--------------|--------------|
| 21     | 7[15:8] | 49[7:0] | R/W  | IGMP_TIMEOUT_VLE[7:0]<br>IGMP Timeout Value            | *            |              |
|        |         |         |  | IGMP Timeout = IGMP_TIMEOUT_UNIT *<br>IGMP_TIMEOUT_VLE |              |              |
|        |         |         |  | Default Value  |              |              |
|        |         |         |  | HW_IGMP_EN=1   |              | HW_IGMP_EN=0 |
|        |         |         |  | 8'h96  |              | 8'h00        |
| 7[1:0] | 50[1:0] | R/W     | IGMP_TIMEOUT_UNIT[1:0]<br>IGMP Timeout Unit                              | *  |              |              |
|        |         |         | 2'b00: 1 second<br>2'b01: 2 second<br>2'b10: 4 second<br>2'b11: 8 second |  |              |              |
|        |         |         | Default Value  |  |              |              |
|        |         |         | HW_IGMP_EN=1   |  | HW_IGMP_EN=0 |              |
|        |         |         | 2'b01  |  | 2'b00        |              |

## 5.6 Rate Control

### 5.6.1 Basic Rate Setting Register

| PHY | MII      | ROM | R/W | Description  | Default      |
|-----|----------|-----|-----|--|--------------|
| 21  | 8[7:0]   | --  | R/W | BW_TI[7:0]<br>Rate control time interval.<br>Only used by egress port and output queue<br>unit : millisecond | 8'h01        |
|     | 9[15:0]  | --  | R/W | BW_MBS[15:0]<br>Rate control Maximum Burst Size<br>Expressed in byte.  | 16'h<br>0000 |
|     | 10[15:0] | --  | R/W | BW_CREDIT_SIZE[15:0]<br>Credit size to accumulate the bucket in per time interval.<br>Expressed in byte.     | 16'h<br>0000 |

### 5.6.2 Rate Setting Access Control Register

| PHY | MII     | ROM | R/W         | Description   | Default |
|-----|---------|-----|-------------|---|---------|
| 21  | 12[2:0] | --  | R/W         | BW_PORT[2:0]<br>Port number for setting bandwidth rate.   | 3'h0    |
|     | 12[3]   | --  | R/W         | BW_IOE<br>Bandwidth rate setting is on ingress or egress port<br>0: ingress port (default)<br>1: egress port  | 1'b0    |
|     | 12[5:4] | --  | R/W         | BW_QUEUE[1:0]<br>Assign the egress output queue number for setting rate control<br>value<br>2'b00:egress port (default)<br>2'b01:queue 1<br>2'b10:queue 2<br>2'b11:queue 3  | 2'b00   |
|     | 12[8]   | --  | R/W         | BW_RW<br>Rate control data read/write signal<br>0: read rate control data (default)<br>1: write rate control data   | 1'b0    |
|     | 12[9]   | --  | R/W<br>(SC) | BW_RW_START<br>Indicates start read/write rate control data of a port, when write a<br>logical "1" to this register.<br>A self cleared register after read/write data done. | 1'b0    |

## 5.7 Address Table Access Register

### 5.7.1 Command Register

| PHY | MII       | ROM | R/W      | Description   | Default |
|-----|-----------|-----|----------|---|---------|
| 21  | 14[15]    | --  | R/W (SC) | START/DONE<br>To initiate a read or write command when set as 1.<br>Self-cleared after read or write command is finished<br>1: start access the address table<br>0: access operation is completed | 1'b0    |
|     | 14[14]    | --  |          | RESERVED  | 1'b0    |
|     | 14[13]    | --  | RO       | DATA_VALID<br>Data Valid<br>IP175DLF will set this bit to 1 to indicate the data is available in "Data Buffer Register" for read operation  | 1'b0    |
|     | 14[12:11] | --  | R/W      | COMMAND[1:0]<br>Address Table Command<br>2'b00: reserved<br>2'b01: single write<br>2'b10: single read<br>2'b11: reserved  | 2'b00   |
|     | 14[10:0]  | --  | R/W      | INDEX<br>The index selects one of address table entries.  | 11'h000 |

### 5.7.2 Data Buffer Register (For Unicast MAC Address)

| PHY | MII       | ROM | R/W | Description   | Default  |
|-----|-----------|-----|-----|---|----------|
| 21  | 15[15:0]  | --  | R/W | MAC_ADDR[15:0]  | 16'h0000 |
|     | 16[15:0]  | --  | R/W | MAC_ADDR[31:16]   | 16'h0000 |
|     | 17[15:0]  | --  | R/W | MAC_ADDR[47:32]   | 16'h0000 |
|     | 18[15:14] | --  | R/W | FILTER_INFO   | 2'b00    |
|     | 18[13:10] | --  | R/W | PRI_INFO  | 4'h0     |
|     | 18[9:6]   | --  | R/W | FID   | 4'h0     |
|     | 18[5:3]   | --  | R/W | PORT_ID<br>Note – If PORT_ID set to all zero, frame's DMAC matched this entry is discarded. | 3'b000   |
|     | 18[2:0]   | --  | R/W | AGE<br>Note – Entry is aged out or invalid if this field is all zero.                       | 3'b000   |
|     | 19[15:2]  |     |     | RESERVED  |          |
|     | 19[1]     | --  | R/W | STATIC<br>Entry is static and can not overwrite or aged out.                                | 1'b0     |
|     | 19[0]     | --  | R/W | RESERVED  |          |

### 5.7.3 Data Buffer Register (For Multicast MAC Address)

| PHY | MII      | ROM | R/W | Description     | Default  |
|-----|----------|-----|-----|-----------------|----------|
| 21  | 15[15:0] | --  | R/W | MAC_ADDR[15:0]  | 16'h0000 |
|     | 16[15:0] | --  | R/W | MAC_ADDR[31:16] | 16'h0000 |
|     | 17[15:0] | --  | R/W | MAC_ADDR[47:32] | 16'h0000 |

| PHY | MII       | ROM | R/W | Description  | Default |
|-----|-----------|-----|-----|--|---------|
|     | 18[15:14] | --  | R/W | FILTER_INFO  | 2'b00   |
|     | 18[13:10] | --  | R/W | PRI_INFO   | 4'h0    |
|     | 18[9:6]   | --  | R/W | FID  | 4'h0    |
|     | 18[5:0]   | --  | R/W | PORT_MAP<br>Note –If PORT_MAP set to all zero, frame's DMAC matched this entry is discarded. | 6'h0    |
|     | 19[15:2]  |     |     | RESERVED   |         |
|     | 19[1]     | --  | R/W | VALID<br>Entry is valid.   | 1'b0    |
|     | 19[0]     | --  | R/W | IGMP<br>This bit shall set to 0.   | 1'b0    |

#### 5.7.4 Data Buffer Register (For IP Multicast Address)

| PHY   | MII       | ROM | R/W                              | Description   | Default  |
|-------|-----------|-----|----------------------------------|---|----------|
| 21    | 15[15:0]  | --  | R/W                              | MAC_ADDR[15:0]  | 16'h0000 |
|       | 16[15:14] | --  | R/W                              | TIMEOUT_P2[1:0]   | 2'b00    |
|       | 16[13:11] | --  | R/W                              | TIMEOUT_P1[2:0]   | 3'b000   |
|       | 16[10:8]  | --  | R/W                              | TIMEOUT_P0[2:0]   | 3'b000   |
|       | 16[7]     | --  | R/W                              | MAC_ADDR[23]<br>This bit shall be set to 0.   | 1'b0     |
|       | 16[6:0]   | --  | R/W                              | MAC_ADDR[22:16]   | 7'h0     |
|       | 17[15:10] |     |                                  | RESERVED  |          |
|       | 17[9:7]   | --  | R/W                              | TIMEOUT_P5[2:0]   | 3'b000   |
|       | 17[6:4]   | --  | R/W                              | TIMEOUT_P4[2:0]   | 3'b000   |
|       | 17[3:1]   | --  | R/W                              | TIMEOUT_P3[2:0]   | 3'b000   |
|       | 17[0]     | --  | R/W                              | TIMEOUT_P2[2]   | 1'b0     |
|       | 18[15:14] | --  | R/W                              | FILTER_INFO   | 2'b00    |
|       | 18[13:10] | --  | R/W                              | PRI_INFO  | 4'h0     |
|       | 18[9:6]   | --  | R/W                              | FID   | 4'h0     |
|       | 18[5:0]   | --  | R/W                              | PORT_MAP<br>Note – If PORT_MAP set to all zero, frame's DMAC matched this entry is discarded. | 6'h0     |
|       | 19[15:2]  |     |                                  | RESERVED  |          |
|       | 19[1]     | --  | R/W                              | VALID<br>Entry is valid.  | 1'b0     |
| 19[0] | --        | R/W | IGMP<br>This bit shall set to 1. | 1'b1  |          |

## 5.8 CPU Interrupt Register

### 5.8.1 CPU Interrupt Control Register

| PHY | MII    | ROM | R/W | Description  | Default |
|-----|--------|-----|-----|--|---------|
| 21  | 20[15] | --  | R/W | INIT_HIGH<br>Interrupt signal is active high.<br>1: active high<br>0: active low | 1'b0    |

### 5.8.2 CPU Interrupt Enable Register

| PHY | MII   | ROM | R/W | Description   | Default |
|-----|-------|-----|-----|---|---------|
| 21  | 20[7] | --  | R/W | VLAN_VIO_INT_EN<br>Enable VLAN violation interrupt                                      | 1'b0    |
|     | 20[6] | --  | R/W | AT_UNICAST_VIO_INT_EN<br>Enable address table violation interrupt for unicast frame     | 1'b0    |
|     | 20[5] | --  | R/W | AT_MULTICAST_VIO_INT_EN<br>Enable address table violation interrupt for multicast frame | 1'b0    |
|     | 20[4] | --  | R/W | AT_IGMP_VIO_INT_EN<br>Enable address table violation interrupt for IP multicast frame   | 1'b0    |
|     | 20[3] | --  | R/W | SEC_VIO_INT_EN<br>Enable security violation interrupt                                   | 1'b0    |
|     | 20[2] | --  | R/W | LEARN_VIO_INT_EN<br>Enable learning violation interrupt                                 | 1'b0    |
|     | 20[1] | --  | R/W | SBP_INT_EN<br>Enable source blocking protection interrupt                               | 1'b0    |
|     | 20[0] | --  | R/W | MF_CNT_OF_INT_EN<br>Enable Multi-Field counter overflow interrupt                       | 1'b0    |

### 5.8.3 CPU Interrupt Status Register

The interrupt registers are self-cleared register after read.

| PHY | MII   | ROM | R/W        | Description   | Default |
|-----|-------|-----|------------|---|---------|
| 21  | 21[7] | --  | RO<br>(SC) | VLAN_VIO_INT<br>Violates the VLAN rule interrupt                              | 1'b0    |
|     | 21[6] | --  | RO<br>(SC) | AT_UNICAST_VIO_INT<br>Address table violation interrupt for unicast frame     | 1'b0    |
|     | 21[5] | --  | RO<br>(SC) | AT_MULTICAST_VIO_INT<br>Address table violation interrupt for multicast frame | 1'b0    |
|     | 21[4] | --  | RO<br>(SC) | AT_IGMP_VIO_INT<br>Address table violation interrupt for IP multicast frame   | 1'b0    |
|     | 21[3] | --  | RO<br>(SC) | SEC_VIO_INT<br>Security violation interrupt                                   | 1'b0    |
|     | 21[2] | --  | RO<br>(SC) | LEARN_VIO_INT<br>Learning violation interrupt                                 | 1'b0    |
|     | 21[1] | --  | RO<br>(SC) | SBP_INT<br>Source blocking protection interrupt                               | 1'b0    |
|     | 21[0] | --  | RO<br>(SC) | MF_CNT_OF_INT<br>Multi-Field counter overflow interrupt                       | 1'b0    |

### 5.9 Miscellaneous Control Register

| PHY   | MII       | ROM     | R/W   | Description  | Default        |                   |
|-------|-----------|---------|---|--|----------------|-------------------|
| 21    | 22[15]    |         |   | RESERVED   |                |                   |
|       | 22[14]    | 51[6]   | R/W   | REDUCE_IPG<br>This function reduce the IPG by random from 0~20 PPM<br>1: enable<br>0: disable  | *              |                   |
|       |           |         |   | Default Value  |                |                   |
|       |           |         |   | Pin 113 MII2_EN=1  |                | Pin 113 MII2_EN=0 |
|       |           |         |   | 0  |                | Pin 97(1)         |
|       | 22[13]    | 51[5]   | R/W   | TWOPARTD<br>Reset the inter-frame-gap counter to zero, if the CRS signal asserted during the two third of IPG period.<br>1: enable<br>0 disable  | 1'b1           |                   |
|       | 22[12]    | 51[4]   | R/W   | HP_DIS_FLOW_EN<br>High priority packet to disable flow control<br>1: a port will disable its flow control function for 2 sec if it receives a high priority packet.<br>0: the function is disabled | 1'b0           |                   |
|       | 22[11:10] | 51[3:2] | R/W   | DRIVE[1:0]<br>Pad driving capability selection<br>00: 4 mA<br>01: 8 mA<br>10: 12 mA<br>11: 16 mA   | 2'b01          |                   |
|       | 22[9:8]   |         |   | RESERVED   |                |                   |
|       | 22[3]     | 50[5]   | R/W   | LINK_Q_EN, LINK quality enable<br>1:enable (default)<br>0:disable  | pin_101<br>(1) |                   |
| 22[2] | 50[4]     | R/W     | TB31_EN<br>Turbo MII0 31.25MHZ output enable<br>1: Turbo MII mode (MII0) output 31.25MHZ MIICLK<br>0: Turbo MII mode (MII0) output 50MHZ MIICLK | 1'b0   |                |                   |
| 22[1] | 50[3]     | R/W     | STAG_TX_EN<br>Special tagging for TX enable<br>1: enable<br>0: disable  | 1'b0   |                |                   |
| 22[0] | 50[2]     | R/W     | STAG_RX_EN<br>Special tagging for RX enable<br>1: enable<br>0: disable  | 1'b0   |                |                   |

| PHY  | MII     | ROM   | R/W                    | Description            | Default   |            |
|--|---------|-------|------------------------|------------------------|---|------------|
| <b>Reserved register (It is for testing only and is not released to users)</b> |         |       |                        |                        |   |            |
| 21   | 23[12]  | 52[7] | R/W                    | PHY_TEST_PIN_SETTING_5 | *   |            |
|  |         |       |                        | Default Value          |   |            |
|  |         |       |                        | TEST2=0                |   | TEST2=1    |
|  |         |       |                        | 1                      |   | Pin 57 (0) |
| 23[11]   | 52[6]   | R/W   | PHY_TEST_PIN_SETTING_2 | *                      |   |            |
|  |         |       | Default Value          |                        |   |            |
|  |         |       | TEST2=0                |                        | TEST2=1   |            |
|  |         |       | 0                      |                        | Pin 79 (0)  |            |
| 23[10]   | 52[5]   | R/W   | PHY_TEST_PIN_SETTING_3 | *                      |   |            |
|  |         |       | Default Value          |                        |   |            |
|  |         |       | TEST2=0                |                        | TEST2=1   |            |
|  |         |       | 0                      |                        | Pin 84 (0)  |            |
| 23[9]  | 52[4]   | R/W   | PHY_TEST_PIN_SETTING_4 | *                      |   |            |
|  |         |       | Default Value          |                        |   |            |
|  |         |       | TEST2=0                |                        | TEST2=1   |            |
|  |         |       | 0                      |                        | Pin 109 (0)   |            |
| 23[8]  | 52[3]   | R/W   | PHY_TEST_PIN_SETTING_0 | *                      |   |            |
|  |         |       | Default Value          |                        |   |            |
|  |         |       | TEST2=0                |                        | TEST2=1   |            |
|  |         |       | 0                      |                        | Pin 63 (0)  |            |
| 23[7]  | 52[2]   | R/W   | PHY_TEST_PIN_SETTING_6 | *                      |   |            |
|  |         |       | Default Value          |                        |   |            |
|  |         |       | TEST2=0                |                        | TEST2=1   |            |
|  |         |       | 0                      |                        | Pin 59 (0)  |            |
| 23[6]  | 52[1]   | R/W   | PHY_TEST_PIN_SETTING_1 | *                      |   |            |
|  |         |       | Default Value          |                        |   |            |
|  |         |       | TEST2=0                |                        | TEST2=1   |            |
|  |         |       | 0                      |                        | Pin 80 (0)  |            |
| 23[5:0]  | 53[5:0] | R/W   | TMOD_SEL[5:0]          | *                      |   |            |
|  |         |       | Default Value          |                        |   |            |
|  |         |       | TEST2=0                |                        | TEST2=1   |            |
|  |         |       | 6'b000000              |                        | {pin64(0), pin65(1), pin67(1), pin100(1), pin101(1), pin102(0)} |            |



| PHY   | MII                 | ROM     | R/W   | Description   | Default |         |
|-------|---------------------|---------|---|---|---------|---------|
| 21    | 24[7:2]             | 54[7:2] | R/W   | FLOOD_FRM[5:0]<br>Flood frame for each port                       | 6'h00   |         |
|       | 24[1]               | --      | RO  | FAST<br>Fast mode for simulation,<br>1: Fast mode, 0: normal mode | *       |         |
|       |                     |         |   | Default Value   |         |         |
|       |                     |         |   | TEST2=0   |         | TEST2=1 |
| 0     | Pin 66 FASTMODE (0) |         |   |   |         |         |
| 24[0] | 54[0]               | R/W     | ALLPASS<br>Receive all incoming frame with error. | 1'b0  |         |         |

### 5.10 CRC Counter

| PHY | MII      | ROM | R/W        | Description   | Default |
|-----|----------|-----|------------|---|---------|
| 21  | 25[15:8] |     |            | RESERVED  |         |
|     | 25 [7:0] | --  | RO<br>(SC) | CRC_COUNTER[7:0]<br>CRC counter which accumulates the CRC number of all ports.<br>Any port received a frame with CRC error will increase this counter by 1.<br>Self-clear after read. | 8'h00   |

### 5.11 VLAN Group Control Register

#### 5.11.1 VLAN Classification

| PHY | MII      | ROM     | R/W         | Description   | Default |
|-----|----------|---------|-------------|---|---------|
| 22  | 0[15]    | --      | R/W<br>(SC) | VLAN_TABLE_CLR<br>Clear the contents of VLAN TABLE register<br>1: clear register<br>0: do nothing (default)<br>Self-clear after set and register cleared  | 1'b0    |
|     | 0[14]    |         |             | RESERVED  |         |
|     | 0[13:12] | 55[7:6] | R/W         | UNVID_MODE[1:0]<br>Unknown-VID Mode<br>2'b00 : discard<br>2'b01 : forward to CPU<br>2'b10 : flood packet<br>2'b11 : reserved  | 2'b00   |
|     | 0[11:6]  | 55[5:0] | R/W         | VLAN_CLS[5:0]<br>VLAN Classification associated with each port<br>Only active at tagged-based VLAN<br>0 : use VID to classify VLAN<br>-use VID to search VLAN table if tag packet<br>-use PVID to search VLAN table if untag packet<br>1 : use PVID to classify VLAN<br>-always use PVID to search VLAN table | 6'h00   |



| PHY | MII    | ROM     | R/W | Description   | Default |
|-----|--------|---------|-----|---|---------|
|     | 0[5:0] | 56[5:0] | R/W | VLAN_MODE[5:0]<br>VLAN Mode setting associated with each port<br>0 : Port-based VLAN (default)<br>1 : Tagged-based VLAN | 6'h00   |

### 5.11.2 VLAN Ingress Rule

| PHY    | MII   | ROM     | R/W  | Description  | Default |   |
|--------|---|---------|--|--|---------|---|
| 22     | 1[15:12]  |         |  | RESERVED   |         |   |
|        | 1[11]   | 57[3]   | R/W  | VLAN_DROP_CFI<br>Drop incoming frame, if the CFI field is not equal to zero. | 1'b0    |   |
|        | 1[10:8]   | 57[2:0] | R/W  | RSVD_VID[2:0]<br>Reserved VID  | 3'b100  |   |
|        |   |         |  | Bit 0  |         | The null VID. If set, frames with null VID (priority-tagged frame) treat as untagged frames.<br>0: disable (default)<br>1: enable |
|        |   |         |  | Bit 1  |         | VID=1 (default VID)<br>Replace default VID with PVID<br>0: disable (default)<br>1: enable   |
| Bit 2  | VID=FFF<br>Discard frame if the VID is the value FFF<br>0: disable<br>1: enable (default) |         |  |  |         |   |
| 1[7:6] | 58[7:6]   | R/W     | ACCEPTABLE_FRM_TYPE[1:0]<br>Acceptable Frame Type<br><br>2'b00 Admit all frames (default)<br>2'b01 Admit VLAN-tagged frames<br>2'b10 Admit Untagged frames<br>2'b11 Reserved   | 2'b00  |         |   |
| 1[5:0] | 58[5:0]   | R/W     | VLAN_INGRESS_FILTER[5:0]<br>VLAN Ingress Filter associated with each port<br>If ingress filter for a given port is set, frame shall discard on that port whose VLAN classification does not include that port in its member set. | 6'h3F  |         |   |

### 5.11.3 VLAN Egress Rule

| PHY        | MII        | ROM     | R/W | Description  | Default |
|------------|------------|---------|-----|--|---------|
| 22         | 2[15:12]   |         |     | RESERVED   |         |
|            | 2[11:6]    | 59[5:0] | R/W | IGMP_IGNORE_MEMBER[5:0]<br>IGMP Ignore member set<br>Ignore member set for frame with DMAC inside<br>01-00-5e-xx-xx-xx | *       |
|            |            |         |     | Default Value  |         |
|            |            |         |     | HW_IGMP_EN = 1   |         |
| 6'b10_0000 | 6'b00_0000 |         |     |  |         |

| PHY | MII    | ROM     | R/W | Description   | Default |
|-----|--------|---------|-----|---|---------|
|     | 2[5:0] | 60[5:0] | R/W | KEEP_TAG[5:0] (QinQ register)<br>Keep VLAN Tag Header<br>0: Disabled<br>1: Keep VLAN tag header from frame. If frames transmission on a egress port tags frame, the frame may contain two tag headers | 6'h00   |

**5.11.4 Default VLAN Information**

| PHY | MII     | ROM                | R/W | Description                                  | Default  |
|-----|---------|--------------------|-----|--|----------|
| 22  | 3[15:0] | 62[7:0]<br>61[7:0] | R/W | TPID_VALUE[15:0]<br>802.1Q Tag Protocol Type | 16'h8100 |

| PHY | MII     | ROM                | R/W | Description  | Default  |
|-----|---------|--------------------|-----|--|----------|
| 22  | 4[15:0] | 64[7:0]<br>63[7:0] | R/W | VLAN_INFO_0.<br>Port 0 default VLAN information value (PVID_0) | 16'h0001 |
|     | 5[15:0] | 66[7:0]<br>65[7:0] | R/W | VLAN_INFO_1.<br>Port 1 default VLAN information value (PVID_1) | 16'h0001 |
|     | 6[15:0] | 68[7:0]<br>67[7:0] | R/W | VLAN_INFO_2.<br>Port 2 default VLAN information value (PVID_2) | 16'h0001 |
|     | 7[15:0] | 70[7:0]<br>69[7:0] | R/W | VLAN_INFO_3.<br>Port 3 default VLAN information value (PVID_3) | 16'h0001 |
|     | 8[15:0] | 72[7:0]<br>71[7:0] | R/W | VLAN_INFO_4.<br>Port 4 default VALN information value (PVID_4) | 16'h0001 |
|     | 9[15:0] | 74[7:0]<br>73[7:0] | R/W | VLAN_INFO_5.<br>Port 5 default VALN information value (PVID_5) | 16'h0001 |

### 5.11.5 VLAN Table

#### 5.11.5.1 VLAN Control Register

| PHY | MII      | ROM                | R/W | Description   | Default      |
|-----|----------|--------------------|-----|---|--------------|
| 22  | 10[15:0] | 76[7:0]<br>75[7:0] | R/W | VLAN_VALID[15:0]<br>VLAN filter is valid.<br>The VLAN filter entry X is valid associated with the VID_X.                                      | 16'h<br>0000 |
|     | 11[15:0] | 78[7:0]<br>77[7:0] | R/W | QU_NUM_EN[15:0]<br>Assign new queue number enable<br>Assign a new queue number which defined in PRI_NUM_X register associated with the VID_X. | 16'h00<br>00 |
|     | 12[15:0] | 80[7:0]<br>79[7:0] | R/W | STP_IDX_EN[15:0]<br>Spanning Tree Protocol Index Enable   | 16'h00<br>00 |
|     | 13[15:0] | 82[7:0]<br>81[7:0] | R/W | REW_VLAN_PRI_EN[15:0]<br>Re-write VLAN priority field Enable  | 16'h00<br>00 |

#### 5.11.5.2 VLAN Identifier Register

| PHY | MII       | ROM                | R/W | Description   | Default |
|-----|-----------|--------------------|-----|---|---------|
| 22  | 14[15:12] | 84[7:4]            | R/W | FID_0[3:0]<br>VLAN field identifier associated with VALN 0. | 4'h0    |
|     | 14[11:0]  | 84[3:0]<br>83[7:0] | R/W | VID_0[11:0]<br>VLAN identifier associated with VALN 0.      | 12'h001 |
|     | 15[15:12] | 86[7:4]            | R/W | FID_1[3:0]<br>VLAN field identifier associated with VALN 1. | 4'h0    |
|     | 15[11:0]  | 86[3:0]<br>85[7:4] | R/W | VID_1[11:0]<br>VLAN identifier associated with VALN 1.      | 12'h002 |
|     | 16[15:12] | 88[7:4]            | R/W | FID_2[3:0]<br>VLAN field identifier associated with VALN 2. | 4'h0    |
|     | 16[11:0]  | 88[3:0]<br>87[7:0] | R/W | VID_2[11:0]<br>VLAN identifier associated with VALN 2.      | 12'h003 |
|     | 17[15:12] | 90[7:4]            | R/W | FID_3[3:0]<br>VLAN field identifier associated with VALN 3. | 4'h0    |
|     | 17[11:0]  | 90[3:0]<br>89[7:0] | R/W | VID_3[11:0]<br>VLAN identifier associated with VALN 3.      | 12'h004 |
|     | 18[15:12] | 92[7:4]            | R/W | FID_4[3:0]<br>VLAN field identifier associated with VALN 4. | 4'h0    |
|     | 18[11:0]  | 92[3:0]<br>91[7:0] | R/W | VID_4[11:0]<br>VLAN identifier associated with VALN 4.      | 12'h005 |
|     | 19[15:12] | 94[7:4]            | R/W | FID_5[3:0]<br>VLAN field identifier associated with VALN 5. | 4'h0    |
|     | 19[11:0]  | 94[3:0]<br>93[7:0] | R/W | VID_5[11:0]<br>VLAN identifier associated with VALN 5.      | 12'h006 |
|     | 20[15:12] | 96[7:4]            | R/W | FID_6[3:0]<br>VLAN field identifier associated with VALN 6. | 4'h0    |
|     | 20[11:0]  | 96[3:0]<br>95[7:0] | R/W | VID_6[11:0]<br>VLAN identifier associated with VALN 6.      | 12'h007 |
|     | 21[15:12] | 98[7:4]            | R/W | FID_7[3:0]<br>VLAN field identifier associated with VALN 7. | 4'h0    |



| PHY | MII       | ROM                  | R/W | Description   | Default |
|-----|-----------|----------------------|-----|---|---------|
|     | 21[11:0]  | 98[3:0]<br>97[7:0]   | R/W | VID_7[11:0]<br>VLAN identifier associated with VALN 7.      | 12'h008 |
|     | 22[15:12] | 100[7:4]             | R/W | FID_8[3:0]<br>VLAN field identifier associated with VALN 8. | 4'h0    |
|     | 22[11:0]  | 100[3:0]<br>99[7:0]  | R/W | VID_8[11:0]<br>VLAN identifier associated with VALN 8.      | 12'h009 |
|     | 23[15:12] | 102[7:4]             | R/W | FID_9[3:0]<br>VLAN field identifier associated with VALN 9. | 4'h0    |
|     | 23[11:0]  | 102[3:0]<br>101[7:0] | R/W | VID_9[11:0]<br>VLAN identifier associated with VALN 9.      | 12'h00A |
| 22  | 24[15:12] | 104[7:4]             | R/W | FID_A[3:0]<br>VLAN field identifier associated with VALN A. | 4'h0    |
|     | 24[11:0]  | 104[3:0]<br>103[7:0] | R/W | VID_A[11:0]<br>VLAN identifier associated with VALN A.      | 12'h00B |
|     | 25[15:12] | 106[7:4]             | R/W | FID_B[3:0]<br>VLAN field identifier associated with VALN B. | 4'h0    |
|     | 25[11:0]  | 105[3:0]<br>105[7:0] | R/W | VID_B[11:0]<br>VLAN identifier associated with VALN B.      | 12'h00C |
|     | 26[15:12] | 108[7:4]             | R/W | FID_C[3:0]<br>VLAN field identifier associated with VALN C. | 4'h0    |
|     | 26[11:0]  | 108[3:0]<br>107[7:0] | R/W | VID_C[11:0]<br>VLAN identifier associated with VALN C.      | 12'h00D |
|     | 27[15:12] | 110[7:4]             | R/W | FID_D[3:0]<br>VLAN field identifier associated with VALN D. | 4'h0    |
|     | 27[11:0]  | 110[3:0]<br>109[7:0] | R/W | VID_D[11:0]<br>VLAN identifier associated with VALN D.      | 12'h00E |
|     | 28[15:12] | 112[7:4]             | R/W | FID_E[3:0]<br>VLAN field identifier associated with VALN E. | 4'h0    |
|     | 28[11:0]  | 112[3:0]<br>111[7:0] | R/W | VID_E[11:0]<br>VLAN identifier associated with VALN E.      | 12'h00F |
|     | 29[15:12] | 114[7:4]             | R/W | FID_F[3:0]<br>VLAN field identifier associated with VALN F. | 4'h0    |
|     | 29[11:0]  | 114[3:0]<br>113[7:0] | R/W | VID_F[11:0]<br>VLAN identifier associated with VALN F.      | 12'h010 |

### 5.11.5.3 VLAN Member Register

| PHY | MII     | ROM      | R/W | Description   | Default |
|-----|---------|----------|-----|---|---------|
| 23  | 0[5:0]  | 115[5:0] | R/W | VLAN_MEMBER_0[5:0]<br>VLAN member port<br>VLAN member port associated with the VID_0. | 6'h3F   |
|     | 0[13:8] | 116[5:0] | R/W | VLAN_MEMBER_1[5:0]<br>VLAN member port<br>VLAN member port associated with the VID_1. | 6'h3F   |
|     | 1[5:0]  | 117[5:0] | R/W | VLAN_MEMBER_2[5:0]<br>VLAN member port<br>VLAN member port associated with the VID_2. | 6'h3F   |



| PHY | MII     | ROM      | R/W | Description   | Default |
|-----|---------|----------|-----|---|---------|
|     | 1[13:8] | 118[5:0] | R/W | VLAN_MEMBER_3[5:0]<br>VLAN member port<br>VLAN member port associated with the VID_3. | 6'h3F   |
|     | 2[5:0]  | 119[5:0] | R/W | VLAN_MEMBER_4[5:0]<br>VLAN member port<br>VLAN member port associated with the VID_4. | 6'h3F   |
|     | 2[13:8] | 120[5:0] | R/W | VLAN_MEMBER_5[5:0]<br>VLAN member port<br>VLAN member port associated with the VID_5. | 6'h3F   |
| 23  | 3[5:0]  | 121[5:0] | R/W | VLAN_MEMBER_6[5:0]<br>VLAN member port<br>VLAN member port associated with the VID_6. | 6'h00   |
|     | 3[13:8] | 122[5:0] | R/W | VLAN_MEMBER_7[5:0]<br>VLAN member port<br>VLAN member port associated with the VID_7. | 6'h00   |
|     | 4[5:0]  | 123[5:0] | R/W | VLAN_MEMBER_8[5:0]<br>VLAN member port<br>VLAN member port associated with the VID_8. | 6'h00   |
|     | 4[13:8] | 124[5:0] | R/W | VLAN_MEMBER_9[5:0]<br>VLAN member port<br>VLAN member port associated with the VID_9. | 6'h00   |
|     | 5[5:0]  | 125[5:0] | R/W | VLAN_MEMBER_A[5:0]<br>VLAN member port<br>VLAN member port associated with the VID_A. | 6'h00   |
|     | 5[13:8] | 126[5:0] | R/W | VLAN_MEMBER_B[5:0]<br>VLAN member port<br>VLAN member port associated with the VID_B. | 6'h00   |
|     | 6[5:0]  | 127[5:0] | R/W | VLAN_MEMBER_C[5:0]<br>VLAN member port<br>VLAN member port associated with the VID_C. | 6'h00   |
|     | 6[13:8] | 128[5:0] | R/W | VLAN_MEMBER_D[5:0]<br>VLAN member port<br>VLAN member port associated with the VID_D. | 6'h00   |
|     | 7[5:0]  | 129[5:0] | R/W | VLAN_MEMBER_E[5:0]<br>VLAN member port<br>VLAN member port associated with the VID_E. | 6'h00   |
|     | 7[13:8] | 130[5:0] | R/W | VLAN_MEMBER_F[5:0]<br>VLAN member port<br>VLAN member port associated with the VID_F. | 6'h00   |

5.11.5.4 Add Tag Control Register

| PHY | MII      | ROM      | R/W | Description   | Default       |   |
|-----|----------|----------|-----|---|---------------|---|
| 23  | 8[5:0]   | 131[5:0] | R/W | ADD_TAG_0[5:0]<br>Add VLAN tag<br>Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_0. | 6'b<br>000000 |   |
|     |          |          |     | Bit 0   |               | 1: port 0 adds a VLAN tag to each outgoing packet.<br>0: port 0 doesn't add a VLAN tag. |
|     |          |          |     | Bit 1   |               | 1: port 1 adds a VLAN tag to each outgoing packet.<br>0: port 1 doesn't add a VLAN tag. |
|     |          |          |     | Bit 2   |               | 1: port 2 adds a VLAN tag to each outgoing packet.<br>0: port 2 doesn't add a VLAN tag. |
|     |          |          |     | Bit 3   |               | 1: port 3 adds a VLAN tag to each outgoing packet.<br>0: port 3 doesn't add a VLAN tag. |
|     |          |          |     | Bit 4   |               | 1: port 4 adds a VLAN tag to each outgoing packet.<br>0: port 4 doesn't add a VLAN tag. |
|     |          |          |     | Bit 5   |               | 1: port 5 adds a VLAN tag to each outgoing packet.<br>0: port 5 doesn't add a VLAN tag. |
| 23  | 8[13:8]  | 132[5:0] | R/W | ADD_TAG_1[5:0]<br>Add VLAN tag<br>Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_1. | 6'b<br>000000 |   |
|     | 9[5:0]   | 133[5:0] | R/W | ADD_TAG_2[5:0]<br>Add VLAN tag<br>Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_2. | 6'b<br>000000 |   |
|     | 9[13:8]  | 134[5:0] | R/W | ADD_TAG_3[5:0]<br>Add VLAN tag<br>Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_3. | 6'b<br>000000 |   |
|     | 10[5:0]  | 135[5:0] | R/W | ADD_TAG_4[5:0]<br>Add VLAN tag<br>Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_4. | 6'b<br>000000 |   |
|     | 10[13:8] | 136[5:0] | R/W | ADD_TAG_5[5:0]<br>Add VLAN tag<br>Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_5. | 6'b<br>000000 |   |
|     | 11[5:0]  | 137[5:0] | R/W | ADD_TAG_6[5:0]<br>Add VLAN tag<br>Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_6. | 6'b<br>000000 |   |
|     | 11[13:8] | 138[5:0] | R/W | ADD_TAG_7[5:0]<br>Add VLAN tag<br>Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_7. | 6'b<br>000000 |   |



| PHY | MII      | ROM      | R/W | Description   | Default       |
|-----|----------|----------|-----|---|---------------|
|     | 12[5:0]  | 139[5:0] | R/W | ADD_TAG_8[5:0]<br>Add VLAN tag<br>Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_8. | 6'b<br>000000 |
|     | 12[13:8] | 140[5:0] | R/W | ADD_TAG_9[5:0]<br>Add VLAN tag<br>Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_9. | 6'b<br>000000 |
|     | 13[5:0]  | 141[5:0] | R/W | ADD_TAG_A[5:0]<br>Add VLAN tag<br>Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_A. | 6'b<br>000000 |
|     | 13[13:8] | 142[5:0] | R/W | ADD_TAG_B[5:0]<br>Add VLAN tag<br>Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_B. | 6'b<br>000000 |
| 23  | 14[5:0]  | 143[5:0] | R/W | ADD_TAG_C[5:0]<br>Add VLAN tag<br>Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_C. | 6'b<br>000000 |
|     | 14[13:8] | 144[5:0] | R/W | ADD_TAG_D[5:0]<br>Add VLAN tag<br>Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_D. | 6'b<br>000000 |
|     | 15[5:0]  | 145[5:0] | R/W | ADD_TAG_E[5:0]<br>Add VLAN tag<br>Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_E. | 6'b<br>000000 |
|     | 15[13:8] | 146[5:0] | R/W | ADD_TAG_F[5:0]<br>Add VLAN tag<br>Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_F. | 6'b<br>000000 |

#### 5.11.5.5 Remove Tag Control Register

| PHY | MII     | ROM      | R/W | Description  | Default       |
|-----|---------|----------|-----|--|---------------|
| 23  | 16[5:0] | 147[5:0] | R/W | REMOVE_TAG_0[5:0]<br>Remove VLAN tag<br>Port Y removes VLAN tag to each outgoing packet associated with the VID_0.                 | 6'b<br>000000 |
|     |         |          |     | Bit 0<br>1: port 0 removes the VLAN tag of each outgoing packet.<br>0: port 0 doesn't remove the VLAN tag of each outgoing packet. |               |
|     |         |          |     | Bit 1<br>1: port 1 removes the VLAN tag of each outgoing packet.<br>0: port 1 doesn't remove the VLAN tag of each outgoing packet. |               |
|     |         |          |     | Bit 2<br>1: port 2 removes the VLAN tag of each outgoing packet.<br>0: port 2 doesn't remove the VLAN tag of each outgoing packet. |               |
|     |         |          |     | Bit 3<br>1: port 3 removes the VLAN tag of each outgoing packet.<br>0: port 3 doesn't remove the VLAN tag of each outgoing packet. |               |
|     |         |          |     | Bit 4<br>1: port 4 removes the VLAN tag of each outgoing packet.<br>0: port 4 doesn't remove the VLAN tag of each outgoing packet. |               |



| PHY | MII      | ROM      | R/W | Description  | Default       |
|-----|----------|----------|-----|--|---------------|
|     |          |          |     | Bit 5<br>1: port 5 removes the VLAN tag of each outgoing packet.<br>0: port 5 doesn't remove the VLAN tag of each outgoing packet. |               |
|     | 16[13:8] | 148[5:0] | R/W | REMOVE_TAG_1[5:0]<br>Remove VLAN tag<br>Port Y removes VLAN tag to each outgoing packet associated with the VID_1.                 | 6'b<br>000000 |
|     | 17[5:0]  | 149[5:0] | R/W | REMOVE_TAG_2[5:0]<br>Remove VLAN tag<br>Port Y removes VLAN tag to each outgoing packet associated with the VID_2.                 | 6'b<br>000000 |
|     | 17[13:8] | 150[5:0] | R/W | REMOVE_TAG_3[5:0]<br>Remove VLAN tag<br>Port Y removes VLAN tag to each outgoing packet associated with the VID_3.                 | 6'b<br>000000 |
|     | 18[5:0]  | 151[5:0] | R/W | REMOVE_TAG_4[5:0]<br>Remove VLAN tag<br>Port Y removes VLAN tag to each outgoing packet associated with the VID_4.                 | 6'b<br>000000 |
|     | 18[13:8] | 152[5:0] | R/W | REMOVE_TAG_5[5:0]<br>Remove VLAN tag<br>Port Y removes VLAN tag to each outgoing packet associated with the VID_5.                 | 6'b<br>000000 |
|     | 19[5:0]  | 153[5:0] | R/W | REMOVE_TAG_6[5:0]<br>Remove VLAN tag<br>Port Y removes VLAN tag to each outgoing packet associated with the VID_6.                 | 6'b<br>000000 |
|     | 19[13:8] | 154[5:0] | R/W | REMOVE_TAG_7[5:0]<br>Remove VLAN tag<br>Port Y removes VLAN tag to each outgoing packet associated with the VID_7.                 | 6'b<br>000000 |
|     | 20[5:0]  | 155[5:0] | R/W | REMOVE_TAG_8[5:0]<br>Remove VLAN tag<br>Port Y removes VLAN tag to each outgoing packet associated with the VID_8.                 | 6'b<br>000000 |
|     | 20[13:8] | 156[5:0] | R/W | REMOVE_TAG_9[5:0]<br>Remove VLAN tag<br>Port Y removes VLAN tag to each outgoing packet associated with the VID_9.                 | 6'b<br>000000 |
|     | 21[5:0]  | 157[5:0] | R/W | REMOVE_TAG_A[5:0]<br>Remove VLAN tag<br>Port Y removes VLAN tag to each outgoing packet associated with the VID_A.                 | 6'b<br>000000 |
|     | 21[13:8] | 158[5:0] | R/W | REMOVE_TAG_B[5:0]<br>Remove VLAN tag<br>Port Y removes VLAN tag to each outgoing packet associated with the VID_B.                 | 6'b<br>000000 |

| PHY | MII      | ROM      | R/W | Description  | Default       |
|-----|----------|----------|-----|--|---------------|
|     | 22[5:0]  | 159[5:0] | R/W | REMOVE_TAG_C[5:0]<br>Remove VLAN tag<br>Port Y removes VLAN tag to each outgoing packet associated with the VID_C. | 6'b<br>000000 |
|     | 22[13:8] | 160[5:0] | R/W | REMOVE_TAG_D[5:0]<br>Remove VLAN tag<br>Port Y removes VLAN tag to each outgoing packet associated with the VID_D. | 6'b<br>000000 |
|     | 23[5:0]  | 161[5:0] | R/W | REMOVE_TAG_E[5:0]<br>Remove VLAN tag<br>Port Y removes VLAN tag to each outgoing packet associated with the VID_E. | 6'b<br>000000 |
|     | 23[13:8] | 162[5:0] | R/W | REMOVE_TAG_F[5:0]<br>Remove VLAN tag<br>Port Y removes VLAN tag to each outgoing packet associated with the VID_F. | 6'b<br>000000 |

#### 5.11.5.6 VLAN Miscellaneous Register

| PHY | MII      | ROM      | R/W | Description  | Default |  |
|-----|----------|----------|-----|--|---------|--|
| 23  | 24[7:0]  | 163[7:0] | R/W | VLAN_MISC_0[7:0]<br>VLAN Miscellaneous Registers 0 | 8'h00   |  |
|     |          |          |     | Bit 1-0  |         | STP_IDX[1:0]<br>Spanning Tree Index<br>This registers is effective only STP_IDX_EN[0] is enabled                   |
|     |          |          |     | Bit 3-2  |         | QU_NUM[1:0]<br>Priority Queue Number<br>This registers is effective only QU_NUM_EN[0] is enabled                   |
|     |          |          |     | Bit 4  |         | LEARN_DIS<br>Learning Disable  |
|     |          |          |     | Bit 7-5  |         | REW_VLAN_PRI[2:0]<br>Rewrite VLAN priority value<br>This registers is effective only REW_VLAN_PRI_EN[0] is enabled |
|     | 24[15:8] | 164[7:0] | R/W | VLAN_MISC_1[7:0]<br>VLAN Miscellaneous Registers 1 | 8'h00   |  |
|     | 25[7:0]  | 165[7:0] | R/W | VLAN_MISC_2[7:0]<br>VLAN Miscellaneous Registers 2 | 8'h00   |  |
|     | 25[15:8] | 166[7:0] | R/W | VLAN_MISC_3[7:0]<br>VLAN Miscellaneous Registers 3 | 8'h00   |  |
|     | 26[7:0]  | 167[7:0] | R/W | VLAN_MISC_4[7:0]<br>VLAN Miscellaneous Registers 4 | 8'h00   |  |
|     | 26[15:8] | 168[7:0] | R/W | VLAN_MISC_5[7:0]<br>VLAN Miscellaneous Registers 5 | 8'h00   |  |
|     | 27[7:0]  | 169[7:0] | R/W | VLAN_MISC_6[7:0]<br>VLAN Miscellaneous Registers 6 | 8'h00   |  |
|     | 27[15:8] | 170[7:0] | R/W | VLAN_MISC_7[7:0]<br>VLAN Miscellaneous Registers 7 | 8'h00   |  |

| PHY | MII      | ROM      | R/W | Description  | Default |
|-----|----------|----------|-----|--|---------|
|     | 28[7:0]  | 171[7:0] | R/W | VLAN_MISC_8[7:0]<br>VLAN Miscellaneous Registers 8 | 8'h00   |
|     | 28[15:8] | 172[7:0] | R/W | VLAN_MISC_9[7:0]<br>VLAN Miscellaneous Registers 9 | 8'h00   |
|     | 29[7:0]  | 173[7:0] | R/W | VLAN_MISC_A[7:0]<br>VLAN Miscellaneous Registers A | 8'h00   |
|     | 29[15:8] | 174[7:0] | R/W | VLAN_MISC_B[7:0]<br>VLAN Miscellaneous Registers B | 8'h00   |
|     | 30[7:0]  | 175[7:0] | R/W | VLAN_MISC_C[7:0]<br>VLAN Miscellaneous Registers C | 8'h00   |
| 23  | 30[15:8] | 176[7:0] | R/W | VLAN_MISC_D[7:0]<br>VLAN Miscellaneous Registers D | 8'h00   |
|     | 31[7:0]  | 177[7:0] | R/W | VLAN_MISC_E[7:0]<br>VLAN Miscellaneous Registers E | 8'h00   |
|     | 31[15:8] | 178[7:0] | R/W | VLAN_MISC_F[7:0]<br>VLAN Miscellaneous Registers F | 8'h00   |

#### 5.11.5.7 Spanning Tree Table

| PHY | MII     | ROM      | R/W | Description  | Default   |
|-----|---------|----------|-----|--|-----------|
| 24  | 0[13:8] | 179[5:0] | R/W | STP_FORWARD_EN_0[5:0]<br>Spanning Tree packet Forwarding capability for each port associate with STP_IDX | 6'b111111 |
|     | 0[5:0]  | 180[5:0] | R/W | STP_LEARNING_EN_0[5:0]<br>Spanning Tree packet Learning capability for each port associate with STP_IDX  | 6'b111111 |
|     | 1[13:8] | 181[5:0] | R/W | STP_FORWARD_EN_1[5:0]<br>Spanning Tree packet Forwarding capability for each port associate with STP_IDX | 6'b111111 |
|     | 1[5:0]  | 182[5:0] | R/W | STP_LEARNING_EN_1[5:0]<br>Spanning Tree packet Learning capability for each port associate with STP_IDX  | 6'b111111 |
|     | 2[13:8] | 183[5:0] | R/W | STP_FORWARD_EN_2[5:0]<br>Spanning Tree packet Forwarding capability for each port associate with STP_IDX | 6'b111111 |
|     | 2[5:0]  | 184[5:0] | R/W | STP_LEARNING_EN_2[5:0]<br>Spanning Tree packet Learning capability for each port associate with STP_IDX  | 6'b111111 |
|     | 3[13:8] | 185[5:0] | R/W | STP_FORWARD_EN_3[5:0]<br>Spanning Tree packet Forwarding capability for each port associate with STP_IDX | 6'b111111 |
|     | 3[5:0]  | 186[5:0] | R/W | STP_LEARNING_EN_3[5:0]<br>Spanning Tree packet Learning capability for each port associate with STP_IDX  | 6'b111111 |

## 5.12 Quality of Service (QOS)

### 5.12.1 Priority Classification

#### 5.12.1.1 Base Control Register

| PHY    | MII      | ROM                  | R/W   | Description  | Default  |                    |       |
|--------|----------|----------------------|---|--|--|--------------------|-------|
| 25     | 0[15]    | 187[7]               | R/W   | LP_OVER_DSCP<br>Logical port takes a high precedence than DSCP priority.   | 1'b0   |                    |       |
|        | 0[14]    | 187[6]               | R/W   | TOS_OVER_VLAN_PRI<br>IP frame take a higher precedence than VLAN priority. That is the IP frame's priority is over the frame with VLAN tagged. | 1'b0   |                    |       |
|        | 0[13:8]  | 187[5:0]             | R/W   | COS_EN[5:0]<br>Class of service enable for each port<br>1: enable<br>0: disabled (default)<br>Default Value                                    | *  |                    |       |
|        | TEST2=0  |                      | TEST2=1   |  |  |                    |       |
|        | P4EXT=1  | P4EXT=0              |   | 6'h00  |  |                    |       |
|        | 6'h00    | Pin63 COS_EN (6'h00) |   |  |  |                    |       |
|        | 0[7]     | 188[7]               | R/W   | USER_DEF_PRI<br>User Define Priority   | 1'b0   |                    |       |
| 0[6]   |          |                      | RESERVED  |  |  |                    |       |
| 0[5:0] | 188[5:0] | R/W                  | PORT_PRI_EN[5:0]<br>Port based priority function enable control registers for each port.<br>Default Value | *  |  |                    |       |
|        |          |                      | TEST2=0   |  | TEST2=1  |                    |       |
|        |          |                      | P4EXT=1   |  | P4EXT=0  |                    | 6'h00 |
|        |          |                      | 6'h00   |  | HPPS_EN=1<br>(HPPS1,HPPS0)<br>2'b00: cos_en=6'h10<br>2'b01: cos_en=6'h03<br>2'b10: cos_en=6'h18<br>2'b11: cos_en=6'h01 | HPPS_EN=0<br>6'h00 |       |
|        |          |                      |   |  |  |                    |       |

#### 5.12.1.2 Port Priority Map

| PHY | MII    | ROM      | R/W | Description  | Default |
|-----|--------|----------|-----|--|---------|
| 25  | 1[1:0] | 189[1:0] | R/W | P0_PRI[1:0]<br>Port 0 port-based priority output queue number.<br>00: assign packets to queue 0<br>01: assign packets to queue 1<br>10: assign packets to queue 2<br>11: assign packets to queue 3 (default) | 2'b11   |

|    |          |          |     |  |       |
|----|----------|----------|-----|--|-------|
|    | 1[3:2]   | 189[3:2] | R/W | P1_PRI[1:0]<br>Port 1 port-based priority output queue number.<br>00: assign packets to queue 0<br>01: assign packets to queue 1<br>10: assign packets to queue 2<br>11: assign packets to queue 3 (default) | 2'b11 |
|    | 1[5:4]   | 189[5:4] | R/W | P2_PRI[1:0]<br>Port 2 port-based priority output queue number.<br>00: assign packets to queue 0<br>01: assign packets to queue 1<br>10: assign packets to queue 2<br>11: assign packets to queue 3 (default) | 2'b11 |
|    | 1[7:6]   | 189[7:6] | R/W | P3_PRI[1:0]<br>Port 3 port-based priority output queue number.<br>00: assign packets to queue 0<br>01: assign packets to queue 1<br>10: assign packets to queue 2<br>11: assign packets to queue 3 (default) | 2'b11 |
| 25 | 1[9:8]   | 190[1:0] | R/W | P4_PRI[1:0]<br>Port 4 port-based priority output queue number.<br>00: assign packets to queue 0<br>01: assign packets to queue 1<br>10: assign packets to queue 2<br>11: assign packets to queue 3 (default) | 2'b11 |
|    | 1[11:10] | 190[3:2] | R/W | P5_PRI[1:0]<br>Port 0 port-based priority output queue number.<br>00: assign packets to queue 0<br>01: assign packets to queue 1<br>10: assign packets to queue 2<br>11: assign packets to queue 3 (default) | 2'b11 |

### 5.12.1.3 VLAN Priority Map

| PHY | MII      | ROM      | R/W | Description   | Default |
|-----|----------|----------|-----|---|---------|
| 25  | 2[15:14] | 191[7:6] | R/W | VLAN_PRI7<br>Priority map when the VLAN priority is 7 | 2'b00   |
|     | 2[13:12] | 191[5:4] | R/W | VLAN_PRI6<br>Priority map when the VLAN priority is 6 | 2'b00   |
|     | 2[11:10] | 191[3:2] | R/W | VLAN_PRI5<br>Priority map when the VLAN priority is 5 | 2'b00   |
|     | 2[9:8]   | 191[1:0] | R/W | VLAN_PRI4<br>Priority map when the VLAN priority is 4 | 2'b00   |
|     | 2[7:6]   | 192[7:6] | R/W | VLAN_PRI3<br>Priority map when the VLAN priority is 3 | 2'b00   |
|     | 2[5:4]   | 192[5:4] | R/W | VLAN_PRI2<br>Priority map when the VLAN priority is 2 | 2'b00   |
|     | 2[3:2]   | 192[3:2] | R/W | VLAN_PRI1<br>Priority map when the VLAN priority is 1 | 2'b00   |
|     | 2[1:0]   | 192[1:0] | R/W | VLAN_PRI0<br>Priority map when the VLAN priority is 0 | 2'b00   |



5.12.1.4 TOS/DSCP Priority Map

| PHY      | MII      | ROM      | R/W      | Description   | Default   |
|----------|----------|----------|----------|---|---|
| 25       | 3[15:14] | 193[7:6] | R/W      | DSCP_7<br>Priority map when the DSCP field is 7               | 2'b00   |
|          | 3[13:12] | 193[5:4] | R/W      | DSCP_6<br>Priority map when the DSCP field is 6               | 2'b00   |
|          | 3[11:10] | 193[3:2] | R/W      | DSCP_5<br>Priority map when the DSCP field is 5               | 2'b00   |
|          | 3[9:8]   | 193[1:0] | R/W      | DSCP_4<br>Priority map when the DSCP field is 4               | 2'b00   |
|          | 3[7:6]   | 194[7:6] | R/W      | DSCP_3<br>Priority map when the DSCP field is 3               | 2'b00   |
|          | 3[5:4]   | 194[5:4] | R/W      | DSCP_2<br>Priority map when the DSCP field is 2               | 2'b00   |
|          | 3[3:2]   | 194[3:2] | R/W      | DSCP_1<br>Priority map when the DSCP field is 1               | 2'b00   |
|          | 3[1:0]   | 194[1:0] | R/W      | DSCP_0 (Best Effort)<br>Priority map when the DSCP field is 0 | 2'b00   |
|          | 4[15:14] | 195[7:6] | R/W      | DSCP_F<br>Priority map when the DSCP field is F               | 2'b00   |
|          | 4[13:12] | 195[5:4] | R/W      | DSCP_E (AF13)<br>Priority map when the DSCP field is E        | 2'b00   |
|          | 4[11:10] | 195[3:2] | R/W      | DSCP_D<br>Priority map when the DSCP field is D               | 2'b00   |
|          | 4[9:8]   | 195[1:0] | R/W      | DSCP_C (AF12)<br>Priority map when the DSCP field is C        | 2'b00   |
|          | 25       | 4[7:6]   | 196[7:6] | R/W   | DSCP_B<br>Priority map when the DSCP field is B |
| 4[5:4]   |          | 196[5:4] | R/W      | DSCP_A (AF11)<br>Priority map when the DSCP field is A        | 2'b11   |
| 4[3:2]   |          | 196[3:2] | R/W      | DSCP_9<br>Priority map when the DSCP field is 9               | 2'b00   |
| 4[1:0]   |          | 196[1:0] | R/W      | DSCP_8 (CS1)<br>Priority map when the DSCP field is 8         | 2'b00   |
| 5[15:14] |          | 197[7:6] | R/W      | DSCP_17<br>Priority map when the DSCP field is 17             | 2'b00   |
| 5[13:12] |          | 197[5:4] | R/W      | DSCP_16 (AF23)<br>Priority map when the DSCP field is 16      | 2'b00   |
| 5[11:10] |          | 197[3:2] | R/W      | DSCP_15<br>Priority map when the DSCP field is 15             | 2'b00   |
| 5[9:8]   |          | 197[1:0] | R/W      | DSCP_14 (AF22)<br>Priority map when the DSCP field is 14      | 2'b00   |
| 5[7:6]   |          | 198[7:6] | R/W      | DSCP_13<br>Priority map when the DSCP field is 13             | 2'b00   |
| 5[5:4]   |          | 198[5:4] | R/W      | DSCP_12 (AF21)<br>Priority map when the DSCP field is 12      | 2'b11   |



|    |          |          |     |  |       |
|----|----------|----------|-----|--|-------|
|    | 5[3:2]   | 198[3:2] | R/W | DSCP_11<br>Priority map when the DSCP field is 11        | 2'b00 |
|    | 5[1:0]   | 198[1:0] | R/W | DSCP_10 (CS2)<br>Priority map when the DSCP field is 10  | 2'b00 |
|    | 6[15:14] | 199[7:6] | R/W | DSCP_1F<br>Priority map when the DSCP field is 1F        | 2'b00 |
|    | 6[13:12] | 199[5:4] | R/W | DSCP_1E (AF33)<br>Priority map when the DSCP field is 1E | 2'b00 |
|    | 6[11:10] | 199[3:2] | R/W | DSCP_1D<br>Priority map when the DSCP field is 1D        | 2'b00 |
|    | 6[9:8]   | 199[1:0] | R/W | DSCP_1C (AF32)<br>Priority map when the DSCP field is 1C | 2'b00 |
|    | 6[7:6]   | 200[7:6] | R/W | DSCP_1B<br>Priority map when the DSCP field is 1B        | 2'b00 |
|    | 6[5:4]   | 200[5:4] | R/W | DSCP_1A (AF31)<br>Priority map when the DSCP field is 1A | 2'b11 |
|    | 6[3:2]   | 200[3:2] | R/W | DSCP_19<br>Priority map when the DSCP field is 19        | 2'b00 |
|    | 6[1:0]   | 200[1:0] | R/W | DSCP_18 (CS3)<br>Priority map when the DSCP field is 18  | 2'b00 |
|    | 7[15:14] | 201[7:6] | R/W | DSCP_27<br>Priority map when the DSCP field is 27        | 2'b00 |
|    | 7[13:12] | 201[5:4] | R/W | DSCP_26 (AF43)<br>Priority map when the DSCP field is 26 | 2'b00 |
|    | 7[11:10] | 201[3:2] | R/W | DSCP_25<br>Priority map when the DSCP field is 25        | 2'b00 |
|    | 7[9:8]   | 201[1:0] | R/W | DSCP_24 (AF42)<br>Priority map when the DSCP field is 24 | 2'b00 |
| 25 | 7[7:6]   | 202[7:6] | R/W | DSCP_23<br>Priority map when the DSCP field is 23        | 2'b00 |
|    | 7[5:4]   | 202[5:4] | R/W | DSCP_22 (AF41)<br>Priority map when the DSCP field is 22 | 2'b11 |
|    | 7[3:2]   | 202[3:2] | R/W | DSCP_21<br>Priority map when the DSCP field is 21        | 2'b00 |
|    | 7[1:0]   | 202[1:0] | R/W | DSCP_20 (CS4)<br>Priority map when the DSCP field is 20  | 2'b00 |
|    | 8[15:14] | 203[7:6] | R/W | DSCP_2F<br>Priority map when the DSCP field is 2F        | 2'b00 |
|    | 8[13:12] | 203[5:4] | R/W | DSCP_2E (EF)<br>Priority map when the DSCP field is 2E   | 2'b11 |
|    | 8[11:10] | 203[3:2] | R/W | DSCP_2D<br>Priority map when the DSCP field is 2D        | 2'b00 |
|    | 8[9:8]   | 203[1:0] | R/W | DSCP_2C<br>Priority map when the DSCP field is 2C        | 2'b00 |
|    | 8[7:6]   | 204[7:6] | R/W | DSCP_2B<br>Priority map when the DSCP field is 2B        | 2'b00 |





|    |           |          |     |   |       |
|----|-----------|----------|-----|---|-------|
|    | 8[5:4]    | 204[5:4] | R/W | DSCP_2A<br>Priority map when the DSCP field is 2A       | 2'b00 |
|    | 8[3:2]    | 204[3:2] | R/W | DSCP_29<br>Priority map when the DSCP field is 29       | 2'b00 |
|    | 8[1:0]    | 204[1:0] | R/W | DSCP_28 (CS5)<br>Priority map when the DSCP field is 28 | 2'b00 |
|    | 9[15:14]  | 205[7:6] | R/W | DSCP_37<br>Priority map when the DSCP field is 37       | 2'b00 |
|    | 9[13:12]  | 205[5:4] | R/W | DSCP_36<br>Priority map when the DSCP field is 36       | 2'b00 |
|    | 9[11:10]  | 205[3:2] | R/W | DSCP_35<br>Priority map when the DSCP field is 35       | 2'b00 |
|    | 9[9:8]    | 205[1:0] | R/W | DSCP_34<br>Priority map when the DSCP field is 34       | 2'b00 |
|    | 9[7:6]    | 206[7:6] | R/W | DSCP_33<br>Priority map when the DSCP field is 33       | 2'b00 |
|    | 9[5:4]    | 206[5:4] | R/W | DSCP_32<br>Priority map when the DSCP field is 32       | 2'b00 |
|    | 9[3:2]    | 206[3:2] | R/W | DSCP_31<br>Priority map when the DSCP field is 31       | 2'b00 |
|    | 9[1:0]    | 206[1:0] | R/W | DSCP_30 (CS6)<br>Priority map when the DSCP field is 30 | 2'b11 |
|    | 10[15:14] | 207[7:6] | R/W | DSCP_3F<br>Priority map when the DSCP field is 3F       | 2'b00 |
|    | 10[13:12] | 207[5:4] | R/W | DSCP_3E<br>Priority map when the DSCP field is 3E       | 2'b00 |
|    | 10[11:10] | 207[3:2] | R/W | DSCP_3D<br>Priority map when the DSCP field is 3D       | 2'b00 |
| 25 | 10[9:8]   | 207[1:0] | R/W | DSCP_3C<br>Priority map when the DSCP field is 3C       | 2'b00 |
|    | 10[7:6]   | 208[7:6] | R/W | DSCP_3B<br>Priority map when the DSCP field is 3B       | 2'b00 |
|    | 10[5:4]   | 208[5:4] | R/W | DSCP_3A<br>Priority map when the DSCP field is 3A       | 2'b00 |
|    | 10[3:2]   | 208[3:2] | R/W | DSCP_39<br>Priority map when the DSCP field is 39       | 2'b00 |
|    | 10[1:0]   | 208[1:0] | R/W | DSCP_38 (CS7)<br>Priority map when the DSCP field is 38 | 2'b11 |

5.12.1.5 TCP/UDP Port Priority

| PHY       | MII      | ROM                  | R/W                  | Description   | Default   |          |
|-----------|----------|----------------------|----------------------|---|---|----------|
| 25        | 11[15:8] |                      |                      | RESERVED  |   |          |
|           | 11[7:6]  | 209[7:6]             | R/W                  | LP_TYPE<br>Logical Port Type<br>2'b00 – Logic port priority disable<br>2'b01 – Source logic port priority enable<br>2'b10 – Destination logic port priority enable<br>2'b11 – Source or destination logic port priority enable    | 2'b11   |          |
|           | 11[5:4]  | 209[5:4]             | R/W                  | USERDEF_RANGE_EN[1:0]<br>User defined logic port range enable.<br>bit[1]: user define range 1 register enable<br>bit[0]: user define range 0 register enable  | 2'b11   |          |
|           | 11[3:0]  | 209[3:0]             | R/W                  | PREDEF_PORT_EN[3:0]<br>Pre-defined logic port number enable.<br>bit[3]: logic port 3 enable, port 6000<br>bit[2]: logic port 2 enable, port 3389<br>bit[1]: logic port 1 enable, port 443<br>bit[0]: logic port 0 enable, port 22 | 4'hF  |          |
|           | 12[15:0] | 211[7:0]<br>210[7:0] | R/W                  | PREDEF_PORT_0[15:0]<br>Pre-defined logical port 0.<br>The default value is SSH protocol.  | 16'd22  |          |
|           | 13[15:0] | 213[7:0]<br>212[7:0] | R/W                  | PREDEF_PORT_1[15:0]<br>Pre-defined logical port 1.<br>The default value is HTTPs protocol.  | 16'd443   |          |
|           | 14[15:0] | 215[7:0]<br>214[7:0] | R/W                  | PREDEF_PORT_2[15:0]<br>Pre-defined logical port 2.<br>The default value is RDP (Windows Remote Desktop Protocol) protocol.  | 16'd3389  |          |
|           | 15[15:0] | 217[7:0]<br>216[7:0] | R/W                  | PREDEF_PORT_3[15:0]<br>Pre-defined logical port 3.<br>The default value is XWIN protocol.   | 16'd6000  |          |
|           | 16[15:0] | 219[7:0]<br>218[7:0] | R/W                  | USERDEF_RANGE0_LOW<br>User defined logic port range 0 low limit   | 16'd23  |          |
|           | 17[15:0] | 221[7:0]<br>220[7:0] | R/W                  | USERDEF_RANGE0_HIGH<br>User defined logic port range 0 high limit<br>The default value is TELNET protocol.  | 16'd23  |          |
|           | 18[15:0] | 223[7:0]<br>222[7:0] | R/W                  | USERDEF_RANGE1_LOW<br>User defined logic port range 1 low limit   | 16'd5800  |          |
|           | 25       | 19[15:0]             | 225[7:0]<br>224[7:0] | R/W   | USERDEF_RANGE1_HIGH<br>User defined logic port range 1 high limit<br>The default value is VNC protocol. | 16'd5800 |
|           |          | 20[15:12]            |                      |   | RESERVED  |          |
| 20[11:10] |          | 226[3:2]             | R/W                  | USERDEF_RANGE_1Q[1:0]<br>User defined logic port range 1 transmit priority queue mapping.   | 2'b10   |          |
| 20[9:8]   |          | 226[1:0]             | R/W                  | USERDEF_RANGE_0Q[1:0]<br>User defined logic port range 0 transmit priority queue mapping.   | 2'b10   |          |

|          |          |     |  |       |
|----------|----------|-----|--|-------|
| 20[7:6]  | 227[7:6] | R/W | PREDEF_PORT_3Q[1:0]<br>Pre-defined port 3 transmit priority queue mapping.   | 2'b10 |
| 20[5:4]  | 227[5:4] | R/W | PREDEF_PORT_2Q[1:0]<br>Pre-defined port 2 transmit priority queue mapping.   | 2'b10 |
| 20[3:2]  | 227[3:2] | R/W | PREDEF_PORT_1Q[1:0]<br>Pre-defined port 1 transmit priority queue mapping.   | 2'b10 |
| 20[1:0]  | 227[1:0] | R/W | PREDEF_PORT_0Q[1:0]<br>Pre-defined port 0 transmit priority queue mapping.   | 2'b10 |
| 21[15:6] |          |     | RESERVED   |       |
| 21[5:2]  | 228[5:2] | R/W | PREDEF_PORT_DROP[3:0]<br>Pre-defined logic port drop packet.<br>Drop the incoming packets that match the TCP/UDP port number defined in PREDEF_PORT_0[15:0] to PREDEF_PORT_3[15:0].<br>Drop ability has the precedence over the frame classify priority.<br>[0] drop packet port number matches PREDEF_PORT_0[15:0]<br>[1] drop packet port number matches PREDEF_PORT_1[15:0]<br>[2] drop packet port number matches PREDEF_PORT_2[15:0]<br>[3] drop packet port number matches PREDEF_PORT_3[15:0] | 4'h0  |
| 21[1:0]  | 228[1:0] | R/W | USERDEF_RANGE_DROP[1:0]<br>User defined logic port drop packet.<br>Drop the incoming packets that match the TCP/UDP port number defined in port range register.<br>[0] USERDEF_RANGE0_LOW~ USERDEF_RANGE0_HIGH<br>[1] USERDEF_RANGE1_LOW~ USERDEF_RANGE1_HIGH<br>Drop ability has the precedence over the frame classify priority.   | 2'b00 |

### 5.12.2 Queue Scheduling Configuration Register

| PHY    | MII       | ROM      | R/W | Description   | Default |    |    |    |    |        |     |     |     |     |        |     |     |     |         |        |    |     |     |    |        |    |    |    |    |
|--------|-----------|----------|-----|---|---------|----|----|----|----|--------|-----|-----|-----|-----|--------|-----|-----|-----|---------|--------|----|-----|-----|----|--------|----|----|----|----|
| 25     | 22[13]    | 229[5]   | R/W | QOS_OVER_FC<br>QoS over Flow Control  | 1'b0    |    |    |    |    |        |     |     |     |     |        |     |     |     |         |        |    |     |     |    |        |    |    |    |    |
|        | 22[12]    |          |     | RESERVED  |         |    |    |    |    |        |     |     |     |     |        |     |     |     |         |        |    |     |     |    |        |    |    |    |    |
|        | 22[11:10] | 229[3:2] | R/W | SCH_TYPE_5[1:0]<br>Queue scheduling configuration of port 5.<br><br><table style="margin-left: 40px; border-collapse: collapse;"> <tr> <td></td> <td>Q3</td> <td>Q2</td> <td>Q1</td> <td>Q0</td> </tr> <tr> <td>2'b00:</td> <td>WRR</td> <td>WRR</td> <td>WRR</td> <td>WRR</td> </tr> <tr> <td>2'b01:</td> <td>WFQ</td> <td>WFQ</td> <td>WFQ</td> <td>WFQ(BE)</td> </tr> <tr> <td>2'b10:</td> <td>SP</td> <td>WFQ</td> <td>WFQ</td> <td>BE</td> </tr> <tr> <td>2'b11:</td> <td>SP</td> <td>SP</td> <td>SP</td> <td>SP</td> </tr> </table><br>WRR: Weight Round Robin<br>WFQ: Weight Far Queuing<br>BE: Best Effort<br>SP: Strictly Priority |         | Q3 | Q2 | Q1 | Q0 | 2'b00: | WRR | WRR | WRR | WRR | 2'b01: | WFQ | WFQ | WFQ | WFQ(BE) | 2'b10: | SP | WFQ | WFQ | BE | 2'b11: | SP | SP | SP | SP |
|        | Q3        | Q2       | Q1  | Q0  |         |    |    |    |    |        |     |     |     |     |        |     |     |     |         |        |    |     |     |    |        |    |    |    |    |
| 2'b00: | WRR       | WRR      | WRR | WRR   |         |    |    |    |    |        |     |     |     |     |        |     |     |     |         |        |    |     |     |    |        |    |    |    |    |
| 2'b01: | WFQ       | WFQ      | WFQ | WFQ(BE)   |         |    |    |    |    |        |     |     |     |     |        |     |     |     |         |        |    |     |     |    |        |    |    |    |    |
| 2'b10: | SP        | WFQ      | WFQ | BE  |         |    |    |    |    |        |     |     |     |     |        |     |     |     |         |        |    |     |     |    |        |    |    |    |    |
| 2'b11: | SP        | SP       | SP  | SP  |         |    |    |    |    |        |     |     |     |     |        |     |     |     |         |        |    |     |     |    |        |    |    |    |    |
|        | 22[9:8]   | 229[1:0] | R/W | SCH_TYPE_4[1:0]<br>Queue scheduling configuration of port 4.  | 2'b00   |    |    |    |    |        |     |     |     |     |        |     |     |     |         |        |    |     |     |    |        |    |    |    |    |



|  |         |          |     |  |       |
|--|---------|----------|-----|--|-------|
|  | 22[7:6] | 230[7:6] | R/W | SCH_TYPE_3[1:0]<br>Queue scheduling configuration of port 3. | 2'b00 |
|  | 22[5:4] | 230[5:4] | R/W | SCH_TYPE_2[1:0]<br>Queue scheduling configuration of port 2. | 2'b00 |
|  | 22[3:2] | 230[3:2] | R/W | SCH_TYPE_1[1:0]<br>Queue scheduling configuration of port 1. | 2'b00 |
|  | 22[1:0] | 230[1:0] | R/W | SCH_TYPE_0[1:0]<br>Queue scheduling configuration of port 0. | 2'b00 |

| PHY | MII       | ROM      | R/W | Description   | Default |
|-----|-----------|----------|-----|---|---------|
| 25  | 23[15:12] | 231[7:4] | R/W | Q3_WEIGHT<br>Output queue 3 Weighted Round-Robin scheduling control registers<br>4'b1111: 15 packets<br>4'b1110: 14 packets<br>.<br>;<br>4'b0010: 2 packets<br>4'b0001: 1 packet<br>4'b0000: reserved | 4'b1000 |
|     | 23[11:8]  | 231[3:0] | R/W | Q2_WEIGHT<br>Output queue 2 Weighted Round-Robin scheduling control registers<br>4'b1111: 15 packets<br>4'b1110: 14 packets<br>.<br>;<br>4'b0010: 2 packets<br>4'b0001: 1 packet<br>4'b0000: reserved | 4'b0100 |
| 25  | 23[7:4]   | 232[7:4] | R/W | Q1_WEIGHT<br>Output queue 1 Weighted Round-Robin scheduling control registers<br>4'b1111: 15 packets<br>4'b1110: 14 packets<br>.<br>;<br>4'b0010: 2 packets<br>4'b0001: 1 packet<br>4'b0000: reserved | 4'b0010 |
|     | 23[3:0]   | 232[3:0] | R/W | Q0_WEIGHT<br>Output queue 0 Weighted Round-Robin scheduling control registers<br>4'b1111: 15 packets<br>4'b1110: 14 packets<br>.<br>;<br>4'b0010: 2 packets<br>4'b0001: 1 packet<br>4'b0000: reserved | 4'b0001 |

### 5.13 QoS Multi-Field Classification

#### 5.13.1 Multi-Field Classification Table Control Register

| PHY | MII    | ROM | R/W         | Description   | Default |
|-----|--------|-----|-------------|---|---------|
| 26  | 0[15]  | --  | R/W         | MF_QOS_EN<br>Multi-Field QoS access control function enabled.<br>When this bit is enabled, switch engine will use Multi-Field registers to classify the incoming frame.   | 1'b0    |
|     | 0[10]  | --  | R/W<br>(SC) | MF_REG_CLR<br>Clear the contents of Multi-Field classification register and Multi-Filed table QOS rate control register. This bit is for programming convenience consideration. When set it will clear all the multi-field registers to zero, excepts the IP mask registers – MF_IP_SA_MASK[3:0] & MF_IP_DA_MASK[3:0].<br>1: clear registers<br>0: do nothing (default)<br>A self-cleared register after set and registers cleared. | 1'b0    |
|     | 0[9]   | --  | R/W<br>(SC) | MF_CNT_RESET<br>Multi-Field counter reset. When reset, it will reference the setting of MF_RESET_EN register.<br>1: enable<br>0: disable  | 1'b0    |
|     | 0[8]   | --  | R/W<br>(SC) | MF_ENTRY_RESET<br>Multi-Field entry reset. When reset, it will reference the setting of MF_RESET_EN register.<br>1: enable<br>0: disable  | 1'b0    |
|     | 0[7:0] | --  | R/W         | MF_RESET_EN[7:0]<br>Multi-Filed reset enable for each entry or counter.<br>1: enable<br>0: disable  | 8'h00   |





|    |          |    |     |  |              |
|----|----------|----|-----|--|--------------|
|    | 8[15:0]  | -- | R/W | MF_ET_VALUE[15:0]<br>EtherType value   | 16'h00<br>00 |
|    | 9[15]    | -- | R/W | MF_ET_EN<br>EtherType field enable   | 1'b0         |
|    | 9[14]    |    |     | RESERVED   |              |
|    | 9[13:12] | -- | R/W | MF_FW_CTRL[1:0]<br>Forward or copy packet to specific port when Multi_Field entry hit<br>2'b00: Disable<br>2'b01: Forward to CPU<br>2'b10: Copy to mirror port<br>2'b11: Reserved  | 2'b00        |
|    | 9[11:9]  | -- | R/W | MF_PRI_CTRL[2:0]<br>Forward packet to specific queue when Multi_Field entry hit<br>3'b000: Disable<br>3'b100: Forward to queue 0<br>3'b101: Forward to queue 1<br>3'b110: Forward to queue 2<br>3'b111: Forward to queue 3<br>Other: Reserved  | 3'b000       |
|    | 9[8]     | -- | R/W | MF_PTL_EN<br>IP protocol number field enable.  | 1'b0         |
|    | 9[7:0]   | -- | R/W | MF_PTL_NUM[7:0]<br>IP protocol number field.   | 8'h00        |
|    | 10[15:5] |    |     | RESERVED   |              |
|    | 10[4]    | -- | R/W | MF_LG_RANGE<br>Enable the TCP/UDP port range monitoring function.<br>When enabled, the source and destination port register is used as a port range monitor register.<br>MF_LG_SP_NUM will be a port monitor start number<br>MF_LG_DP_NUM will be a port monitor stop number<br><br>{MF_LG_DP_TYPE, MF_LG_SP_TYPE}    Monitor type<br>00                                    reserved<br>01                                    TCP<br>10                                    UDP<br>11                                    TCP or UDP<br><br>{MF_LG_DP_EN, MF_LG_SP_EN}       Monitor type<br>00                                    reserved<br>01                                    source port<br>10                                    destination port<br>11                                    source or dest. port | 1'b0         |
| 26 | 10 [3]   | -- | R/W | MF_LG_SP_EN<br>TCP/UDP source port field enable.   | 1'b0         |
|    | 10[2]    | -- | R/W | MF_LG_SP_TYPE<br>Indicates the MF_LG_SP_NUM field is a TCP or UDP port.<br>0: TCP port<br>1: UDP port  | 1'b0         |

|           |    |     |  |       |
|-----------|----|-----|--|-------|
| 10[1]     | -- | R/W | MF_LG_DP_EN<br>TCP/UDP destination port field enable.  | 1'b0  |
| 10[0]     | -- | R/W | MF_LG_DP_TYPE<br>Indicates the MF_LG_DP_NUM field is a TCP or UDP port.<br>0: TCP port<br>1: UDP port  | 1'b0  |
| 11[15:0]  | -- | R/W | MF_LG_SP_NUM[15:0]<br>TCP/UDP source port number to be monitored.  | 16'h0 |
| 12[15:0]  | -- | R/W | MF_LG_DP_NUM[15:0]<br>TCP/UDP destination port number to be monitored.   | 16'h0 |
| 13[15]    |    | R/W | MF_SP_EN<br>Physical source port field enable  | 1'b0  |
| 13[14:10] | -- | R/W | MF_SP_NUM[4:0]<br>Physical source port number (port 0 ~ 4)<br>bit[4]: port 4<br>bit[3]: port 3<br>bit[2]: port 2<br>bit[1]: port 1<br>bit[0]: port 0 | 5'h00 |
| 13[9:0]   |    |     | RESERVED   |       |
| 14[7]     | -- | R/W | MF_BA_EN<br>Behavior Aggregate function enable   | 1'b0  |
| 14[6]     | -- | R/W | MF_BA_TYPE<br>Behavior Aggregate function type<br>0: DSCP ( ipv4 TOS or ipv6 DSCP )<br>1: VLAN priority  | 1'b0  |
| 14[5:0]   | -- | R/W | MF_BA_VALUE[5:0]<br>Behavior Aggregate value<br>For DSCP, using whole 6-bits, but the upper 3-bit for VLAN priority reference.                       | 6'h00 |

### 5.13.3 Multi-Field Table QoS Rate Control Register

| PHY | MII      | ROM | R/W | Description  | Default      |
|-----|----------|-----|-----|--|--------------|
| 26  | 16[15:0] | --  | R/W | MF_MBS[15:0]<br>Maximum Burst Size<br>Expressed in byte.   | 16'h<br>0000 |
|     | 17[15:0] | --  | R/W | MF_CREDIT_SIZE[15:0]<br>Credit size to accumulate the bucket in per time interval.<br>Expressed in byte. | 16'h<br>0000 |

### 5.13.4 Multi-Field Access Control Register

| PHY | MII     | ROM | R/W | Description  | Default |
|-----|---------|-----|-----|--|---------|
| 26  | 19[7:0] | --  | R/W | MF_VALID[7:0]<br>Multi-Field function valid for each entry.                    | 8'h00   |
|     | 20[2:0] | --  | R/W | MF_ENTRY[2:0]<br>Multi-Field entry number.<br>8-entry is used MF QoS function, | 3'h0    |



|          |    |             |   |              |
|----------|----|-------------|---|--------------|
| 20[3]    | -- | R/W         | MF_RW<br>Multi-field data read/write signal<br>0: read Multi-Field data<br>1: write Multi-Field data  | 1'b0         |
| 20[4]    | -- | R/W<br>(SC) | MF_RW_START<br>Indicates start read/write Multi-Field of an entry, when write a logical "1" to this register.<br>A self cleared register after read/write data done.        | 1'b0         |
| 20[5]    | -- | R/W         | MF_OVERFLOW_THR<br>MF counter overflow threshold index<br>1: 32'hFFFF_0000<br>0: 32'hFF00_0000  | 1'b0         |
| 20[6]    | -- | R/W<br>(SC) | MF_CNT_READ<br>Indicates start read Multi-Field counter content of an entry, when write a logical "1" to this register.<br>A self cleared register after read counter done. | 1'b0         |
| 21[15:0] | -- | RO<br>(SC)  | MF_CNT_LSB[15:0]<br>Multi-Field counter content after data read, LSB part.  | 16'h00<br>00 |
| 22[15:0] | -- | RO<br>(SC)  | MF_CNT_MSB[31:16]<br>Multi-Field counter content after data read, MSB part.   | 16'h00<br>00 |

#### 5.13.5 Multi-Field Status Register

| PHY | MII     | ROM | R/W        | Description   | Default |
|-----|---------|-----|------------|---|---------|
| 26  | 23[7:0] | --  | RO<br>(SC) | MF_OVERFLOW[7:0]<br>Multi-Field counter overflow for each entry | 8'h00   |

**6 Crystal Specifications**

| Item | Parameter                    | Range   |
|------|------------------------------|---|
| 1    | Nominal Frequency            | 25.000 MHz  |
| 2    | Oscillation Mode             | Fundamental Mode  |
| 3    | Frequency Tolerance at 25°C  | +/- 50 ppm  |
| 4    | Temperature Characteristics  | +/- 50 ppm  |
| 5    | Operating Temperature Range  | -10°C ~ +70°C (for IP175DLF)<br>-40°C ~ +85°C (for IP175DLFI) |
| 6    | Equivalent Series Resistance | 40 ohm Max.   |
| 7    | Drive Level                  | 100 $\mu$ W   |
| 8    | Load Capacitance             | 20 pF   |
| 9    | Shunt Capacitance            | 7 pF Max  |
| 10   | Insulation Resistance        | Mega ohm Min./DC 100V   |
| 11   | Aging Rate A Year            | +/- 5 ppm/year  |

## 7 Electrical Characteristics

### 7.1 Absolute Maximum Rating

Stresses exceed those values listed under Absolute Maximum Ratings may cause permanent damage to the device. Functional performance and device reliability are not guaranteed under these conditions. All voltages are specified with respect to GND.

|  |       |                |
|--|-------|----------------|
| Supply Voltage                                 | ..... | -0.3V to 3.63V |
| Input Voltage                                  | ..... | -0.3V to 3.63V |
| Output Voltage                                 | ..... | -0.3V to 3.63V |
| Storage Temperature                            |       | -65°C to 150°C |
| Ambient Operating Temperature (Ta) (IP175DLF)  |       | 0°C to 70°C    |
| IC Junction Temperature (Tj) (IP175DLF)        |       | 0°C to 125°C   |
| Ambient Operating Temperature (Ta) (IP175DLFI) |       | -40°C to 85°C  |
| IC Junction Temperature (Tj) (IP175DLFI)       |       | -40°C to 125°C |

### 7.2 DC Characteristic

#### Operating Conditions

| Parameter         | Sym.    | Min.  | Typ. | Max.  | Unit | Conditions                    |
|-------------------|---------|-------|------|-------|------|-------------------------------|
| Supply Voltage    | VCC     | 1.70  | 1.90 | 2.00  | V    |                               |
| Supply Voltage    | VCC_O   | 3.135 | 3.3  | 3.465 | V    |                               |
| Regout Voltage    | REG_OUT | 1.85  | 1.90 | 2.00  | V    | All ports link at 10Mbps mode |
| Power Consumption |         |       | 1    |       | W    | VCC=1.9v, 100Mbps full duplex |

#### Input Clock

| Parameter           | Sym. | Min. | Typ. | Max. | Unit | Conditions |
|---------------------|------|------|------|------|------|------------|
| Frequency           |      |      | 25   |      | MHz  |            |
| Frequency Tolerance |      | -50  |      | +50  | PPM  |            |

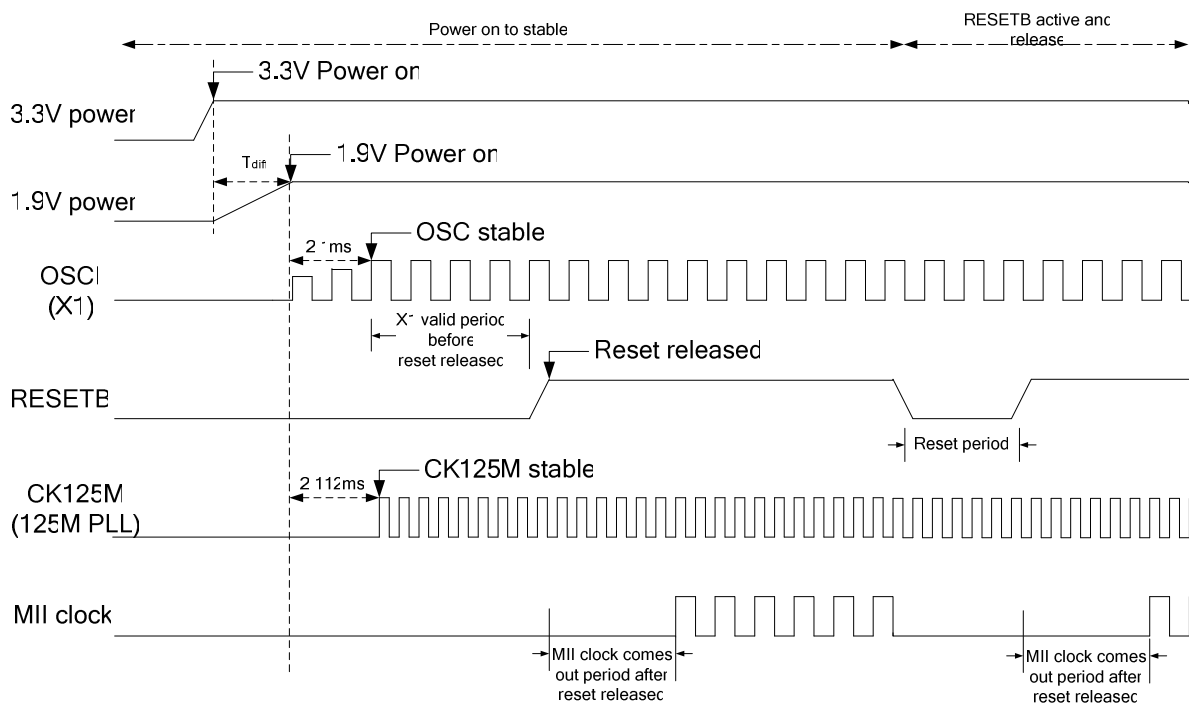
#### I/O Electrical Characteristics

| Parameter   | Sym  | Min.                                  | Max.                                  | Unit | Conditions            |
|---|------|---------------------------------------|---------------------------------------|------|-----------------------|
| Input Low Voltage<br>-LED PAD direct mode<br>-LED PAD bicolor mode<br>-NOT LED PAD  | VIL  |                                       | 0.39*VCC_O<br>0.36*VCC_O<br>0.4*VCC_O | V    |                       |
| Input High Voltage<br>-LED PAD direct mode<br>-LED PAD bicolor mode<br>-NOT LED PAD | VIH  | 0.58*VCC_O<br>0.58*VCC_O<br>0.6*VCC_O |                                       | V    |                       |
| X1 Input Low Voltage  | VIL  |                                       | 0.6                                   | V    | VCC = 1.9V            |
| X1 Input High Voltage   | VIH  | 1.5                                   |                                       | V    | VCC = 1.9V            |
| Output Low Voltage  | VOL  |                                       | 0.4                                   | V    | IOH=4mA, VCC_O_x=3.3V |
| Output High Voltage   | VOH  | 2.4                                   |                                       | V    | IOL=4mA, VCC_O_x=3.3V |
| RESETB Threshold Voltage  | Vrst | 0.4*VCC_O                             | 0.6*VCC_O                             | V    |                       |

### 7.3 AC Timing

#### 7.3.1 Power On Sequence and Reset Timing

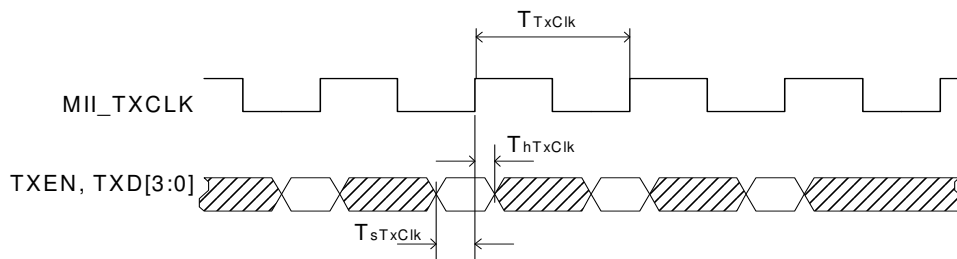
| Description  | Min. | Typ. | Max. | Unit |
|--|------|------|------|------|
| X1 valid period before reset released                          | 10   | -    | -    | ms   |
| Reset period   | 10   | -    | -    | ms   |
| All power source ready before reset released                   | 10   |      |      | ms   |
| Time difference between VCC3.3 and VCC1.9 (T <sub>diff</sub> ) | -2   |      |      | ms   |
| MII clock comes out period after reset released                | -    | 1    | -    | μs   |



7.3.2 PHY Mode MII (Turbo MII) Timing

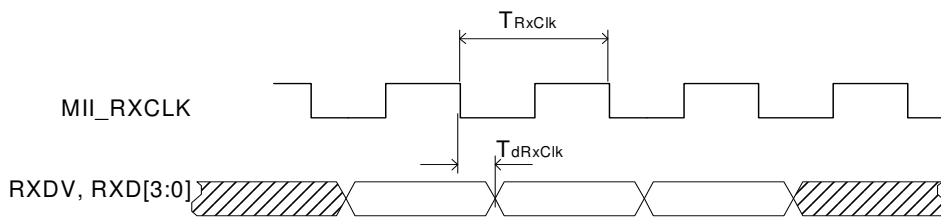
a. Transmit Timing Requirements

| Symbol       | Description                               | Min. | Typ. | Max. | Unit |
|--------------|---|------|------|------|------|
| $T_{TxClk}$  | Transmit clock period 100M MII            | -    | 40   | -    | ns   |
| $T_{TxClk}$  | Transmit clock period 10M MII             | -    | 400  | -    | ns   |
| $T_{TxClk}$  | Transmit clock period for TMII (50MHz)    |      | 20   |      | ns   |
| $T_{TxClk}$  | Transmit clock period for TMII (31.25MHz) |      | 32   |      | ns   |
| $T_{sTxClk}$ | TXEN, TXD to MII_TXCLK setup time         | 10   | -    | -    | ns   |
| $T_{hTxClk}$ | TXEN, TXD to MII_TXCLK hold time          | 5    | -    | -    | ns   |



b. Receive Timing

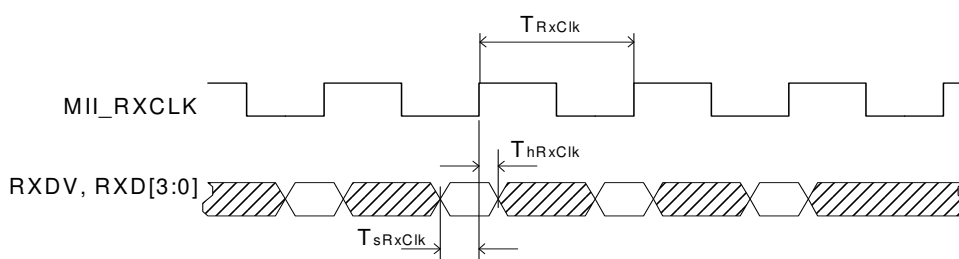
| Symbol       | Description                              | Min. | Typ. | Max. | Unit |
|--------------|--|------|------|------|------|
| $T_{RxClk}$  | Receive clock period 100M MII            | -    | 40   | -    | ns   |
| $T_{RxClk}$  | Receive clock period 10M MII             | -    | 400  | -    | ns   |
| $T_{RxClk}$  | Receive clock period for TMII (50MHz)    |      | 20   |      | ns   |
| $T_{RxClk}$  | Receive clock period for TMII (31.25MHz) |      | 32   |      | ns   |
| $T_{dRxClk}$ | MII_RXCLK falling edge to RXDV, RXD      | 2    | -    | 8    | ns   |



**7.3.3 MAC Mode MII (Turbo MII) Timing**

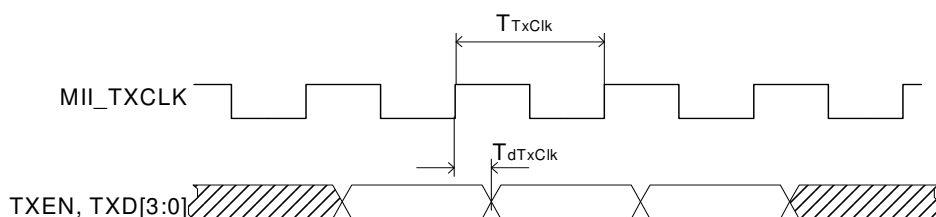
**a. Receive Timing Requirements**

| Symbol              | Description                              | Min. | Typ. | Max. | Unit |
|---------------------|--|------|------|------|------|
| $T_{RxClk}$         | Receive clock period 100M MII            | -    | 40   | -    | ns   |
| $T_{RxClk}$         | Receive clock period 10M MII             | -    | 400  | -    | ns   |
| $T_{RxClk}$         | Receive clock period for TMII (50MHz)    |      | 20   |      | ns   |
| $T_{RxClk}$         | Receive clock period for TMII (31.25MHz) |      | 32   |      | ns   |
| $T_{sRxClk}$        | RXDV, RXD to MII_RXCLK setup time        | 10   | -    | -    | ns   |
| $T_{hRxClk}$        | RXDV, RXD to MII_RXCLK hold time         | 5    | -    | -    | ns   |
| $T_{sRxClk}$ (TMII) | RXDV, RXD to MII_RXCLK setup time        | 4    | -    | -    | ns   |
| $T_{hRxClk}$ (TMII) | RXDV, RXD to MII_RXCLK hold time         | 1    | -    | -    | ns   |



**b. Transmit Timing**

| Symbol              | Description                               | Min. | Typ. | Max. | Unit |
|---------------------|---|------|------|------|------|
| $T_{TxClk}$         | Transmit clock period 100M MII            | -    | 40   | -    | ns   |
| $T_{TxClk}$         | Transmit clock period 10M MII             | -    | 400  | -    | ns   |
| $T_{TxClk}$         | Transmit clock period for TMII (50MHz)    |      | 20   |      | ns   |
| $T_{TxClk}$         | Transmit clock period for TMII (31.25MHz) |      | 32   |      | ns   |
| $T_{dTxClk}$        | MII_TXCLK rising edge to TXEN, TXD        | 6    | -    | 22   | ns   |
| $T_{dTxClk}$ (TMII) | MII_TXCLK rising edge to TXEN, TXD (note) | 6    | -    | 16.5 | ns   |



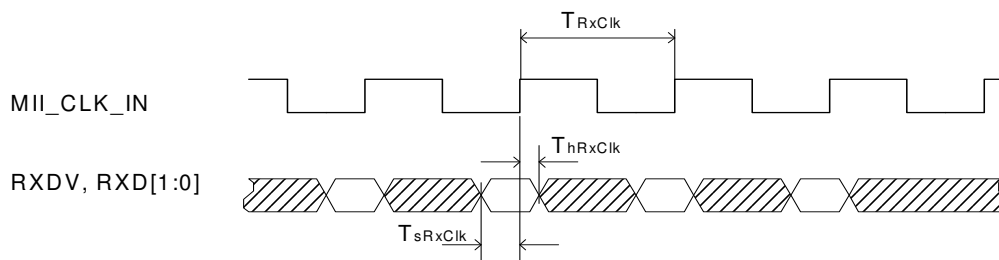
Note:

TMII Max. Condition: Voltage: 1.7V, Temperature: 125°C, Pad Load : 12 pF, Pad Drive : 8 mA

7.3.4 RMI Timing

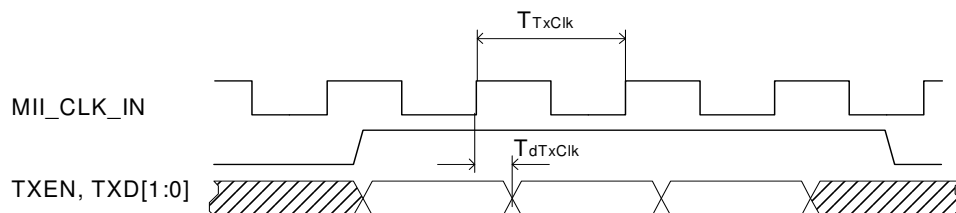
a. Receive Timing Requirements

| Symbol       | Description                        | Min. | Typ. | Max. | Unit |
|--------------|------------------------------------|------|------|------|------|
| $T_{RxClk}$  | Receive clock period               | -    | 20   | -    | ns   |
| $T_{sRxClk}$ | RXDV, RXD to MII_CLK_IN setup time | 4    | -    | -    | ns   |
| $T_{hRxClk}$ | RXDV, RXD to MII_CLK_IN hold time  | 2    | -    | -    | ns   |



b. Transmit Timing

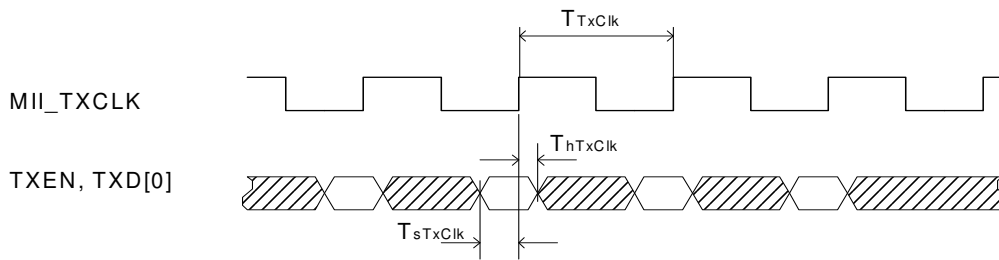
| Symbol      | Description                         | Min. | Typ. | Max. | Unit |
|-------------|-------------------------------------|------|------|------|------|
| $T_{TxClk}$ | Transmit clock period               | -    | 20   | -    | ns   |
| $T_{dTxCk}$ | MII_CLK_IN rising edge to TXEN, TXD | 5    | -    | 14   | ns   |



7.3.5 SNI Timing

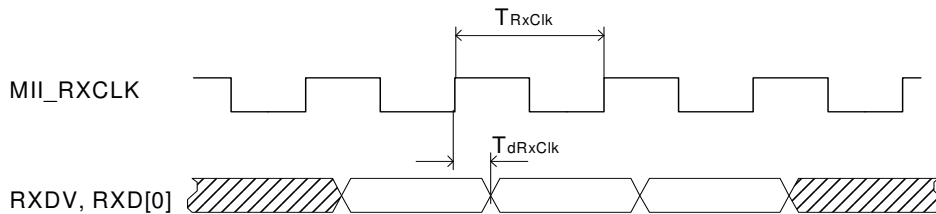
a. Transmit Timing Requirements

| Symbol       | Description                       | Min. | Typ. | Max. | Unit |
|--------------|-----------------------------------|------|------|------|------|
| $T_{TxClk}$  | Transmit clock period             | -    | 100  | -    | ns   |
| $T_{sTxClk}$ | TXEN, TXD to MII_TXCLK setup time | 10   | -    | -    | ns   |
| $T_{hTxClk}$ | TXEN, TXD to MII_TXCLK hold time  | 5    | -    | -    | ns   |



b. Receive Timing

| Symbol       | Description                        | Min. | Typ. | Max. | Unit |
|--------------|------------------------------------|------|------|------|------|
| $T_{RxClk}$  | Receive clock period               | -    | 100  | -    | ns   |
| $T_{dRxClk}$ | MII_RXCLK rising edge to RXDV, RXD | 1    | -    | 6    | ns   |

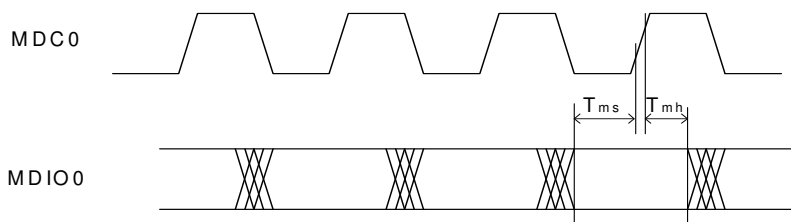




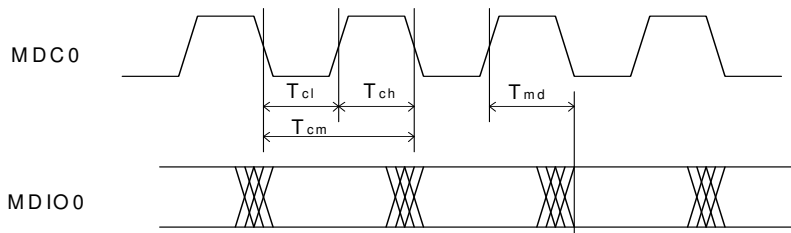
7.3.6 SMI Timing

a. MDC0/MDIO0 Timing

| Symbol   | Description        | Min. | Typ. | Max. | Unit |
|----------|--------------------|------|------|------|------|
| $T_{ch}$ | MDC0 High Time     | 40   | -    | -    | ns   |
| $T_{cl}$ | MDC0 Low Time      | 40   | -    | -    | ns   |
| $T_{cm}$ | MDC0 period        | 80   | -    | -    | ns   |
| $T_{md}$ | MDIO0 output delay | -    | -    | 15   | ns   |
| $T_{mh}$ | MDIO0 setup time   | 10   | -    | -    | ns   |
| $T_{ms}$ | MDIO0 hold time    | 5    | -    | -    | ns   |



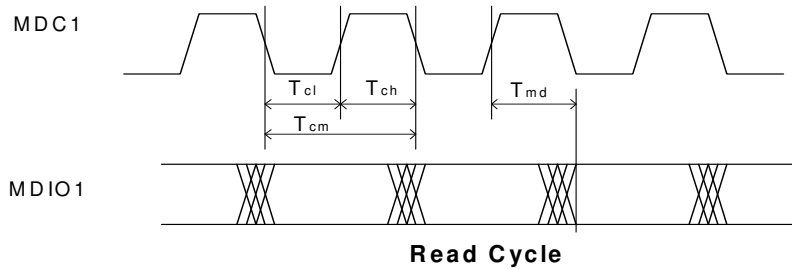
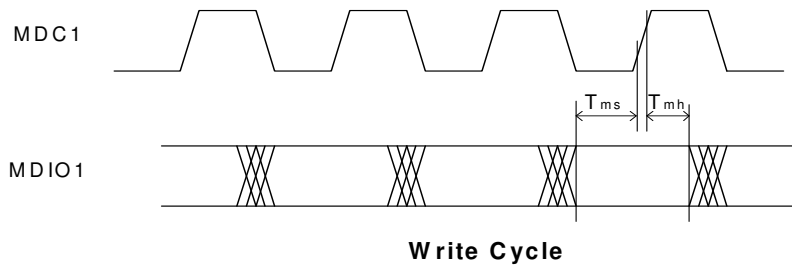
Write Cycle



Read Cycle

**b. MDC1/ MDIO1 Timing**

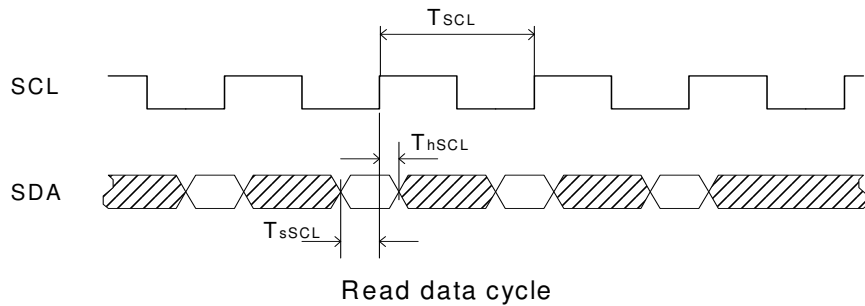
| Symbol   | Description   | Min. | Typ. | Max. | Unit |
|----------|---|------|------|------|------|
| $T_{ch}$ | MDC1 High Time  | 200  | -    | -    | ns   |
| $T_{cl}$ | MDC1 Low Time   | 200  | -    | -    | ns   |
| $T_{cm}$ | MDC1 period   | 400  | -    | -    | ns   |
| $T_{md}$ | MDIO1 output address delay<br>(for PHY address & register address only) | -    | -    | 200  | ns   |
| $T_{ms}$ | MDIO1 setup time  | 10   | -    | -    | ns   |
| $T_{mh}$ | MDIO1 hold time   | 10   | -    | -    | ns   |



### 7.3.7 EEPROM Timing

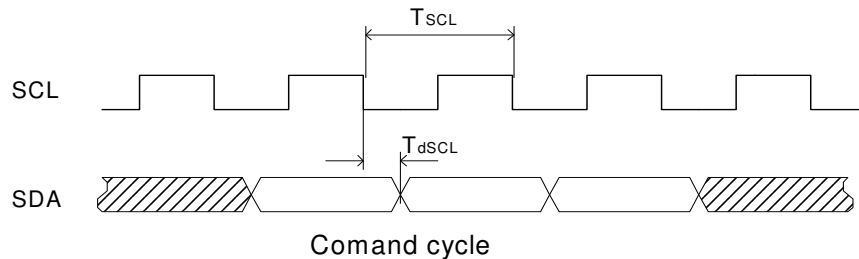
a.

| Symbol     | Description           | Min. | Typ.  | Max. | Unit |
|------------|-----------------------|------|-------|------|------|
| $T_{SCL}$  | Receive clock period  | -    | 20480 | -    | ns   |
| $T_{sSCL}$ | SDA to SCL setup time | 20   | -     | -    | ns   |
| $T_{hSCL}$ | SDA to SCL hold time  | 20   | -     | -    | ns   |



b.

| Symbol     | Description             | Min. | Typ.  | Max. | Unit |
|------------|-------------------------|------|-------|------|------|
| $T_{SCL}$  | Transmit clock period   | -    | 20480 | -    | ns   |
| $T_{dSCL}$ | SCL falling edge to SDA | -    | -     | 5200 | ns   |



### 7.4 Thermal Data

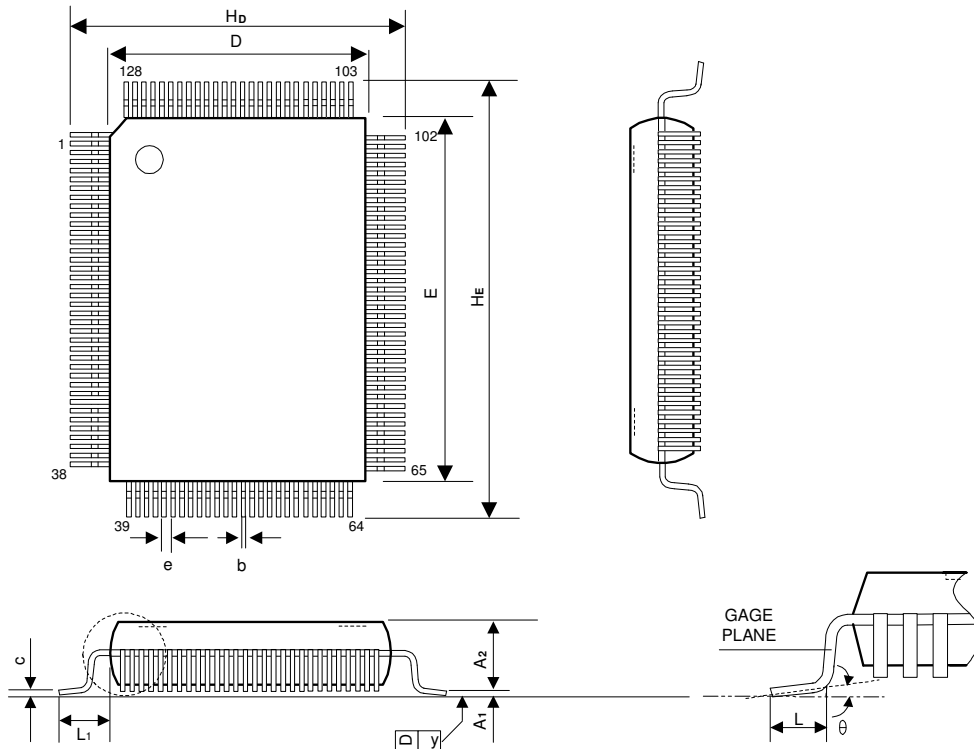
| Theta Ja | Theta Jc | Conditions  | Units |
|----------|----------|-------------|-------|
| 38.2     | --       | 2 Layer PCB | °C/W  |

### 8 Order Information

| Part No.  | Package      | Notice        |
|-----------|--------------|---------------|
| IP175DLF  | 128-PIN PQFP | -             |
| IP175DLFI | 128-PIN PQFP | -40°C to 85°C |

## 9 Package Detail

### 128 PQFP Outline Dimensions



| Symbol   | Dimensions In Inches |       |       | Dimensions In mm |       |       |
|----------|----------------------|-------|-------|------------------|-------|-------|
|          | Min.                 | Nom.  | Max.  | Min.             | Nom.  | Max.  |
| A1       | 0.010                | 0.014 | 0.018 | 0.25             | 0.35  | 0.45  |
| A2       | 0.107                | 0.112 | 0.117 | 2.73             | 2.85  | 2.97  |
| b        | 0.007                | 0.009 | 0.011 | 0.17             | 0.22  | 0.27  |
| c        | 0.004                | 0.006 | 0.008 | 0.09             | 0.15  | 0.20  |
| HD       | 0.669                | 0.677 | 0.685 | 17.00            | 17.20 | 17.40 |
| D        | 0.547                | 0.551 | 0.555 | 13.90            | 14.00 | 14.10 |
| HE       | 0.906                | 0.913 | 0.921 | 23.00            | 23.20 | 23.40 |
| E        | 0.783                | 0.787 | 0.791 | 19.90            | 20.00 | 20.10 |
| e        | -                    | 0.020 | -     | -                | 0.50  | -     |
| L        | 0.025                | 0.035 | 0.041 | 0.65             | 0.88  | 1.03  |
| L1       | -                    | 0.063 | -     | -                | 1.60  | -     |
| y        | -                    | -     | 0.004 | -                | -     | 0.10  |
| $\theta$ | 0°                   | -     | 12°   | 0°               | -     | 12°   |

Note:

1. Dimension D & E do not include mold protrusion.
2. Dimension B does not include dambar protrusion. Total in excess of the B dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot.