

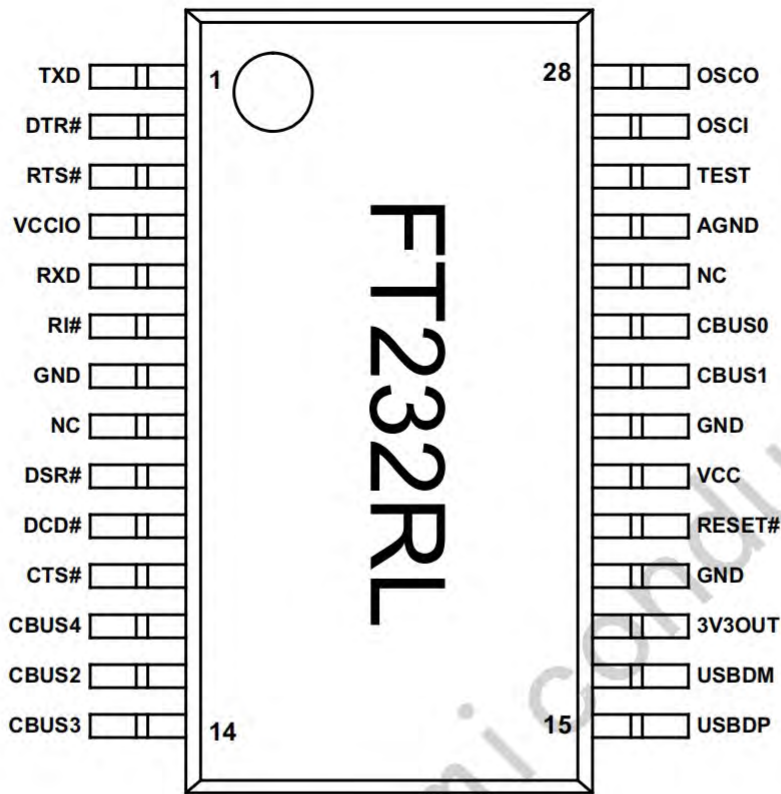
## 1. Hardware Features

- Single chip USB to asynchronous serial data transfer interface.
- Entire USB protocol handled on the chip. No USB specific firmware programming required.
- UART interface support for 7 or 8 data bits, 1 or 2 stop bits and odd / even / mark / space / no parity.
- Fully assisted hardware or X-On / X-Off software handshaking.
- Data transfer rates from 300 baud to 3 Megabaud (RS422 / RS485 and at TTL levels) and 300 baud to 1 Megabaud (RS232).
- 128 byte receive buffer and 256 byte transmit buffer utilising buffer smoothing technology to allow for high data throughput.
- In-built support for event characters and line break condition.
- New configurable CBUS I/O pins.
- Auto transmit buffer control for RS485 applications.
- Transmit and receive LED drive signals.
- New 48MHz, 24MHz, 12MHz, and 6MHz clock output signal options for driving external MCU or FPGA.
- FIFO receive and transmit buffers for high data throughput.
- Adjustable receive buffer timeout.
- Synchronous and asynchronous bit bang mode interface options with RD# and WR# strobes.
- New CBUS bit bang mode option.
- Integrated 1024 bit internal EEPROM for I/O configuration and storing USB VID, PID, serial number and product description strings.
- Support for USB suspend / resume.
- Support for bus powered, self powered, and high-power bus powered USB configurations.
- Integrated 3.3V level converter for USB I/O.
- Integrated level converter on UART and CBUS for interfacing to 5V – 1.8V Logic.
- True 5V / 3.3V / 2.8V / 1.8V CMOS drive output and TTL input.
- High I/O pin output drive option.
- Integrated USB resistors.
- Integrated power-on-reset circuit.
- Fully integrated clock – no external crystal, oscillator, or resonator required.
- Fully integrated AVCC supply filtering – No separate AVCC pin and no external R-C filter required.
- UART signal inversion option.
- USB bulk transfer mode.
- 3.3V to 5.25V Single Supply Operation.
- Low operating and USB suspend current.
- Low USB bandwidth consumption.
- UHCI / OHCI / EHCI host controller compatible.
- USB 2.0 Full Speed compatible.
- -40°C to 85°C extended operating temperature range.
- Available in 28 Pin SSOP package (RoHS compliant).

## 2. Application Areas

- USB to RS232 / RS422 / RS485 Converters
- Upgrading Legacy Peripherals to USB
- Cellular and Cordless Phone USB data transfer cables and interfaces
- Interfacing MCU / PLD / FPGA based designs to USB
- USB Audio and Low Bandwidth Video data transfer
- PDA to USB data transfer
- USB Smart Card Readers
- USB Instrumentation
- USB Industrial Control
- USB MP3 Player Interface
- USB FLASH Card Reader / Writers
- Set Top Box PC – USB interface
- USB Digital Camera Interface
- USB Hardware Modems
- USB Wireless Modems
- USB Bar Code Readers
- USB Software / Hardware Encryption Dongles

### 3. Device Pin Out and Signal Description



28-LD SSOP Package

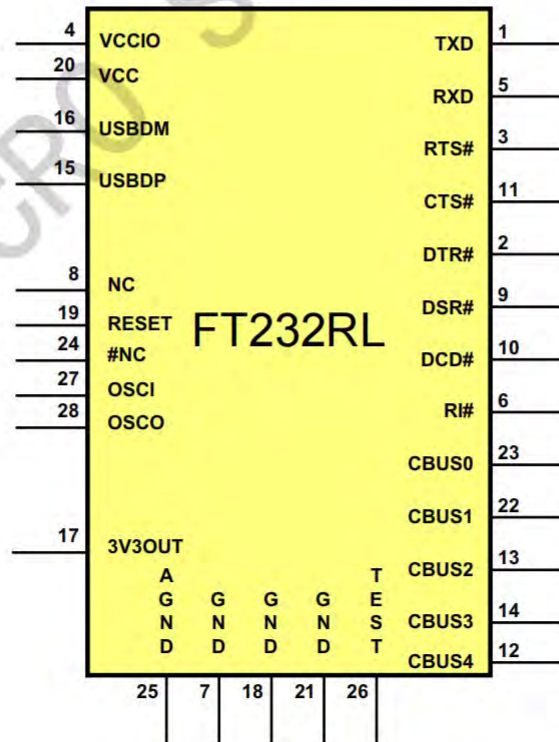


Figure 2. SSOP Package Pin Out and Schematic Symbol

**Table 1 SSOP Package Pin Out Description**

Pin No.	Name	Type	Description
<b>USB Interface Group</b>			
15	USBDP	I/O	USB Data Signal Plus, incorporating internal series resistor and 1.5kΩ pull up resistor to 3.3V.
16	USBDM	I/O	USB Data Signal Minus, incorporating internal series resistor.
<b>Power and Ground Group</b>			
4	VCCIO	PWR	+1.8V to +5.25V supply to the UART Interface and CBUS group pins (1...3, 5, 6, 9...14, 22, 23). In USB bus powered designs connect this pin to 3V3OUT pin to drive out at +3.3V levels, or connect to VCC to drive out at 5V CMOS level. This pin can also be supplied with an external +1.8V to +2.8V supply in order to drive outputs at lower levels. It should be noted that in this case this supply should originate from the same source as the supply to VCC. This means that in bus powered designs a regulator which is supplied by the +5V on the USB bus should be used.
7, 18, 21	GND	PWR	Device ground supply pins
17	3V3OUT	Output	+3.3V output from integrated LDO regulator. This pin should be decoupled to ground using a 100nF capacitor. The main use of this pin is to provide the internal +3.3V supply to the USB transceiver cell and the internal 1.5kΩ pull up resistor on USBDP. Up to 50mA can be drawn from this pin to power external logic if required. This pin can also be used to supply the VCCIO pin.
20	VCC	PWR	+3.3V to +5.25V supply to the device core.
25	AGND	PWR	Device analogue ground supply for internal clock multiplier
<b>Miscellaneous Signal Group</b>			
8, 24	NC	NC	No internal connection
19	RESET#	Input	Active low reset pin. This can be used by an external device to reset the FT232R. If not required can be left unconnected, or pulled up to VCC
26	TEST	Input	Puts the device into IC test mode. Must be tied to GND for normal operation.
27	OSCI	Input	Input 12MHz Oscillator Cell. Optional – Can be left unconnected for normal operation.
28	OSCO	Output	Output from 12MHZ Oscillator Cell. Optional – Can be left unconnected for normal operation if internal Oscillator is used.
<b>UART Interface and CBUS Group **</b>			
1	TXD	Output	Transmit Asynchronous Data Output
2	DTR#	Output	Data Terminal Ready Control Output / Handshake Signal.
3	RTS#	Output	Request to Send Control Output / Handshake Signal.
5	RXD	Input	Receiving Asynchronous Data Input.
6	RI#	Input	Ring Indicator Control Input. When remote wake up is enabled in the internal EEPROM taking RI# low can be used to resume the PC USB host controller from suspend.
9	DSR#	Input	Data Set Ready Control Input / Handshake Signal.
10	DCD#	Input	Data Carrier Detect Control Input.
11	CTS#	Input	Clear To Send Control Input / Handshake Signal.
12	CBUS4	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal EEPROM. Factory default configuration is SLEEP#. See CBUS Signal Options, Table 2.
13	CBUS2	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal EEPROM. Factory default configuration is TXDEN. See CBUS Signal Options, Table 2.
14	CBUS3	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal EEPROM. Factory default configuration is PWREN#. See CBUS Signal Options, Table 2.
22	CBUS1	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal EEPROM. Factory default configuration is RXLED#. See CBUS Signal Options, Table 2.
23	CBUS0	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal EEPROM. Factory default configuration is TXLED#. See CBUS Signal Options, Table 2.

\*\* When used in Input Mode, the input pins are pulled to VCCIO via internal 200kΩ resistors. These pins can be programmed to gently pull low during USB suspend (PWREN# = "1") by setting an option in the internal EEPROM.



### CBUS Signal Options

The following options can be configured on the CBUS I/O pins. CBUS signal options are common to both package versions of the FT232R. These options can be configured in the internal EEPROM using the software utility MPROG.

Table 2 CBUS Configuration Control

CBUS Signal Option	Available On CBUS Pin	Description
TXDEN	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	Enable transmit data for RS485
PWREN#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	Output is low after the device has been configured by USB, then high during USB suspending mode. This output can be used to control power to external logic P-Channel logic level MOSFET switch. Enable the interface pull-down option when using the PWREN# in this way.
TXLED#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	Transmit data LED drive: Data from USB Host to FT232R. Pulses low when transmitting data via USB. See Section 9 for more details.
RXLED#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	Receive data LED drive: Data from FT232R to USB Host. Pulses low when receiving data via USB. See Section 9 for more details
TX&RXLED#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	LED drive – pulses low when transmitting or receiving data via USB. See Section 9 for more details.
SLEEP#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	Goes low during USB suspend mode. Typically used to power down an external TTL to RS232 level converter IC in USB to RS232 converter designs.
CLK48	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	48 MHz Clock output.
CLK24	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	24 MHz Clock output.
CLK12	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	12 MHz Clock output.
CLK6	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	6 MHz Clock output.
CBitBangI/O	CBUS0, CBUS1, CBUS2, CBUS3	CBUS bit bang mode option. Allows up to 4 of the CBUS pins to be used as general purpose I/O. Configured individually for CBUS0, CBUS1, CBUS2 and CBUS3 in the internal EEPROM. A separate application note describes in more detail how to use CBUS bit bang mode.
BitBangWRn	CBUS0, CBUS1, CBUS2, CBUS3	Synchronous and asynchronous bit bang mode WR# strobe output.
BitBangRDn	CBUS0, CBUS1, CBUS2, CBUS3	Synchronous and asynchronous bit bang mode RD# strobe output.

## 4. Features

**Integrated Clock Circuit** - Previous generations of USB UART devices required an external crystal or ceramic resonator. The clock circuit has now been integrated onto the device meaning that no crystal or ceramic resonator is required. However, if required, an external 12MHz crystal can be used as the clock source.

**Integrated EEPROM** - A user area of the internal EEPROM is available for storing additional data. The internal EEPROM is programmable in circuit, over USB without any additional voltage requirement.

**Integrated USB Resistors** - Previous generations of FTDI's USB UART devices required two external series resistors on the USBDP and USBDM lines, and a 1.5 k $\Omega$  pull up resistor on USBDP. These three resistors have now been integrated onto the device.

**Integrated AVCC Filtering** - Previous generations of FTDI's USB UART devices had a separate AVCC pin – the supply to the internal PLL. This pin required an external R-C filter. The separate AVCC pin is now connected internally to VCC, and the filter has now been integrated onto the chip.

**Less External Components** - Integration of the crystal, EEPROM, USB resistors, and AVCC filter will substantially reduce the bill of materials cost for USB interface designs using the FT232R compared to its FT232BM predecessor.

**Transmit and Receive Buffer Smoothing** - The FT232R's 256 byte receive buffer and 128 byte transmit buffer utilise new buffer smoothing technology to allow for high data throughput.

**Configurable CBUS I/O Pin Options** - There are now 5 configurable Control Bus (CBUS) lines. Options are **TXDEN** - transmit enable for RS485 designs, **PWREN#** - Power control for high power, bus powered designs, **TXLED#** - for pulsing an LED upon transmission of data, **RXLED#** - for pulsing an LED upon receiving data, **TX&RXLED#** - which will pulse an LED upon transmission OR reception of data, **SLEEP#** - indicates that the device going into USB suspend mode, **CLK48 / CLK24 / CLK12 / CLK6** - 48MHz, 24MHz, 12MHz, and 6MHz clock output signal options. There is also the option to bring out bit bang mode read and write strobes (see below). The CBUS lines can be configured with any one of these output options by setting bits in the internal EEPROM.

**Enhanced Asynchronous Bit Bang Mode with RD# and WR# Strobes** - The FT232R supports BM chip bit bang mode. In bit bang mode, the eight UART lines can be switched from the regular interface mode to an 8-bit general purpose I/O port. Data packets can be sent to the device and they will be sequentially sent to the interface at a rate controlled by an internal timer (equivalent to the baud rate prescaler). With the FT232R device this mode has been enhanced so that the internal RD# and WR# strobes are now brought out of the device which can be used to allow external logic to be clocked by accesses to the bit bang I/O bus. This option will be described more fully in a separate application note.

**Synchronous Bit Bang Mode** - Synchronous bit bang mode differs from asynchronous bit bang mode in that the interface pins are only read when the device is written to. Thus making it easier for the controlling program to measure the response to an output stimulus as the data returned is synchronous to the output data.

**CBUS Bit Bang Mode** - This mode allows four of the CBUS pins to be individually configured as GPIO pins, similar to Asynchronous bit bang mode. It is possible to use this mode while the UART interface is being used, thus providing up to four general purpose I/O pins which are available during normal operation.

**Lower Supply Voltage** - Previous generations of the chip required 5V supply on the VCC pin. The FT232R will work with a Vcc supply in the range 3.3V - 5.25V. Bus powered designs would still take their supply from the 5V on the USB bus, but for self powered designs where only 3.3V is available and there is no 5V supply there is no longer any need for an additional external regulator.

**Integrated Level Converter on UART Interface and Control Signals** - VCCIO pin supply can be from 1.8V to 5V. Connecting the VCCIO pin to 1.8V, 2.8V, or 3.3V allows the device to directly interface to 1.8V, 2.8V or 3.3V and other logic families without the need for external level converter I.C. devices.

**5V / 3.3V / 2.8V / 1.8V Logic Interface** - The FT232R provides true CMOS Drive Outputs and TTL level Inputs.

**Integrated Power-On-Reset (POR) Circuit**- The device incorporates an internal POR function. A RESET# pin is available in order to allow external logic to reset the FT232R where required. However, for many applications the RESET# pin can be left unconnected, or pulled up to VCCIO.

**Lower Operating and Suspend Current** - The device operating supply current has been further reduced to 15mA, and the suspend current has been reduced to around 70µA. This allows greater margin for peripheral designs to meet the USB suspend current limit of 500µA.

**Low USB Bandwidth Consumption** - The operation of the USB interface to the FT232R has been designed to use as little as possible of the total USB bandwidth available from the USB host controller.

**High Output Drive Option** - The UART interface and CBUS I/O pins can be made to drive out at three times the standard signal drive level thus allowing multiple devices to be driven, or devices that require a greater signal drive strength to be interfaced to the FT232R. This option is enabled in the internal EEPROM.

**Power Management Control for USB Bus Powered, High Current Designs**- The PWREN# signal can be used to directly drive a transistor or P-Channel MOSFET in applications where power switching of external circuitry is required. An option in the internal EEPROM makes the device gently pull down on its UART interface lines when the power is shut off (PWREN# is high). In this mode any residual voltage on external circuitry is bled to GND when power is removed, thus ensuring that external circuitry controlled by PWREN# resets reliably when power is restored.

**UART Pin Signal Inversion** - The sense of each of the eight UART signals can be individually inverted by setting options in the internal EEPROM. Thus, CTS# (active low) can be changed to CTS (active high), or TXD can be changed to TXD#.

**Improved EMI Performance** - The reduced operating current and improved on-chip VCC decoupling significantly improves the ease of PCB design requirements in order to meet FCC, CE and other EMI related specifications.

**Programmable Receive Buffer Timeout** - The receive buffer timeout is used to flush remaining data from the receive buffer. This time defaults to 16ms, but is programmable over USB in 1ms increments from 1ms to 255ms, thus allowing the device to be optimised for protocols that require fast response times from short data packets.

**Extended Operating Temperature Range** - The FT232R operates over an extended temperature range of -40° to +85° C thus allowing the device to be used in automotive and industrial applications.

The FT232R is available in a compact 28 pin SSOP package (FT232RL) that is lead (Pb) free, and uses a 'green' compound. The package is fully compliant with European Union directive 2002/95/EC.



## 5. Block Diagram

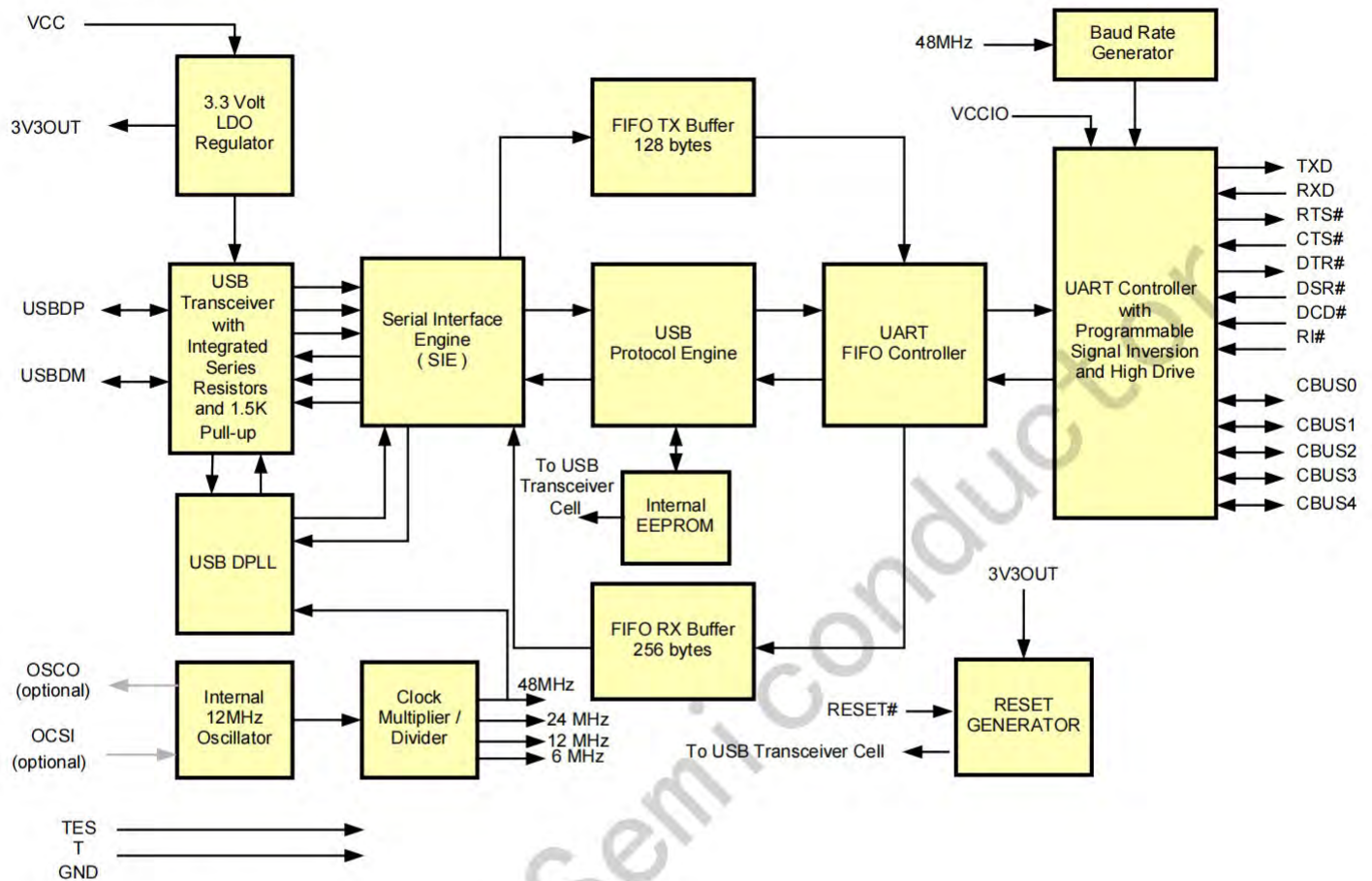


Figure 3. FT232R Block Diagram

## 6. Functional Block Descriptions

**3.3V LDO Regulator** - The 3.3V LDO Regulator generates the 3.3V reference voltage for driving the USB transceiver cell output buffers. It requires an external decoupling capacitor to be attached to the 3V3OUT regulator output pin. It also provides 3.3V power to the 1.5kΩ internal pull up resistor on USBDP. The main function of this block is to power the USB Transceiver and the Reset Generator Cells rather than to power external logic. However, external circuitry requiring a 3.3V nominal supply at a current of around than 50mA could also draw its power from the 3V3OUT pin, if required.

**USB Transceiver** - The USB Transceiver Cell provides the USB 1.1 / USB 2.0 full-speed physical interface to the USB cable. The output drivers provide 3.3V level slew rate control signalling, whilst a differential receiver and two single ended receivers provide USB data in, SEO and USB Reset condition detection. This Cell also incorporates internal USB series resistors on the USB data lines, and a 1.5kΩ pull up resistor on USBDP.

**USB DPLL** - The USB DPLL cell locks on to the incoming NRZI USB data and provides separate recovered clock and data signals to the SIE block.

**Internal 12MHz Oscillator** - The Internal 12MHz Oscillator cell generates a 12MHz reference clock input to the x4 Clock multiplier. The 12MHz Oscillator is also used as the reference clock for the SIE, USB Protocol Engine and UART FIFO controller blocks

**Clock Multiplier / Divider** - The Clock Multiplier / Divider takes the 12MHz input from the Oscillator Cell and generates the 48MHz, 24MHz, 12MHz, and 6MHz reference clock signals. The 48Mz clock reference is used for the USB DPLL and the Baud Rate Generator blocks.

**Serial Interface Engine (SIE)** - The Serial Interface Engine (SIE) block performs the Parallel to Serial and Serial to Parallel conversion of the USB data. In accordance to the USB 2.0 specification, it performs bit stuffing / un-stuffing and CRC5 / CRC16 generation / checking on the USB data stream.

**USB Protocol Engine** - The USB Protocol Engine manages the data stream from the device USB control endpoint. It handles the low level USB protocol (Chapter 9) requests generated by the USB host controller and the commands for controlling the functional parameters of the UART.

**FIFO TX Buffer (128 bytes)** - Data from the USB data out endpoint is stored in the FIFO TX buffer and removed from the buffer to the UART transmit register under control of the UART FIFO controller.

**FIFO RX Buffer (256 bytes)** - Data from the UART receive register is stored in the FIFO RX buffer prior to being removed by the SIE on a USB request for data from the device data in endpoint.

**UART FIFO Controller** - The UART FIFO controller handles the transfer of data between the FIFO RX and TX buffers and the UART transmit and receive registers.

**UART Controller with Programmable Signal Inversion and High Drive** - Together with the UART FIFO Controller the UART Controller handles the transfer of data between the FIFO RX and FIFO TX buffers and the UART transmit and receive registers. It performs asynchronous 7 / 8 bit Parallel to Serial and Serial to Parallel conversion of the data on the RS232 (RS422 and RS485) interface. Control signals supported by UART mode include RTS, CTS, DSR, DTR, DCD and RI. The UART Controller also provides a transmitter enable control signal pin option (TXDEN) to assist with interfacing to RS485 transceivers. RTS / CTS, DSR / DTR and X-On / X-Off handshaking options are also supported. Handshaking, where required, is handled in hardware to ensure fast response times. The UART also supports the RS232 BREAK setting and detection conditions. A new feature, programmable in the internal EEPROM allows the UART signals to each be individually inverted. Another new EEPROM programmable feature allows a high signal drive strength to be enabled on the UART interface and CBUS pins.

**Baud Rate Generator** - The Baud Rate Generator provides a x16 clock input to the UART Controller from the 48MHz reference clock and consists of a 14 bit prescaler and 3 register bits which provide fine tuning of the baud rate (used to divide by a number plus a fraction or "sub-integer"). This determines the Baud Rate of the UART, which is programmable from 183 baud to 3 million baud.

The FT232R supports all standard baud rates and non-standard baud rates from 300 Baud up to 3 Megabaud. Achievable non-standard baud rates are calculated as follows -

$$\text{Baud Rate} = 3000000 / (n + x)$$

where n can be any integer between 2 and 16,384 ( = 2<sup>14</sup> ) and x can be a sub-integer of the value 0, 0.125, 0.25, 0.375, 0.5, 0.625, 0.75, or 0.875. When n = 1, x = 0, i.e. baud rate divisors with values between 1 and 2 are not possible.

This gives achievable baud rates in the range 183.1 baud to 3,000,000 baud. When a non-standard baud rate is required simply pass the required baud rate value to the driver as normal, and the FTDI driver will calculate the required divisor, and set the baud rate.

**RESET Generator** - The integrated Reset Generator Cell provides a reliable power-on reset to the device internal circuitry on power up. A RESET# input pin is provided to allow other devices to reset the FT232R. RESET# can be tied to VCCIO or left unconnected, unless it is a requirement to reset the device from external logic or an external reset generator I.C.

**Internal EEPROM** - The internal EEPROM in the FT232R can be used to store USB Vendor ID (VID), Product ID (PID), device serial number, product description string, and various other USB configuration descriptors. The internal EEPROM is also used to configure the CBUS pin functions. The device is supplied with the internal EEPROM settings preprogrammed as described in Section 10.



## 7. Absolute Maximum Ratings

The absolute maximum ratings for the FT232R devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

Table 3 - Absolute Maximum Ratings

Parameter	Value	Unit
Storage Temperature	-65°C to 150°C	Degrees C
Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity)	168Hours (IPC/JEDECJ-STD-033A MSL Level 3 Compliant)*	Hours
Ambient Temperature (Power Applied)	-40°C to 85°C	Degrees C
Vcc Supply Voltage	-0.5 to +6.00	V
D.C. Input Voltage - USBDP and USBDM	-0.5 to +3.8	V
D.C. Input Voltage - High Impedance Bidirectionals	-0.5 to + (Vcc+0.5)	V
D.C. Input Voltage - All other Inputs	-0.5 to + (Vcc+0.5)	V
D.C. Output Current - Outputs	24	mA
D.C. Output Current - Low Impedance Bidirectionals	24	mA
Power Dissipation (Vcc = 5.25V)	500	mW

\* If devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of 125°C and baked for up to 17 hours.

## DC Characteristics

DC Characteristics (Ambient Temperature = -40°C to +85°C)

Table 4 - Operating Voltage and Current

Parameter	Description	Min	Typ	Max	Units	Conditions
Vcc1	VCC Operating Supply Voltage	3.3	-	5.25	V	
Vcc2	VCCIO Operating Supply Voltage	1.8	-	5.25	V	
Icc1	Operating Supply Current	-	15	-	mA	Normal Operation
Icc2	Operating Supply Current	50	70	100	µA	USB Suspend

Table 5 - UART and CBUS I/O Pin Characteristics (VCCIO = 5.0V, Standard Drive Level)

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	3.2	4.1	4.9	V	I source = 2mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 2mA
Vin	Input Switching Threshold	1.3	1.6	1.9	V	**
VHys	Input Switching Hysteresis	50	55	60	mV	**

Table 6 - UART and CBUS I/O Pin Characteristics (VCCIO = 3.3V, Standard Drive Level)

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	2.2	2.7	3.2	V	I source = 1mA
Vol	Output Voltage Low	0.3	0.4	0.5	V	I sink = 2mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

**Table 7 - UART and CBUS I/O Pin Characteristics (VCCIO = 2.8V, Standard Drive Level)**

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	2.1	2.6	3.1	V	I source = 1mA
Vol	Output Voltage Low	0.3	0.4	0.5	V	I sink = 2mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

**Table 8 - UART and CBUS I/O Pin Characteristics (VCCIO = 5.0V, High Drive Level)**

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	3.2	4.1	4.9	V	I source = 6mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 6mA
Vin	Input Switching Threshold	1.3	1.6	1.9	V	**
VHys	Input Switching Hysteresis	50	55	60	mV	**

**Table 9 - UART and CBUS I/O Pin Characteristics (VCCIO = 3.3V, High Drive Level)**

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	2.2	2.8	3.2	V	I source = 3mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 8mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

**Table 10 - UART and CBUS I/O Pin Characteristics (VCCIO = 3.3V, High Drive Level)**

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	2.1	2.8	3.2	V	I source = 3mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 8mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

\*\*Inputs have an internal 200kΩ pull-up resistor to VCCIO.

**Table 11 - RESET# and TEST Pin Characteristics**

Parameter	Description	Min	Typ	Max	Units	Conditions
Vin	Input Switching Threshold	1.3	1.6	1.9	V	
VHys	Input Switching Hysteresis	50	55	60	mV	

**Table 12 - USB I/O Pin (USBDP, USBDM) Characteristics**

Parameter	Description	Min	Typ	Max	Units	Conditions
UVoh	I/O Pins Static Output (High)	2.8		3.6	V	RI = 1.5kΩ to 3V3Out ( D+ ) RI = 15kΩ to GND ( D- )
UVol	I/O Pins Static Output (Low)	0		0.3	V	RI = 1.5kΩ to 3V3Out ( D+ ) RI = 15kΩ to GND ( D- )
UVse	Single Ended Rx Threshold	0.8		2.0	V	
UCom	Differential Common Mode	0.8		2.5	V	
UVDif	Differential Input Sensitivity	0.2			V	
UDrvZ	Driver Output Impedance	26	29	44	Ohms	***

\*\*\*Driver Output Impedance includes the internal USB series resistors on USBDP and USBDM pins.

### EEPROM Reliability Characteristics

The internal 1024 Bit EEPROM has the following reliability characteristics.

Table 13 - EEPROM Characteristics

Parameter	Value	Units
Data Retention	15	Years
Read / Write Cycles	100,000	Cycles

### Internal Clock Characteristics

The internal Clock Oscillator has the following characteristics.

Table 14 - Internal Clock Characteristics

Parameter	Value			Units
	Min	Typical	Max	
Frequency of Operation	11.98	12.00	12.02	MHz****
Clock Period	83.19	83.33	83.47	ns
Duty Cycle	45	50	55	%

\*\*\*\*Equivalent to +/-1667ppm.

Table 15 - OSCI, OSCO Pin Characteristics (Optional - Only applies if external Oscillator is used\*\*\*\*\*)

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	2.8	-	3.6	V	Fosc=12MHz
Vol	Output Voltage Low	0.1	-	1.0	V	Fosc=12MHz
Vin	Input Switching Threshold	1.8	2.5	3.2	V	

\*\*\*\*\*When supplied the device is configured to use its internal clock oscillator.



## 8. Device Configurations

### Bus Powered Configuration

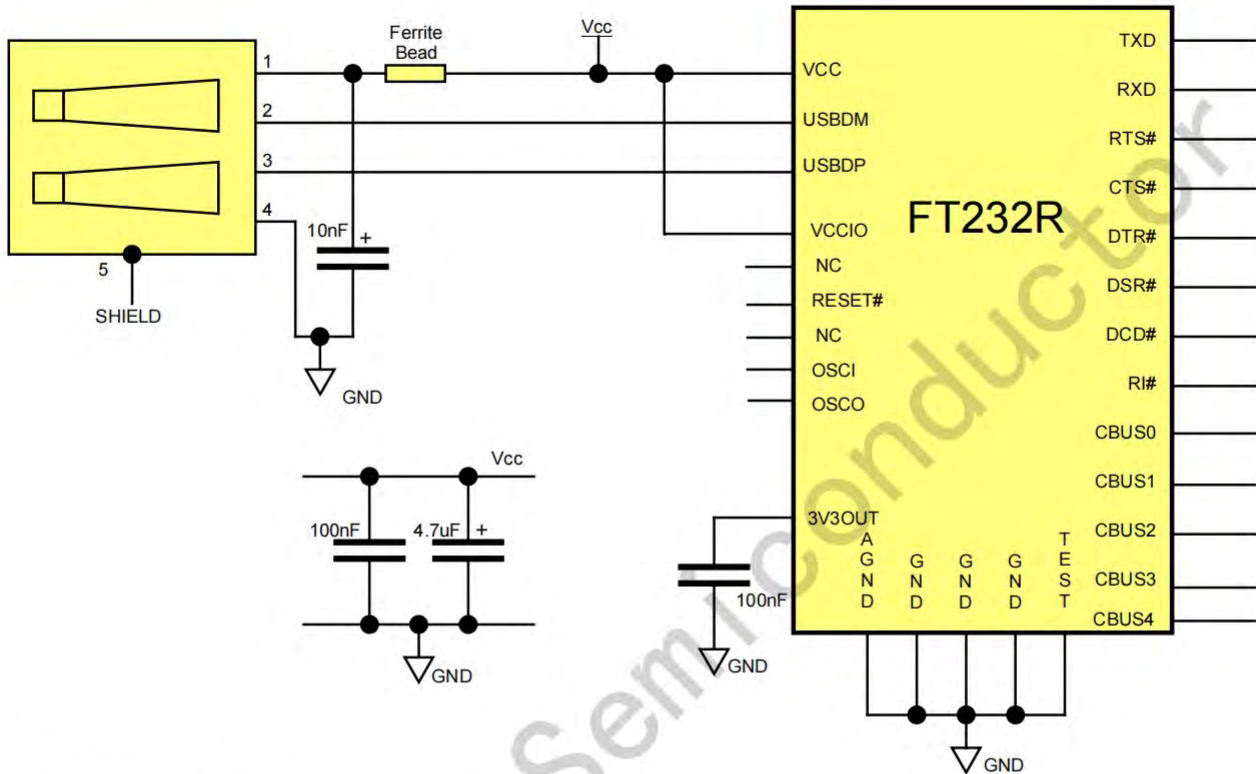


Figure 4 - Bus Powered Configuration

Figure 4 illustrates the FT232R in a typical USB bus powered design configuration. A USB Bus Powered device gets its power from the USB bus. Basic rules for USB Bus power devices are as follows –

- 1) On plug-in to USB, the device must draw no more than 100mA.
- 2) On USB Suspend the device must draw no more than 500 $\mu$ A.
- 3) A Bus Powered High Power USB Device (one that draws more than 100mA) should use one of the CBUS pins configured as PWREN# and use it to keep the current below 100mA on plug-in and 500 $\mu$ A on USB suspend.
- 4) A device that consumes more than 100mA can not be plugged into a USB Bus Powered Hub.
- 5) No device can draw more that 500mA from the USB Bus.

The power descriptor in the internal EEPROM should be programmed to match the current draw of the device. A Ferrite Bead is connected in series with USB power to prevent noise from the device and associated circuitry (EMI) being radiated down the USB cable to the Host. The value of the Ferrite Bead depends on the total current required by the circuit.

Self Powered Configuration

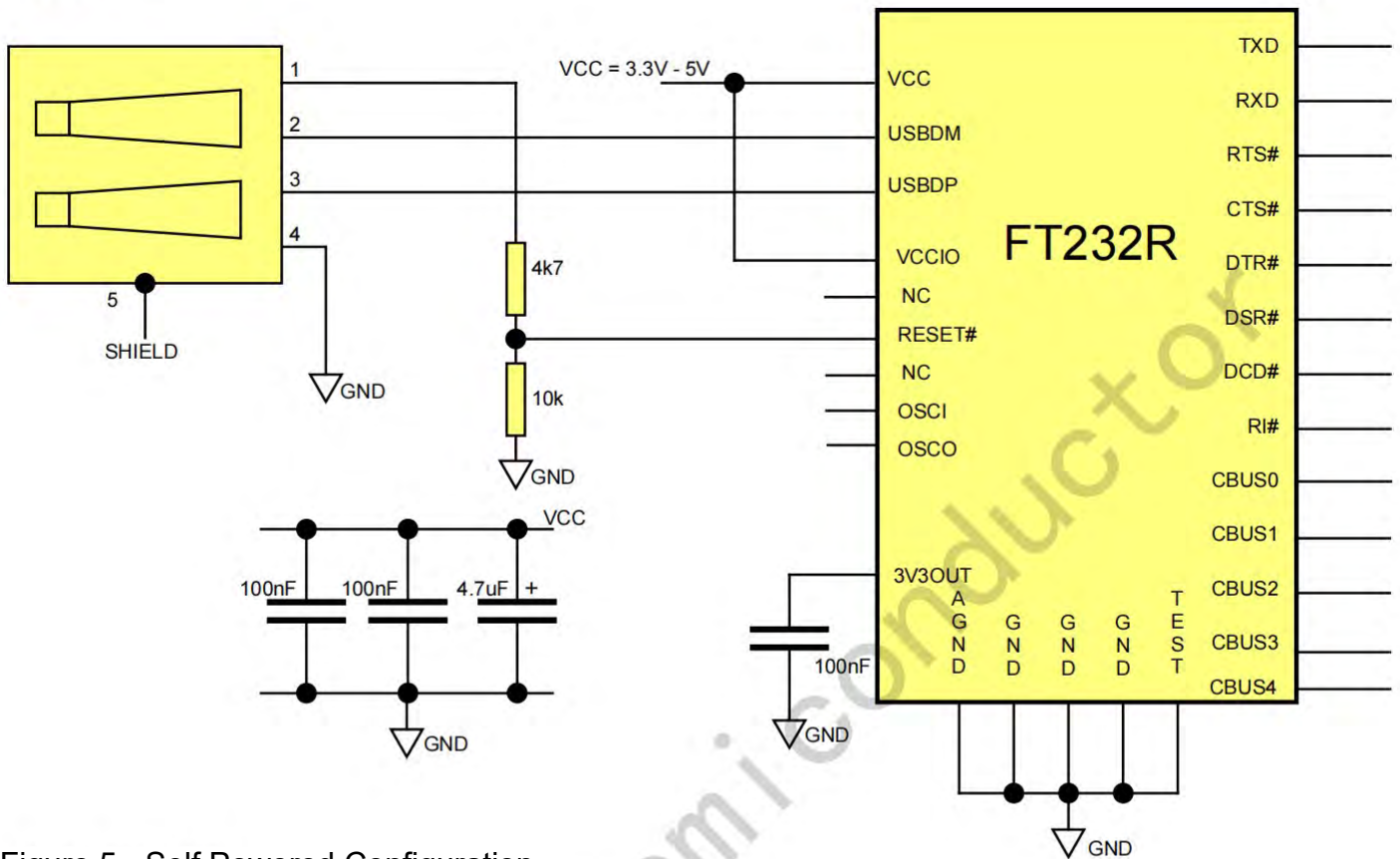


Figure 5 - Self Powered Configuration

Figure 5 illustrates the FT232R in a typical USB self powered configuration. A USB Self Powered device gets its power from its own power supply and does not draw current from the USB bus. The basic rules for USB self powered devices are as follows –

- 1) A Self Powered device should not force current down the USB bus when the USB Host or Hub Controller is powered down.
- 2) A Self Powered Device can use as much current as it likes during normal operation and USB suspend as it has its own power supply.
- 3) A Self Powered Device can be used with any USB Host and both Bus and Self Powered USB Hubs.

The power descriptor in the internal EEPROM should be programmed to a value of zero (self powered).

In order to meet requirement (1) the USB Bus Power is used to control the RESET# Pin of the FT232R device. When the USB Host or Hub is powered up the internal 1.5kΩ resistor on USBDP is pulled up to 3.3V, thus identifying the device as a full speed device to USB. When the USB Host or Hub power is off, RESET# will go low and the device will be held in reset. As RESET# is low, the internal 1.5kΩ resistor will not be pulled up to 3.3V, so no current will be forced down USBDP via the 1.5kΩ pull-up resistor when the host or hub is powered down. Failure to do this may cause some USB host or hub controllers to power up erratically.

Note: When the FT232R is in reset, the UART interface pins all go tri-state. These pins have internal 200kΩ pull-up resistors to VCCIO, so they will gently pull high unless driven by some external logic.





USB Bus Powered with 3.3V / 5V Supply and Logic Drive / IO Supply Voltage

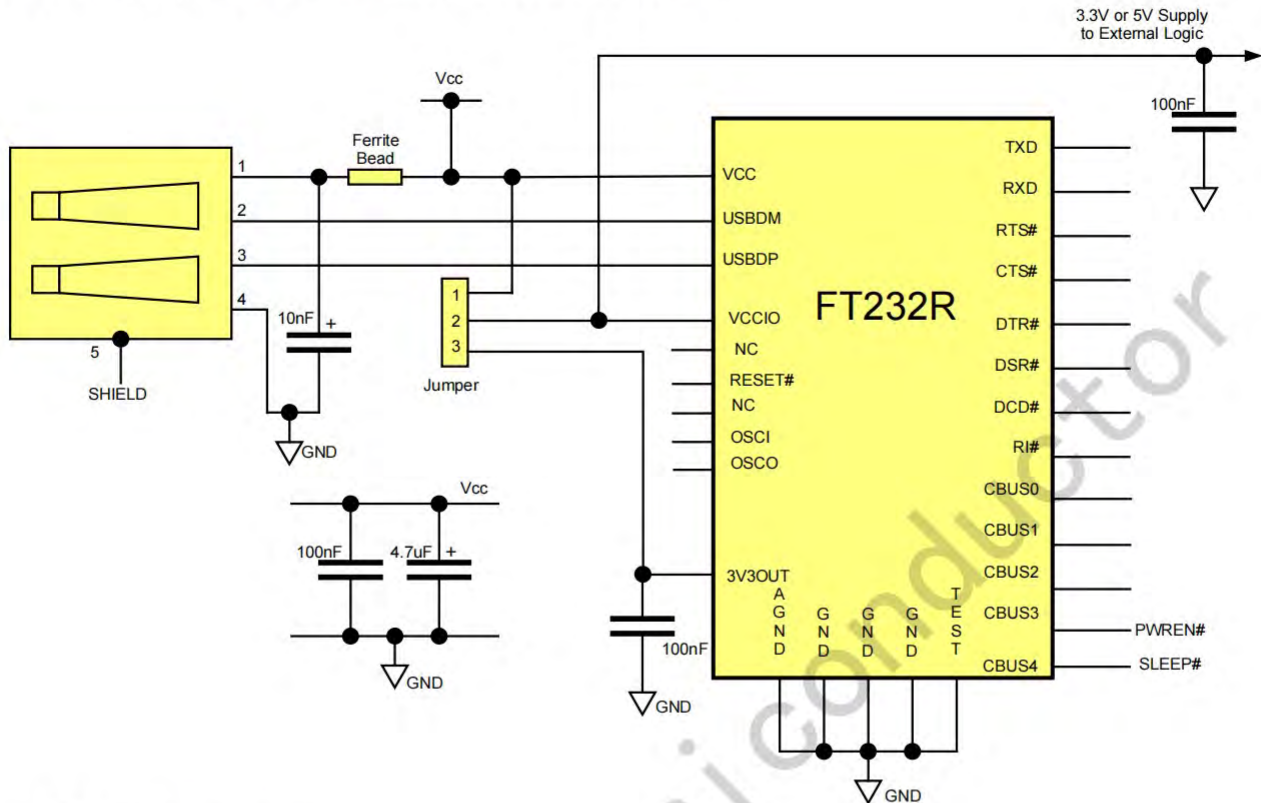


Figure 7 - Bus Powered with 3.3V / 5V Supply and Logic Drive

Figure 7 shows a configuration where a jumper switch is used to allow the FT232R to be interfaced with a 3.3V or 5V logic devices. The VCCIO pin is either supplied with 5V from the USB bus, or with 3.3V from the 3V3OUT pin. The supply to VCCIO is also used to supply external logic.

Please note the following in relation to bus powered designs of this type -

- 1) PWREN# or SLEEP# signals should be used to power down external logic during USB suspend mode, in order to comply with the limit of 500µA. If this is not possible, use the configuration shown in page 12
- 2) The maximum current source from USB Bus during normal operation should not exceed 100mA, otherwise a bus powered design with power switching (page 12) should be used.

Another possible configuration would be to use a discrete low dropout regulator which is supplied by the 5V on the USB bus to supply 2.8V - 1.8V to the VCCIO pin and to the external logic. VCC would be supplied with the 5V from the USB bus. With VCCIO connected to the output of the low dropout regulator, would in turn will cause the FT232R I/O pins to drive out at 2.8V - 1.8V logic levels.

For USB bus powered circuits some considerations have to be taken into account when selecting the regulator –

- 3) The regulator must be capable of sustaining its output voltage with an input voltage of 4.35V. A Low Drop Out (L.D.O.) regulator must be selected.
- 4) The quiescent current of the regulator must be low in order to meet the USB suspend total current requirement of <= 500µA during USB suspend.

An example of a regulator family that meets these requirements is the MicroChip TC55 Series of devices (www.microchip.com). These devices can supply up to 250mA current and have a quiescent current of under 1µA.

## 9. Example Interface Configurations

### 9.1 USB to RS232 Converter Configuration

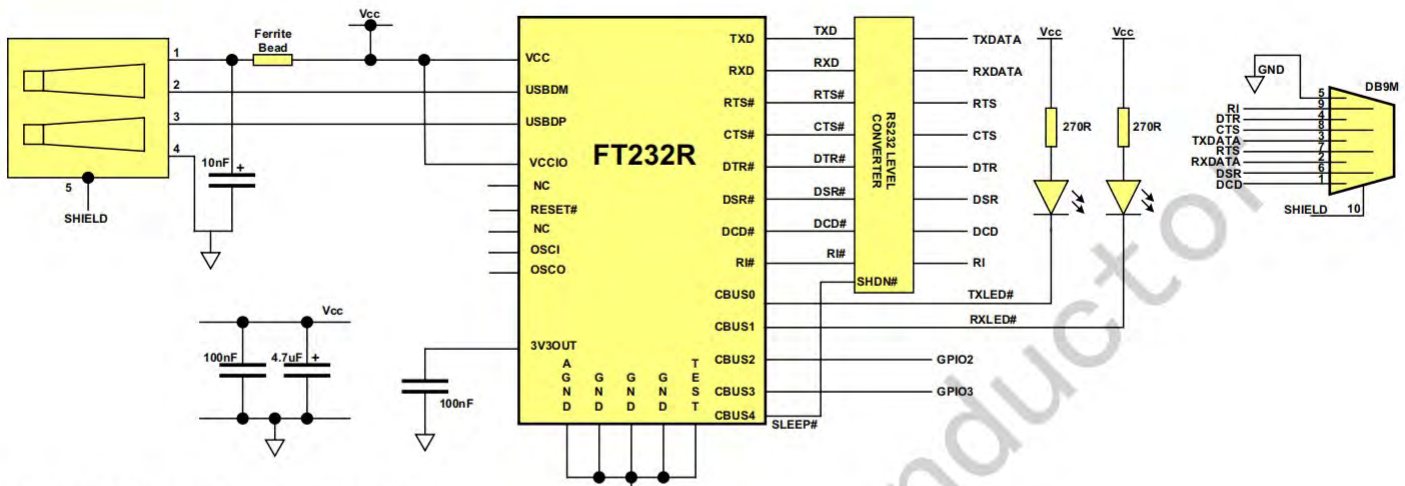


Figure 8 - Example USB to RS232 Converter Configuration

Figure 8 illustrates how to connect an FT232R as a USB to RS232 converter. A TTL – RS232 Level Converter I.C. is used on the serial UART of the FT232R to make the RS232 level conversion. This, for example can be done using the popular „213” series of TTL to RS232 level converters. These devices have 4 transmitters and 5 receivers in a 28-LD SSOP package and feature an in-built voltage converter to convert the 5V (nominal) VCC to the +/- 9 volts required by RS232. An important feature of these devices is the SHDN# pin which can power down the device to a low quiescent current during USB suspend mode.

An example of a device which can be used for this is a Sipex SP213EHCA which is capable of RS232 communication at up to 500kbaud. If a lower baud rate is acceptable, then several pin compatible alternatives are available such as the Sipex SP213ECA, the Maxim MAX213CAI and the Analog Devices ADM213E, which are all good for communication at up to 115,200 baud. If a higher baud rate is desired, use a Maxim MAX3245CAI part which is capable of RS232 communication at rates of up to 1M baud. The MAX3245 is not pin compatible with the 213 series devices, also its SHDN pin is active high, so connect it to PWREN# instead of SLEEP#.

In the above example CBUS0 and CBUS1 have been configured as TXLED# and RXLED#, and are being used to drive two LEDs.

9.2 USB to RS485 Converter Configuration

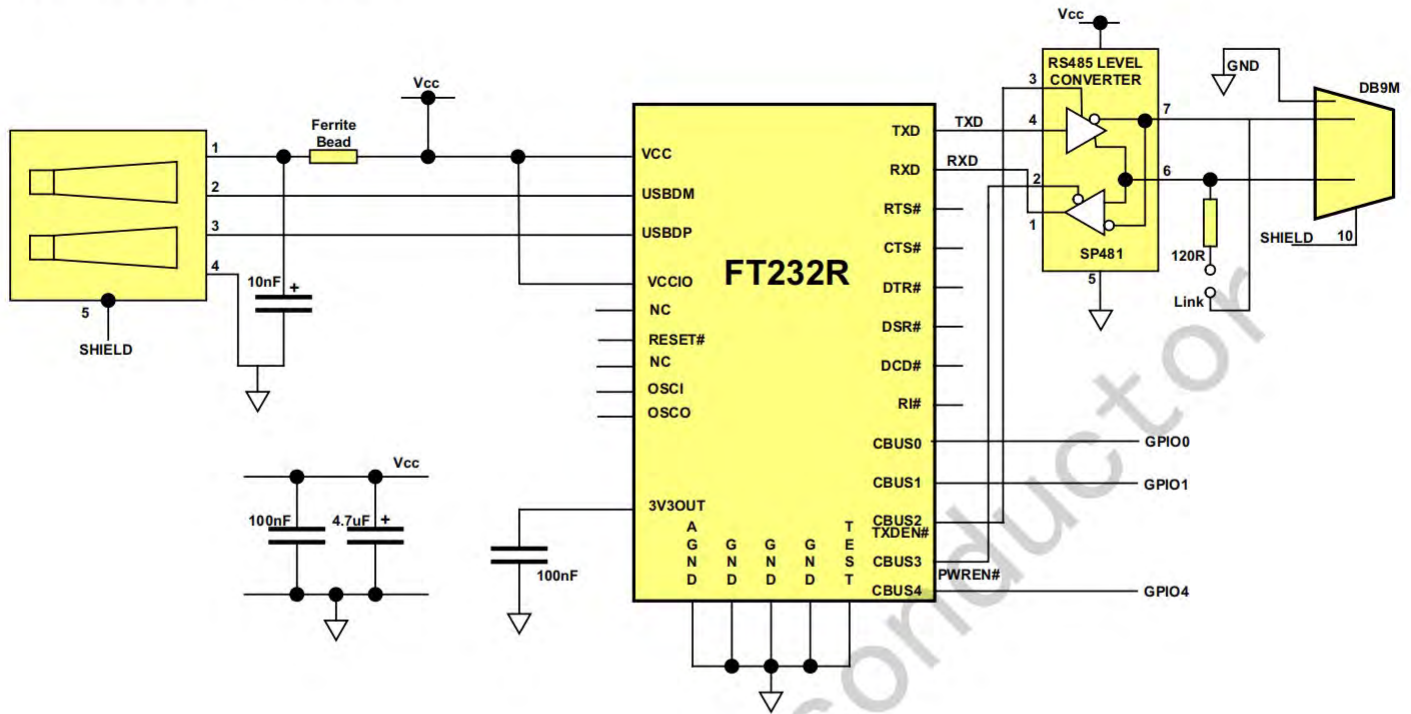


Figure 9 - Example USB to RS485 Converter Configuration

Figure 9 illustrates how to connect the FT232R's UART interface to a TTL – RS485 Level Converter I.C. to make a USB to RS485 converter. This example uses the Sipex SP481 device but there are similar parts available from Maxim and Analog Devices amongst others. The SP481 is a RS485 device in a compact 8 pin SOP package. It has separate enables on both the transmitter and receiver. With RS485, the transmitter is only enabled when a character is being transmitted from the UART. The TXDEN signal CBUS pin option on the FT232R is provided for exactly this purpose and so the transmitter enable is wired to CBUS2 which has been configured as TXDEN. Similarly, CBUS3 has been configured as PWREN#. This signal is used to control the SP481's receiver enable. The receiver enable is active low, so it is wired to the PWREN# pin to disable the receiver when in USB suspend mode. CBUS2 = TXDEN and CBUS3 = PWREN# are the default device configurations of these pins.

RS485 is a multi-drop network – i.e. many devices can communicate with each other over a single two wire cable connection. The RS485 cable requires to be terminated at each end of the cable. A link is provided to allow the cable to be terminated if the device is physically positioned at either end of the cable.

In this example the data transmitted by the FT232R is also received by the device that is transmitting. This is a common feature of RS485 and requires the application software to remove the transmitted data from the received data stream. With the FT232R it is possible to do this entirely in hardware – simply modify the schematic so that RXD of the FT232R is the logical OR of the SP481 receiver output with TXDEN using an HC32 or similar logic gate.



### 9.3 USB to RS422 Converter Configuration

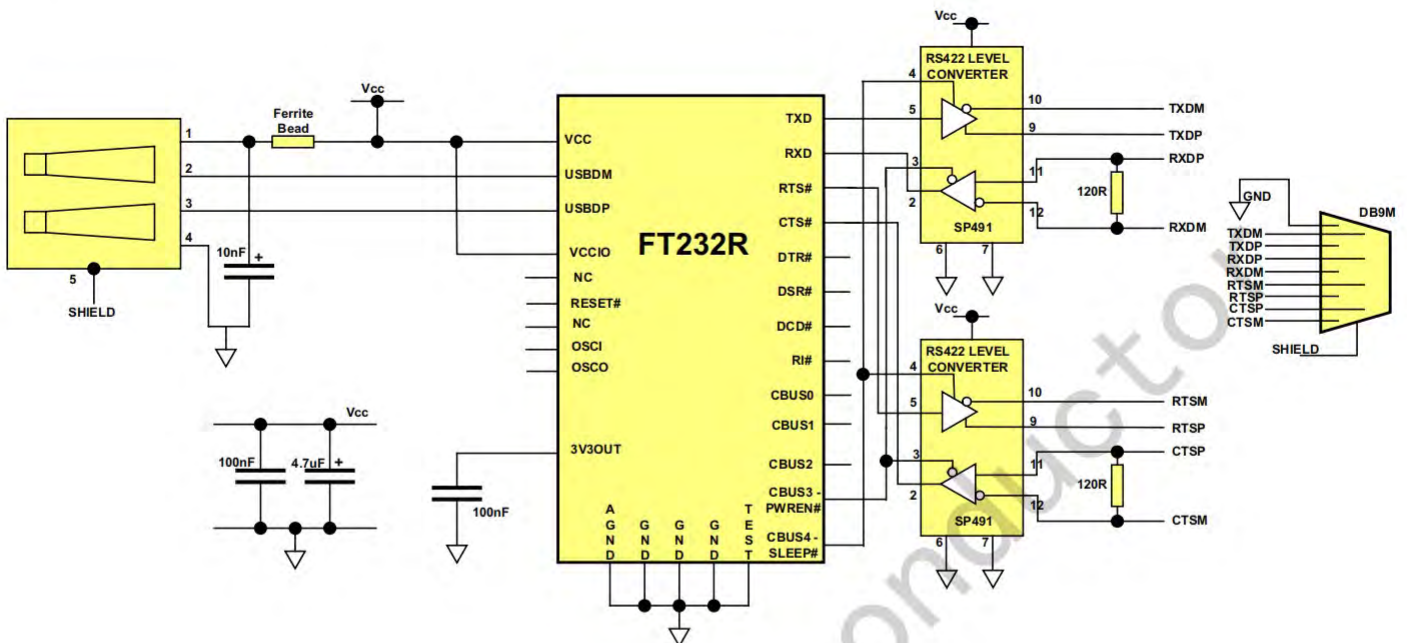


Figure 10 - Example USB to RS422 Converter Configuration

Figure 10 illustrates how to connect the UART interface of the FT232R to a TTL – RS422 Level Converter I.C. to make a USB to RS422 converter. There are many such level converter devices available – this example uses Sipex SP491 devices which have enables on both the transmitter and receiver. Because the transmitter enable is active high, it is connected to a CBUS pin in SLEEP# configuration. The receiver enable is active low and so is connected to a CBUS pin PWREN# configuration. This ensures that both the transmitters and receivers are enabled when the device is active, and disabled when the device is in USB suspend mode. If the design is USB BUS powered, it may be necessary to use a P-Channel logic level MOSFET (controlled by PWREN#) in the VCC line of the SP491 devices to ensure that the USB stand-by current of 500µA is met.

The SP491 is good for sending and receiving data at a rate of up to 5 Megbaud – in this case the maximum rate is limited to 3 Megbaud by the FT232R.

9.4 USB to MCU UART Interface

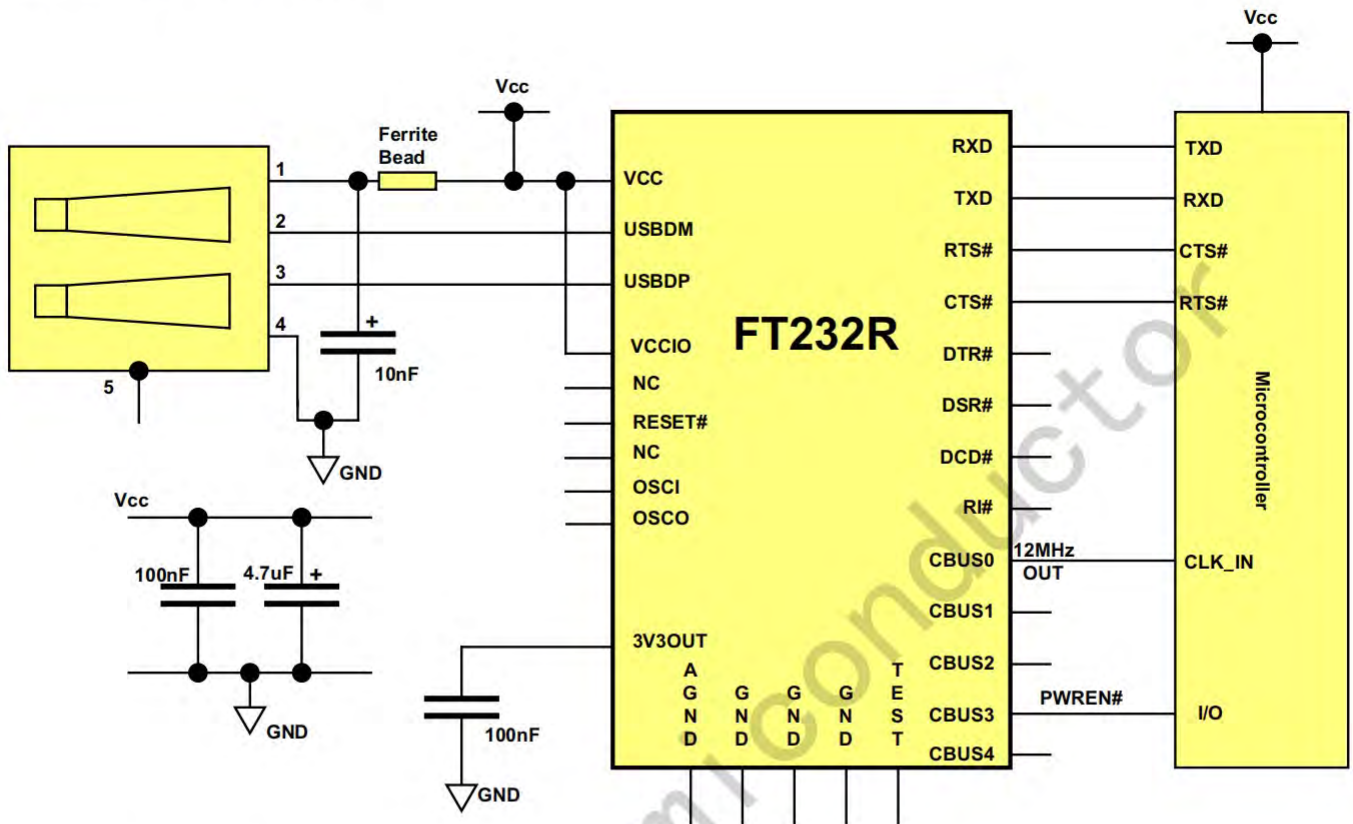


Figure 11 - Example USB to MCU UART Interface

Figure 11 is an example of interfacing the FT232R to a Microcontroller (MCU) UART interface. This example uses TXD and RXD for transmission and reception of data, and RTS# / CTS# hardware handshaking. Also in this example CBUS0 has been configured as a 12MHz output which is being used to clock the MCU.

Optionally, RI# can be connected to another I/O pin on the MCU and could be used to wake up the USB host controller from suspend mode. If the MCU is handling power management functions, then a CBUS pin can be configured as PWREN# and should also be connected to an I/O pin of the MCU.

## 10. LED Interface

Any of the 5 CBUS I/O pins can be configured to drive an LED. The FT232R has 3 options for driving an LED - these are TXLED#, RXLED#, and TX&RXLED#.

Figure 12 - Dual LED Configuration

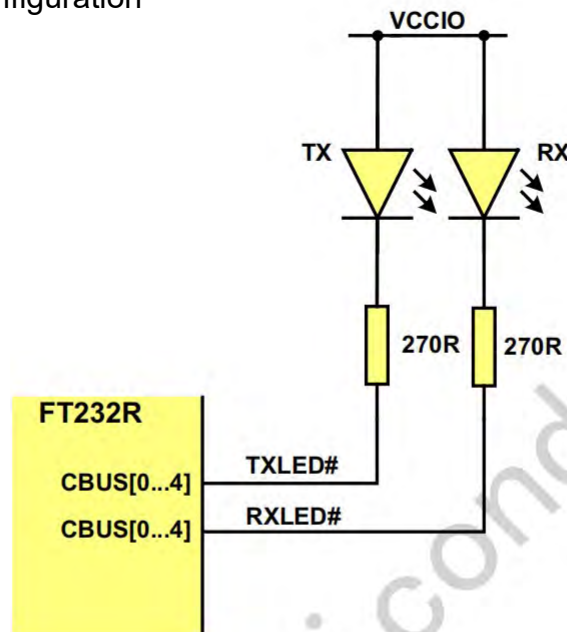


Figure 12 illustrates the configuration where one pin is used to indicate transmission of data (TXLED#) and another is used to indicate receiving data (RXLED#). When data is being transmitted or received the respective pins will drive from tri-state to low in order to provide indication on the LEDs of data transfer. A digital one-shot time is used so that even a small percentage of data transfer is visible to the end user.

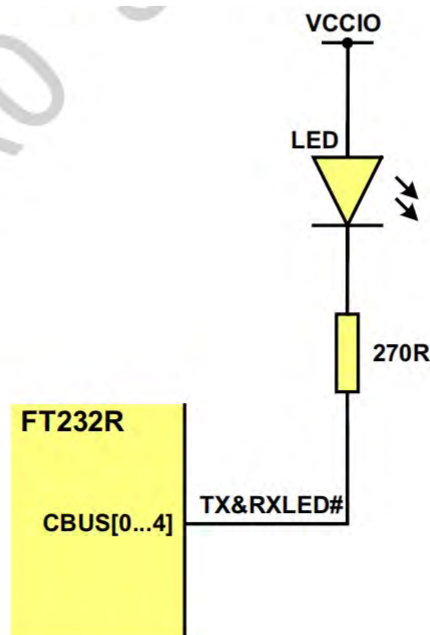


Figure 13 -Single LED Configuration

In figure 13 the TX&RXLED CBUS option is used. This option will cause the pin to drive a single LED when data is being transmitted or received by the device.



### Package Information

SSOP-28

