AFBR-5803Z/5803TZ/5803AZ/5803ATZ

FDDI, 100 Mb/s ATM, and Fast Ethernet Transceivers in Low-Cost 1 × 9 Package Style

Data Sheet

Description

The AFBR-5800Z family of transceivers from Broadcom® provide the system designer with products to implement a range of Fast Ethernet, FDDI, and Asynchronous Transfer Mode (ATM) designs at the 100 Mb/s-125 MBd rate.

The transceivers are all supplied in the industry standard 1 × 9 SIP package style with either a duplex SC or a duplex ST*[1] connector interface.

FDDI PMD, ATM and Fast Ethernet 2-km Backbone Links

The AFBR-5803Z/5803TZ are 1300-nm products with optical performance compliant with the FDDI PMD standard. The FDDI PMD standard is ISO/IEC 9314-3: 1990 and ANSI X3.166 – 1990.

These transceivers for 2-km multimode fiber backbones are supplied in the small 1 × 9 duplex SC or ST package style.

The AFBR-5803Z/5803TZ is useful for both ATM 100 Mb/s interfaces and Fast Ethernet 100BASE-FX interfaces. The ATM Forum User-Network Interface (UNI) Standard, Version 3.0, defines the Physical Layer for 100-Mb/s Multimode Fiber Interface for ATM in Section 2.3 to be the FDDI PMD Standard. Likewise, the Fast Ethernet Alliance defines the Physical Layer for 100BASE-FX for Fast Ethernet to be the FDDI PMD Standard.

ATM applications for physical layers other than 100-Mb/s Multimode Fiber Interface are supported by Broadcom. Products are available for both the single mode and the multi-mode fiber SONET OC-3c (STS-3c) ATM interfaces and the 155 Mb/s-194 MBd multi-mode fiber ATM interface as specified in the ATM Forum UNI.

Contact your Broadcom sales representative for information on these alternative Fast Ethernet, FDDI, and ATM products.

Features

- Full compatibility with the optical performance requirements of the FDDI PMD standard
- Full compatibility with the FDDI LCF-PMD standard
- Full compatibility with the optical performance requirements of the ATM 100-Mb/s physical layer
- Full compatibility with the optical performance requirements of 100BASE-FX version of IEEE802.3u
- Multisourced 1 × 9 package style with choice of duplex SC or duplex ST[1] receptacle
- Wave solder and aqueous wash process compatible
- Single +3.3V or +5V power supply
- RoHS compliance

Applications

- Multimode fiber backbone links
- Multimode fiber wiring closet to desktop links
- Very low cost multimode fiber links from wiring closet to desktop
- Multimode fiber media converters

1. ST is a registered trademark of AT&T Lightguide Cable Connectors

Transmitter Sections

The transmitter section of the AFBR-5803Z and AFBR-5805Z series usee 1300-nm surface-emitting InGaAsP LEDs. These LEDs are packaged in the optical subassembly portion of the transmitter section. They are driven by a custom silicon IC, which converts differential PECL logic signals, ECL referenced (shifted) to a +3.3V or +5V supply, into an analog LED drive current.

Receiver Sections

The receiver sections of the AFBR-5803Z and AFBR-5805Z series use InGaAs PIN photodiodes coupled to a custom silicon transimpedance preamplifier IC. These are packaged in the optical subassembly portion of the receiver.

These PIN/preamplifier combinations are coupled to a custom quantizer IC that provides the final pulse shaping for the logic output and the Signal Detect function. The data output is differential. The signal detect output is single-ended. Both data and signal detect outputs are PECL compatible, ECL referenced (shifted) to a +3.3V or +5V power supply.

Package

The overall package concept for the Broadcom transceivers consists of the following basic elements: two optical subassemblies, an electrical subassembly, and the housing as illustrated in Figure 1 and Figure 2.

The package outline drawings and pin out are shown in Figure 3, Figure 4, and Figure 5. The details of this package outline and pin out are compliant with the multi-source definition of the 1 × 9 SIP. The low profile of the Broadcom transceiver design complies with the maximum height allowed for the duplex SC connector over the entire length of the package.

The optical subassemblies use a high-volume assembly process together with low-cost lens elements that result in a cost effective building block.

The electrical subassembly consists of a high-volume multilayer printed circuit board on which the IC chips and various surface-mounted passive circuit elements are attached.

The package includes internal shields for the electrical and optical subassemblies to ensure low EMI emissions and high immunity to external EMI fields.

The outer housing including the duplex SC connector receptacle or the duplex ST ports is molded of filled nonconductive plastic to provide mechanical strength and electrical isolation. The solder posts of the Broadcom design are isolated from the circuit design of the transceiver and do not require connection to a ground plane on the circuit board.

The transceiver is attached to a printed circuit board with the nine signal pins and the two solder posts that exit the bottom of the housing. The two solder posts provide the primary mechanical strength to withstand the loads imposed on the transceiver by mating with duplex or simplex SC or ST connectored fiber cables.

Figure 1 SC Connector Block Diagram

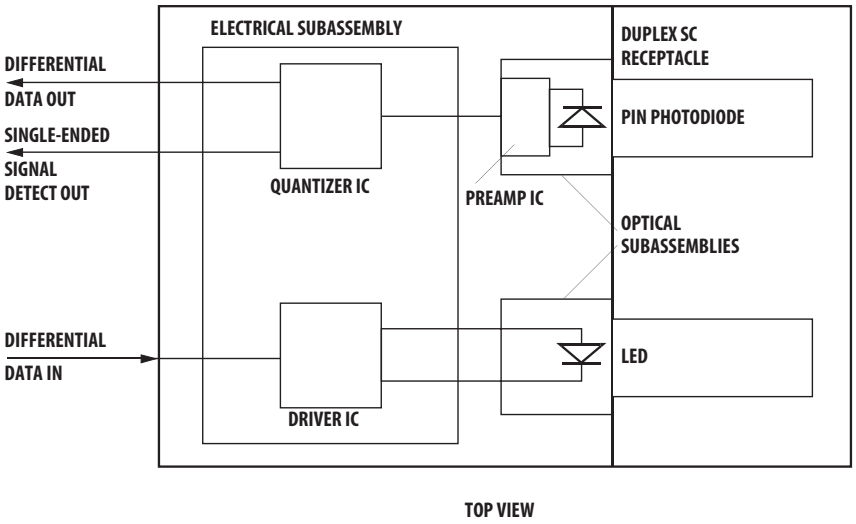


Figure 2 ST Connector Block Diagram

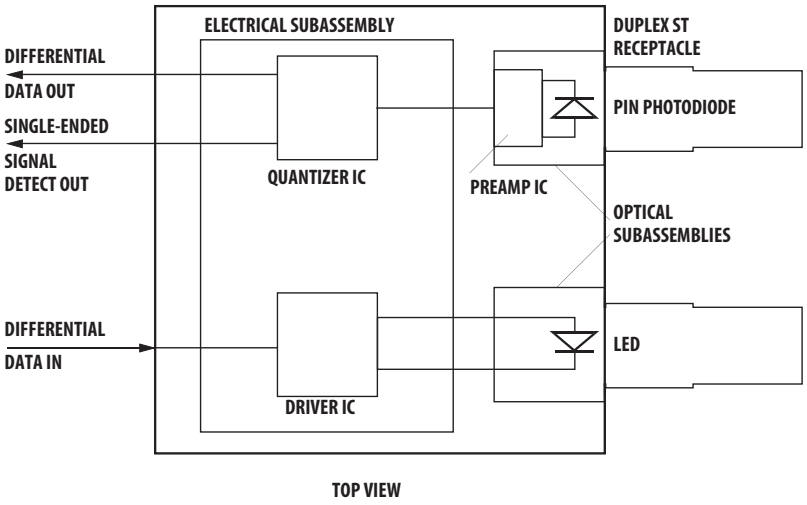
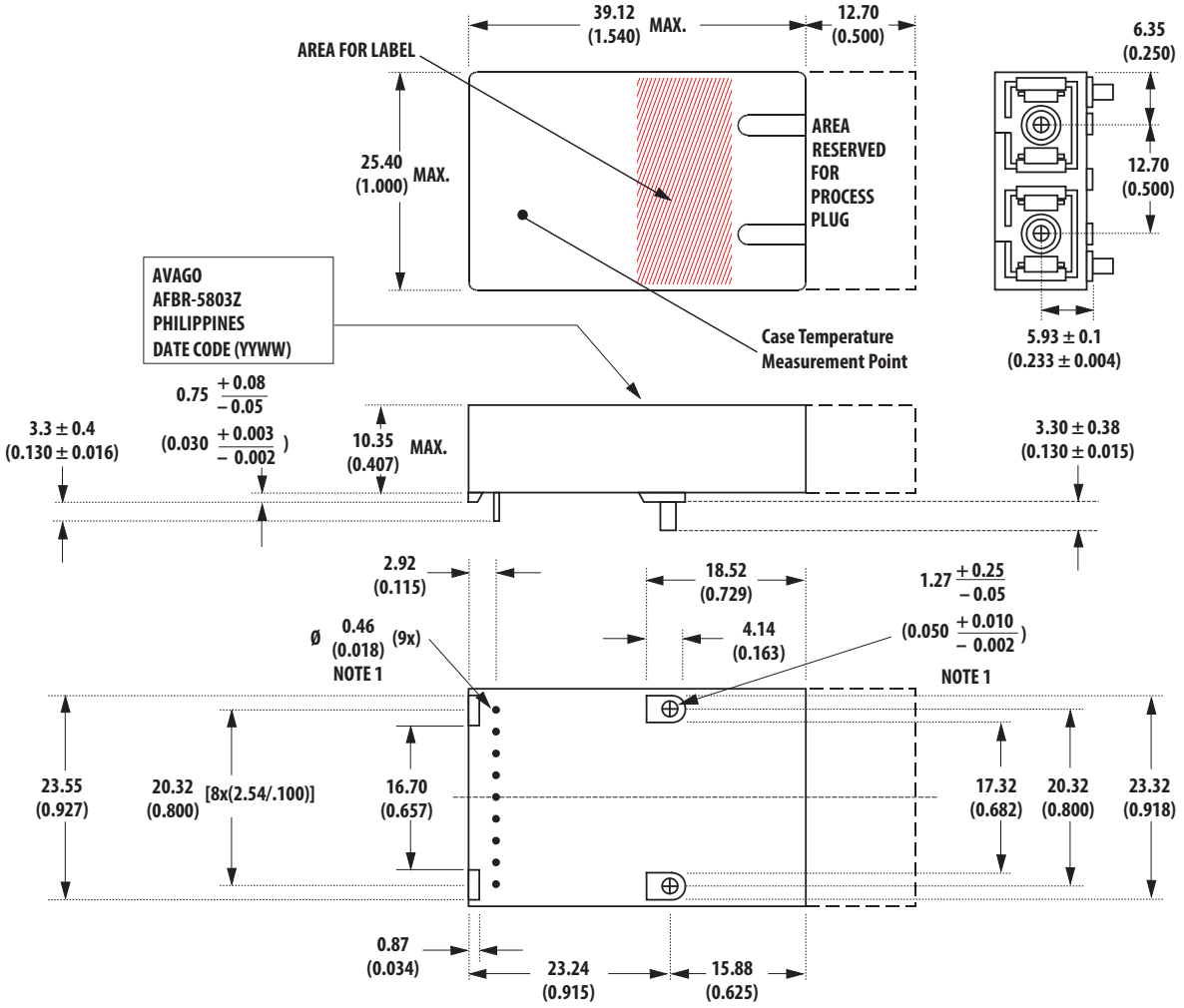


Figure 3 SC Connector Package Outline Drawing with Standard Height



Note 1: Phosphor bronze is the base material for the posts & pins. For lead-free soldering, the solder posts have Tin Copper over Nickel plating, and the electrical pins have pure Tin over Nickel plating.

DIMENSIONS ARE IN MILLIMETERS (INCHES).

Figure 4 ST Connector Package Outline Drawing with Standard Height

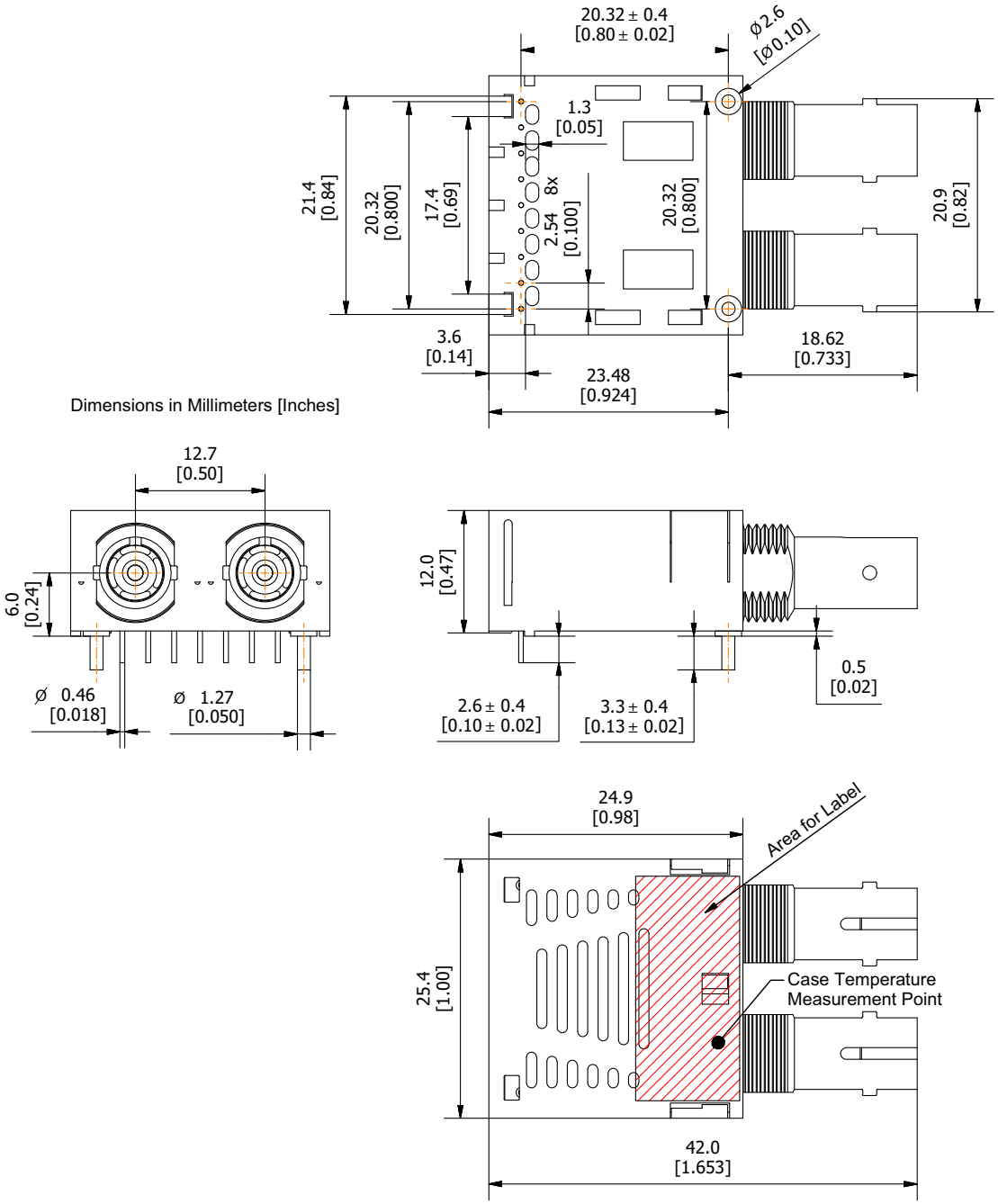
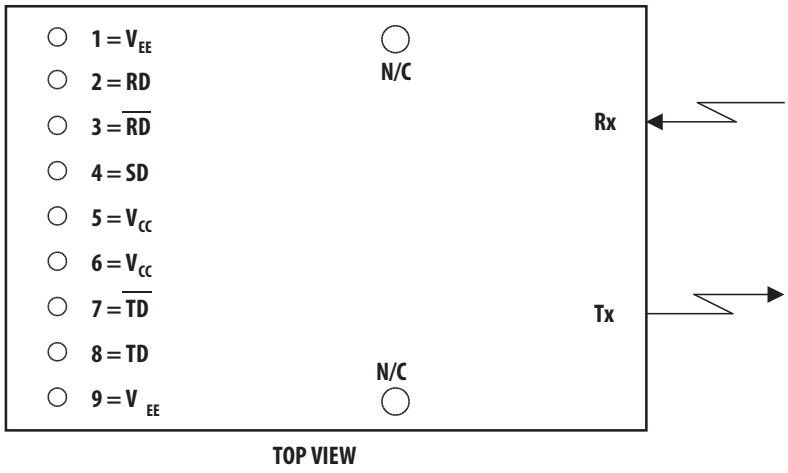


Figure 5 Pin Out Diagram



Application Information

The Applications Engineering group in the Broadcom Fiber Optics Communication Division is available to assist you with the technical understanding and design trade-offs associated with these transceivers. You can contact them through your Broadcom sales representative.

The following information is provided to answer some of the most common questions about the use of these parts.

Transceiver Optical Power Budget versus Link Length

Optical Power Budget (OPB) is the available optical power for a fiber-optic link to accommodate fiber cable losses plus losses due to inline connectors, splices, optical switches, and to provide margin for link aging and unplanned losses due to cable plant reconfiguration or repair.

Figure 6 illustrates the predicted OPB associated with the transceiver series specified in this data sheet at the Beginning of Life (BOL). These curves represent the attenuation and chromatic plus modal dispersion losses associated with the 62.5/125-µm and 50/125-µm fiber cables only. The area under the curves represents the remaining OPB at any link length, which is available for overcoming non-fiber cable-related losses.

Broadcom LED technology has produced 1300-nm LED devices with lower aging characteristics than normally associated with these technologies in the industry. The industry convention is 1.5-dB aging for 1300-nm LEDs. The Broadcom 1300-nm LEDs will experience less than 1dB of aging over normal commercial equipment mission life periods. Contact your Broadcom sales representative for additional details.

Figure 6 was generated with a Broadcom fiber-optic link model containing the current industry conventions for fiber cable specifications and the FDDI PMD and LCF-PMD optical parameters. These parameters are reflected in the guaranteed performance of the transceiver specifications in this data sheet. This same model has been used extensively in the ANSI and IEEE committees, including the ANSI X3T9.5 committee, to establish the optical performance requirements for various fiber optic interface standards. The cable parameters used come from the ISO/IEC JTC1/SC 25/WG3 Generic Cabling for Customer Premises per DIS 11801 document and the EIA/TIA-568-A Commercial Building Telecommunications Cabling Standard per SP-2840.

Transceiver Signaling Operating Rate Range and BER Performance

For purposes of definition, the symbol (Baud) rate, also called signaling rate, is the reciprocal of the shortest symbol time. Data rate (bits/s) is the symbol rate divided by the encoding factor used to encode the data (symbols/bit).

When used in Fast Ethernet, FDDI, and ATM 100-Mb/s applications, the performance of the 1300-nm transceivers is guaranteed over the signaling rate of 10 MBd to 125 MBd to the full conditions listed in individual product specification tables.

The transceivers may be used for other applications at signaling rates outside of the 10-MBd to 125-MBd range with some penalty in the link optical power budget primarily caused by a reduction of receiver sensitivity. Figure 7 gives an indication of the typical performance of these 1300-nm products at different rates.

These transceivers can also be used for applications that require different Bit Error Rate (BER) performance. Figure 8 illustrates the typical trade-off between link BER and the receivers' input optical power level.

Figure 6 Optical Power Budget at BOL vs. Fiber-Optic Cable Length

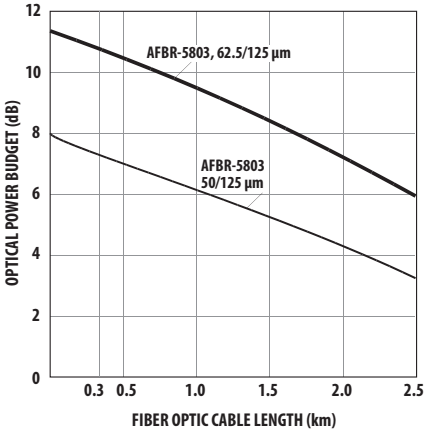
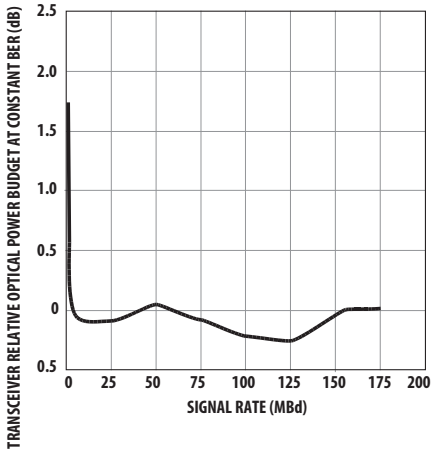
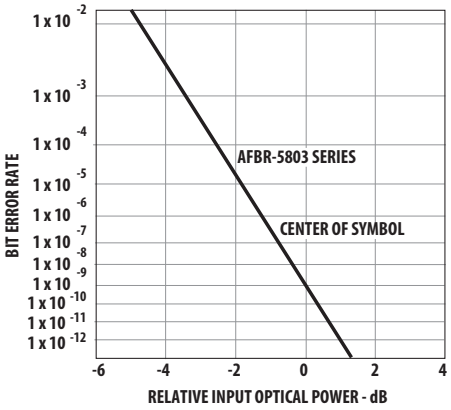


Figure 7 Transceiver Relative Optical Power Budget at Constant BER vs. Signaling Rate



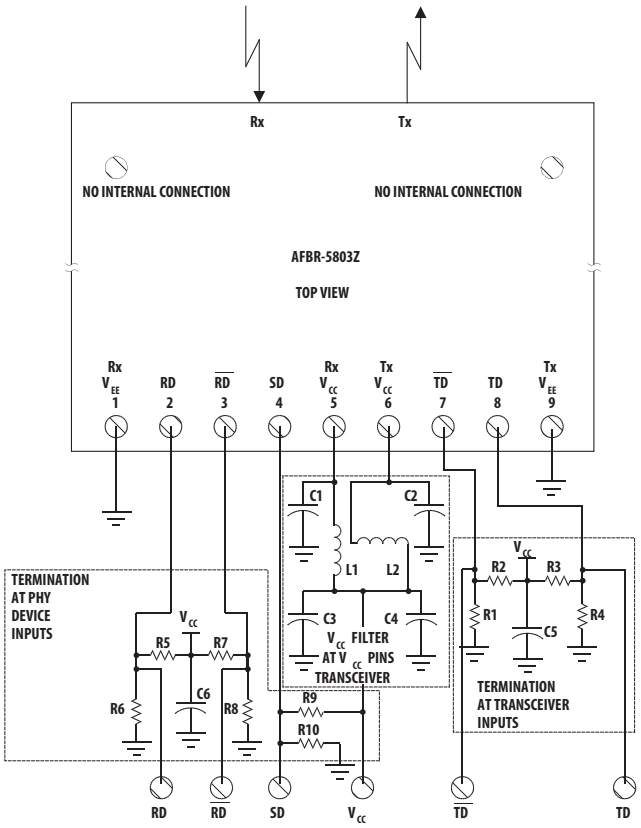
CONDITIONS:
1. PRBS 2^{7}-1
2. DATA SAMPLED AT CENTER OF DATA SYMBOL.
3. BER = 10^{-6}
4. T_A = +25° C
5. V_{CC} = 3.3 V to 5 V dc
6. INPUT OPTICAL RISE/FALL TIMES = 1.0/2.1 ns.

Figure 8 Bit Error Rate vs. Relative Receiver Input Optical Power



CONDITIONS:
1. 155 MBd
2. PRBS 2^{7}-1
3. CENTER OF SYMBOL SAMPLING
4. T_A = +25°C
5. V_{CC} = 3.3 V to 5 V dc
6. INPUT OPTICAL RISE/FALL TIMES = 1.0/2.1 ns.

Figure 9 Recommended Decoupling and Termination Circuits



NOTES:
THE SPLIT-LOAD TERMINATIONS FOR ECL SIGNALS NEED TO BE LOCATED AT THE INPUT OF DEVICES RECEIVING THOSE ECL SIGNALS. RECOMMEND 4-LAYER PRINTED CIRCUIT BOARD WITH 50 OHM MICROSTRIP SIGNAL PATHS BE USED.
R1 = R4 = R6 = R8 = R10 = 130 OHMS FOR +5.0 V OPERATION, 82 OHMS FOR +3.3 V OPERATION.
R2 = R3 = R5 = R7 = R9 = 82 OHMS FOR +5.0 V OPERATION, 130 OHMS FOR +3.3 V OPERATION.
C1 = C2 = C3 = C5 = C6 = 0.1 µF.
C4 = 10 µF.
L1 = L2 = 1 µH COIL OR FERRITE INDUCTOR.

Transceiver Jitter Performance

The Broadcom 1300-nm transceivers are designed to operate per the system jitter allocations stated in Tables E1 of Annexes E of the FDDI PMD and LCF-PMD standards.

The Broadcom 1300-nm transmitters will tolerate the worst-case input electrical jitter allowed in these tables without violating the worst case output jitter requirements of Sections 8.1 Active Output Interface of the FDDI PMD and LCF-PMD standards.

The Broadcom 1300-nm receivers will tolerate the worst-case input optical jitter allowed in Sections 8.2 Active Input Interface of the FDDI PMD and LCF-PMD standards without violating the worst case output electrical jitter allowed in the Tables E1 of the Annexes E.

The jitter specifications stated in the following 1300-nm transceiver specification tables are derived from the values in Tables E1 of Annexes E. They represent the worst-case jitter contribution that the transceivers are allowed to make to the overall system jitter without violating the Annex E allocation example. In practice the typical contribution of the Broadcom transceivers is well below these maximum allowed amounts.

Recommended Handling Precautions

Broadcom recommends that normal static precautions be taken in the handling and assembly of these transceivers to prevent damage that may be induced by electrostatic discharge (ESD). The AFBR-5800 series of transceivers meet MIL-STD-883C Method 3015.4 Class 2 products.

Care should be used to avoid shorting the receiver data or signal detect outputs directly to ground without proper current limiting impedance.

Solder and Wash Process Compatibility

The transceivers are delivered with protective process plugs inserted into the duplex SC or duplex ST connector receptacle. This process plug protects the optical subassemblies during wave solder and aqueous wash processing and acts as a dust cover during shipping.

These transceivers are compatible with either industry standard wave or hand solder processes.

Shipping Container

The transceiver is packaged in a shipping container designed to protect it from mechanical and ESD damage during shipment or storage.

Board Layout – Decoupling Circuit and Ground Planes

It is important to take care in the layout of your circuit board to achieve optimum performance from these transceivers. Figure 9 provides a good example of a schematic for a power supply decoupling circuit that works well with these parts. It is further recommended that a contiguous ground plane be provided in the circuit board directly under the transceiver to provide a low inductance ground for signal return current. This recommendation is in keeping with good high-frequency board layout practices.

Board Layout – Hole Pattern

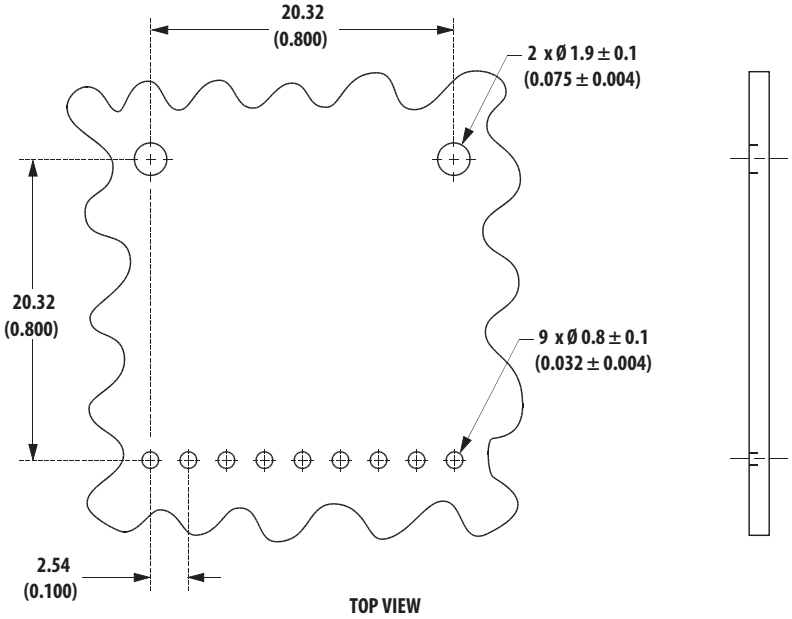
The Broadcom transceiver complies with the circuit board "Common Transceiver Footprint" hole pattern defined in the original multisource announcement that defined the 1 × 9 package style. This drawing is reproduced in Figure 10 with the addition of ANSI Y14.5M compliant dimensioning to be used as a guide in the mechanical layout of your circuit board.

Board Layout – Mechanical

For applications providing a choice of either a duplex SC or a duplex ST connector interface, while using the same pinout on the printed circuit board, the ST port needs to protrude from the chassis panel a minimum of 9.53 mm for sufficient clearance to install the ST connector.

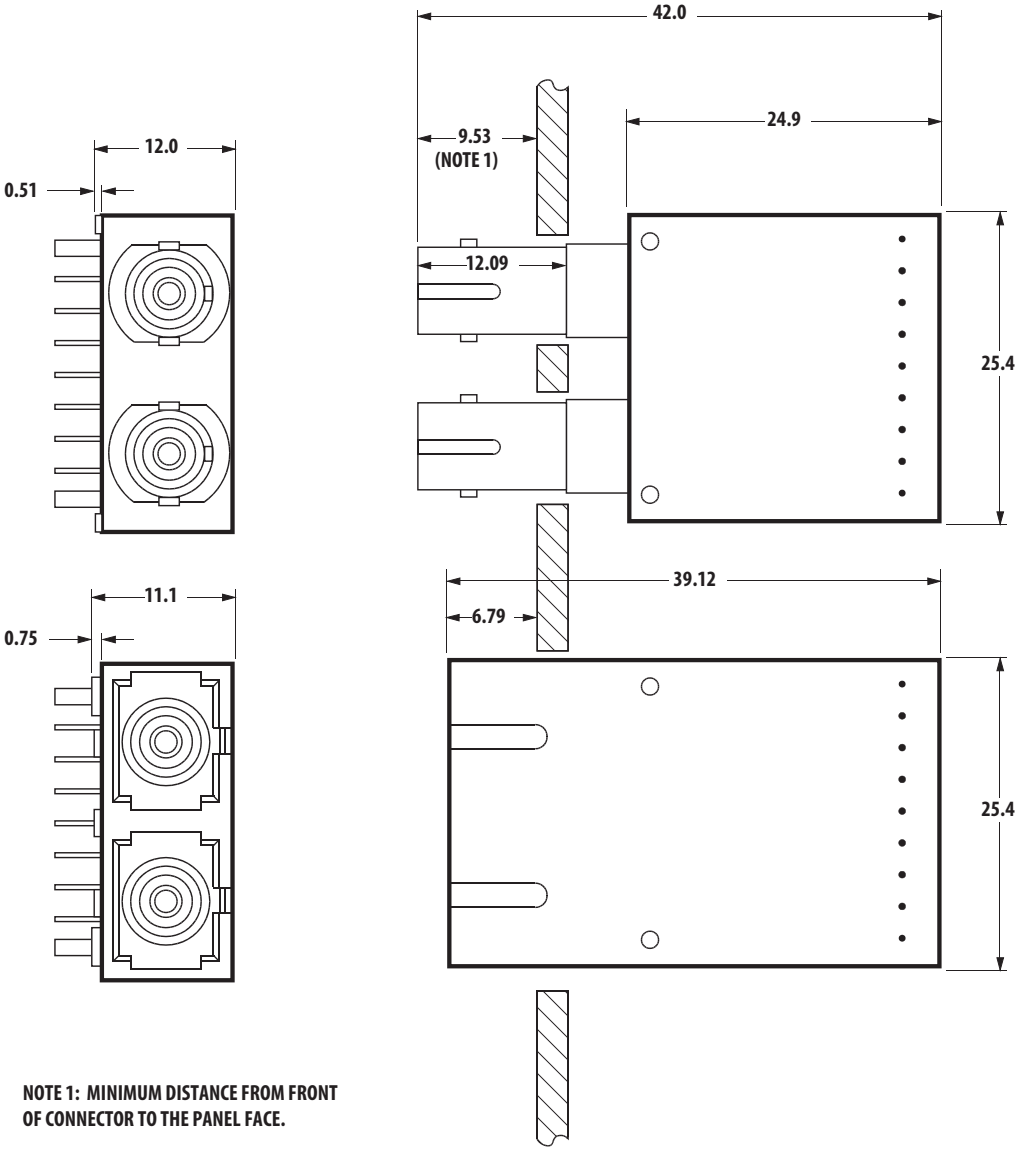
See Figure 11 for a mechanical layout detailing the recommended location of the duplex SC and duplex ST transceiver packages in relation to the chassis panel.

Figure 10 Recommended Board Layout Hole Pattern



DIMENSIONS ARE IN MILLIMETERS (INCHES)

Figure 11 Recommended Common Mechanical Layout for SC and ST 1 × 9 Connectored Transceivers



Regulatory Compliance

These transceiver products are intended to enable commercial system designers to develop equipment that complies with the various international regulations governing certification of Information Technology Equipment. See the Regulatory Compliance Table for details. Additional information is available from your Broadcom sales representative.

Electrostatic Discharge (ESD)

Immunity to ESD damage is important in two cases.

The first case is during handling of the transceiver prior to mounting it on the circuit board. It is important to use normal ESD-handling precautions for ESD-sensitive devices. These precautions include using grounded wrist straps, work benches, and floor mats in ESD-controlled areas.

The second case to consider is static discharges to the exterior of the equipment chassis containing the transceiver parts. To the extent that the duplex SC connector is exposed to the outside of the equipment chassis, it may be subject to whatever ESD system level test criteria that the equipment is intended to meet.

Regulatory Compliance Table

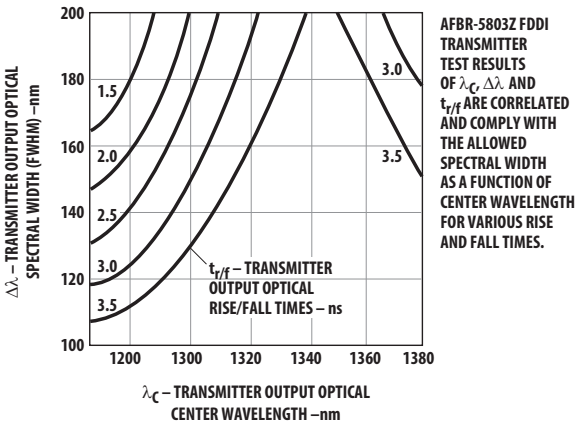
Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883 C Method 3015.4	Meets Class 1 (<1999 Volts) Withstand up to 1500V applied between electrical pins.
Electrostatic Discharge (ESD) to the Duplex SC Receptacle	Variation of IEC 801-2	Typically withstand at least 25 kV without damage when the duplex SC connector receptacle is contacted by a Human Body Model probe.
Electromagnetic Interference (EMI)	FCC Class B CENELEC CEN55022 Class B (CISPR 22B) VCCI Class 2	Transceivers typically provide a 13-dB margin (with duplex SC receptacle) or a 9-dB margin (with duplex ST receptacles) to the noted standard limits. However, it should be noted that final margin depends on the customer's board and chassis design.
Immunity	Variation of IEC 61000-4-3	Typically show no measurable effect from a 10-V/m field swept from 10 MHz to 450 MHz applied to the transceiver when mounted to a circuit card without a chassis enclosure.

Electromagnetic Interference (EMI)

Most equipment designs using these high-speed transceivers from Broadcom will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe, and VCCI in Japan.

In all well-designed chassis, two 0.5-in. holes for ST connectors to protrude through will provide 4.6-dB more shielding than one 1.2-in. duplex SC rectangular cutout. Thus, in a well-designed chassis, the duplex ST 1 × 9 transceiver emissions will be identical to the duplex SC 1 × 9 transceiver emissions.

Figure 12 Transmitter Output Optical Spectral Width (FWHM) vs. Transmitter Output Optical Center Wavelength and Rise/Fall Times



Immunity

Equipment using these transceivers will be subject to radio-frequency electromagnetic fields in some environments. These transceivers have a high immunity to such fields.

For additional information regarding EMI, susceptibility, ESD and conducted noise testing procedures and results on the 1 × 9 Transceiver family, refer to Application Note 1075, *Testing and Measuring Electromagnetic Compatibility Performance of the AFBR-510X/520X Fiber Optic Transceivers*.

Transceiver Reliability and Performance Qualification Data

The 1 × 9 transceivers have passed Broadcom reliability and performance qualification testing and are undergoing ongoing quality monitoring. Details are available from your Broadcom sales representative.

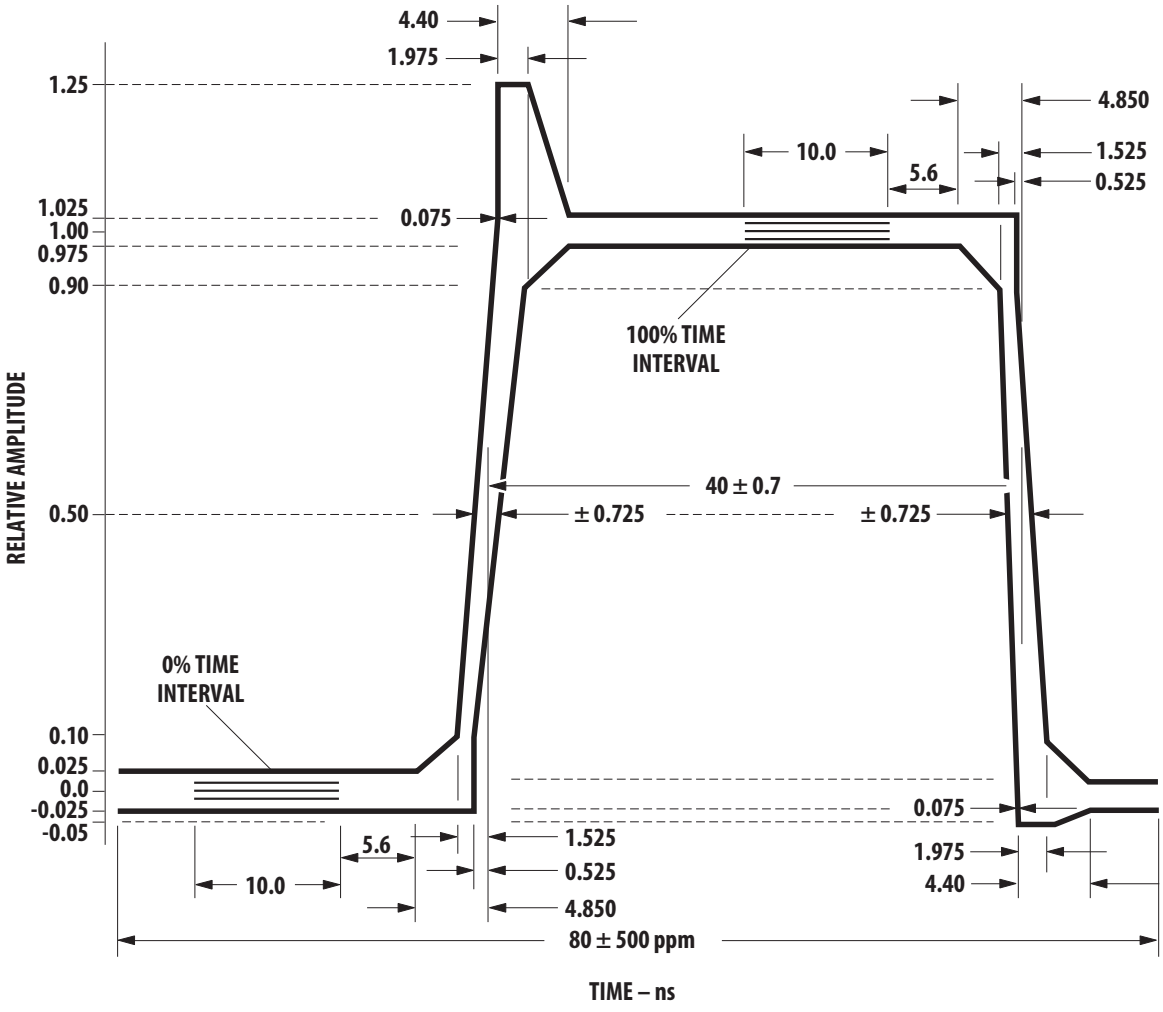
Accessory Duplex SC Connectored Cable Assemblies

Broadcom recommends for optimal coupling the use of flexible-body duplex SC connectored cable.

Accessory Duplex ST Connectored Cable Assemblies

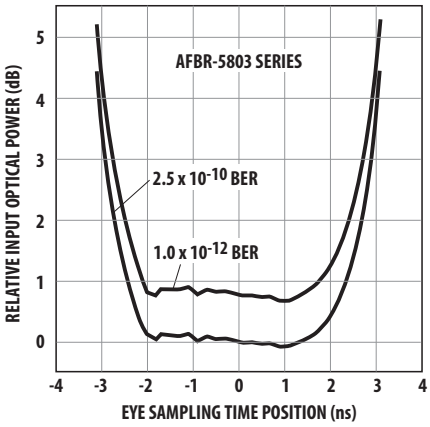
Broadcom recommends the use of duplex push-pull connectored cable for the most repeatable optical power coupling performance.

Figure 13 Output Optical Pulse Envelope



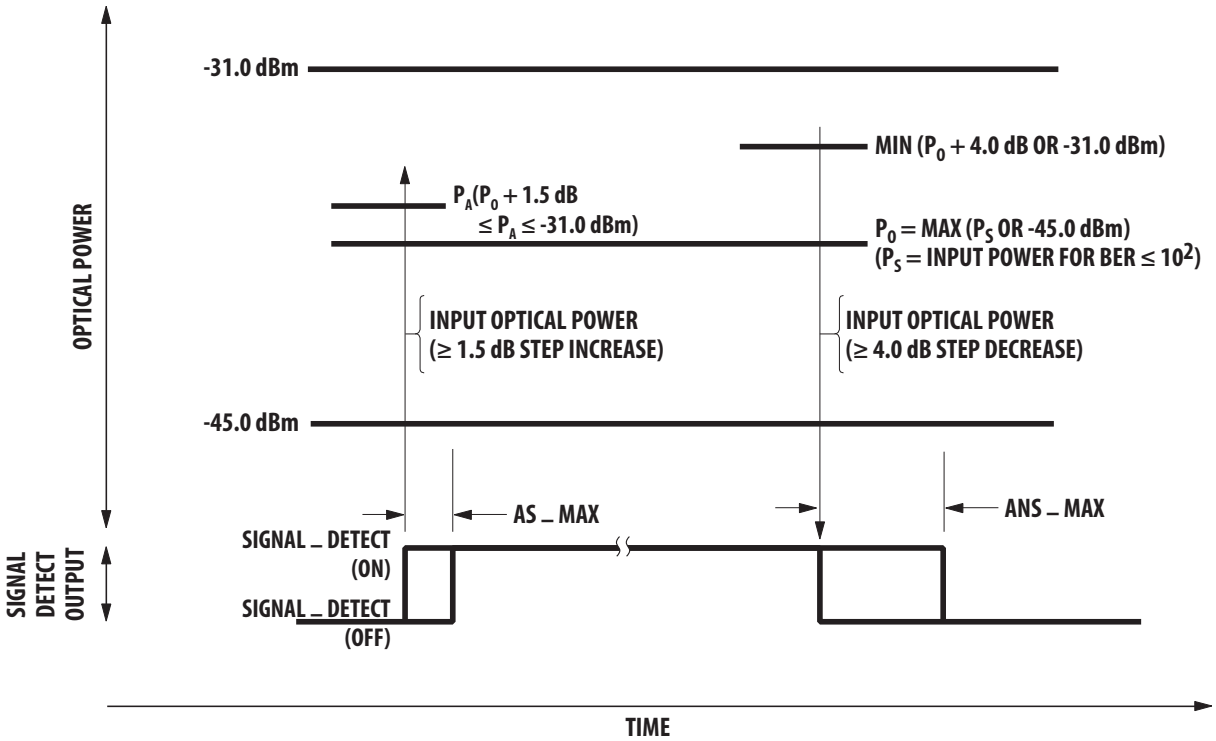
THE AFBR-5803Z OUTPUT OPTICAL PULSE SHAPE SHALL FIT WITHIN THE BOUNDARIES OF THE PULSE ENVELOPE FOR RISE AND FALL TIME MEASUREMENTS.

Figure 14 Relative Input Optical Power vs. Eye Sampling Time Position



CONDITIONS:
1.T_A = 25 C
2. V_{CC} = 5 Vdc
3. INPUT OPTICAL RISE/FALL TIMES = 1.0/2.1 ns.
4. INPUT OPTICAL POWER IS NORMALIZED TO CENTER OF DATA SYMBOL.
5. NOTE 20 AND 21 APPLY.

Figure 15 Signal Detect Thresholds and Timing



AS _ MAX — MAXIMUM ACQUISITION TIME (SIGNAL).
AS _ MAX IS THE MAXIMUM SIGNAL _ DETECT ASSERTION TIME FOR THE STATION.
AS _ MAX SHALL NOT EXCEED 100.0 µs. THE DEFAULT VALUE OF AS _ MAX IS 100.0 µs.

ANS _ MAX — MAXIMUM ACQUISITION TIME (NO SIGNAL).
ANS _ MAX IS THE MAXIMUM SIGNAL _ DETECT DEASSERTION TIME FOR THE STATION.
ANS _ MAX SHALL NOT EXCEED 350 µs. THE DEFAULT VALUE OF AS _ MAX IS 350 µs.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause catastrophic damage to the device. Limits apply to each parameter in isolation, all other parameters having values within the recommended operating conditions. It should not be assumed that limiting values of more than one parameter can be applied to the product at the same time. Exposure to the absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min.	Typ.	Max.	Units	Note
Storage Temperature	T_S	–40	—	+100	°C	
Lead Soldering Temperature	T_{SOLD}	—	—	+260	°C	
Lead Soldering Time	t_{SOLD}	—	—	10	sec.	
Supply Voltage	V_{CC}	–0.5	—	7.0	V	
Data Input Voltage	V_I	–0.5	—	V_{CC}	V	
Differential Input Voltage	V_D	—	—	1.4	V	a
Output Current	I_O	—	—	50	mA	

a. This is the maximum voltage that can be applied across the Differential Transmitter Data Inputs to prevent damage to the input ESD protection circuit.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Note
Ambient Operating Temperature						
■ AFBR-5803Z/5803TZ	T_A	0	—	+70	°C	a
■ AFBR-5803AZ/AFBR-5803ATZ	T_A	–10	—	+85	°C	b
Supply Voltage	V_{CC}	3.135	—	3.5	V	
	V_{CC}	4.75	—	5.25	V	
Data Input Voltage – Low	$V_IL - V_{CC}$	–1.810	—	–1.475	V	
Data Input Voltage – High	$V_{IH} - V_{CC}$	–1.165	—	–0.880	V	
Data and Signal Detect Output Load	R_L	—	50	—	Ω	c

a. Ambient Operating Temperature corresponds to transceiver case temperature of –40°C mininum to +100°C maximum with necessary airflow applied. Recommended case temperature measurement point can be found in Figure 3.

b. Ambient Operating Temperature corresponds to transceiver case temperature of –10°C mininum to +100°C maximum with necessary airflow applied. Recommended case temperature measurement point can be found in Figure 3.

c. The outputs are terminated with 50Ω connected to V_{CC} – 2V.

Transmitter Electrical Characteristics

(AFBR-5803Z/AFBR-5803TZ: T_A = 0°C to +70°C, V_{CC} = 3.135V to 3.5V or 4.75V to 5.25V.)
(AFBR-5803AZ/AFBR-5803ATZ: T_A = –10°C to +85°C, V_{CC} = 3.135V to 3.5V or 4.75V to 5.25V

Parameter		Symbol	Min.	Typ.	Max.	Units	Note
Supply Current		I_{CC}	—	133	175	mA	a
Power Dissipation	at V_{CC} = 3.3V	P_{DISS}	—	0.45	0.6	W	
	at V_{CC} = 5.0V	P_{DISS}	—	0.76	0.97	W	
Data Input Current – Low		I_{IL}	–350	–2	—	µA	
Data Input Current – High		I_{IH}	—	18	350	µA	

a. The power supply current needed to operate the transmitter is provided to differential ECL circuitry. This circuitry maintains a nearly constant current flow from the power supply. Constant current operation helps to prevent unwanted electrical noise from being generated and conducted or emitted to neighboring circuitry.

Receiver Electrical Characteristics

(AFBR-5803Z/AFBR-5803TZ: T_A = 0°C to +70°C, V_{CC} = 3.135V to 3.5V or 4.75V to 5.25V.)
(AFBR-5803AZ/AFBR-5803ATZ: T_A = –10°C to +85°C, V_{CC} = 3.135V to 3.5V or 4.75V to 5.25V.)

Parameter		Symbol	Min.	Typ.	Max.	Units	Note
Supply Current		I_{CC}	—	87	120	mA	a
Power Dissipation	at V_{CC} = 3.3V	P_{DISS}	—	0.15	0.25	W	b
	at V_{CC} = 5.0V	P_{DISS}	—	0.3	0.5	W	b
Data Output Voltage – Low		$V_{OL} – V_{CC}$	–1.83	—	–1.55	V	c
Data Output Voltage – High		$V_{OH} – V_{CC}$	–1.085	—	–0.88	V	c
Data Output Rise Time		t_r	0.35	—	2.2	ns	d
Data Output Fall Time		t_f	0.35	—	2.2	ns	d
Signal Detect Output Voltage – Low		$V_{OL} – V_{CC}$	–1.83	—	–1.55	V	c
Signal Detect Output Voltage – High		$V_OH – V_{CC}$	–1.085	—	–0.88	V	c
Signal Detect Output Rise Time		t_r	0.35	—	2.2	ns	d
Signal Detect Output Fall Time		t_f	0.35	—	2.2	ns	d

a. This value is measured with the outputs terminated into 50Ω connected to V_{CC} – 2V and an Input Optical Power level of –14 dBm average.

b. The power dissipation value is the power dissipated in the receiver itself. Power dissipation is calculated as the sum of the products of supply voltage and currents, minus the sum of the products of the output voltages and currents.

c. This value is measured with respect to V_{CC} with the output terminated into 50Ω connected to V_{CC} – 2V.

d. The output rise and fall times are measured between 20% and 80% levels with the output connected to V_{CC} – 2V through 50Ω.

Transceiver Optical Characteristics

(AFBR-5803Z/AFBR-5803TZ: T_A = 0°C to +70°C, V_{CC} = 3.135V to 3.5V or 4.75V to 5.25V.)
(AFBR-5803AZ/AFBR-5803ATZ: T_A = –10°C to +85°C, V_{CC} = 3.135V to 3.5V or 4.75V to 5.25V.)

Parameter		Symbol	Min.	Typ.	Max.	Units	Figure	Note
Output Optical Power 62.5/125 µm, NA = 0.275 Fiber	BOL EOL	P_O	–19 –20	—	–14	dBm avg.		a
Output Optical Power 50/125 µm, NA = 0.20 Fiber	BOL EOL	P_O	–22.5 –23.5	—	–14	dBm avg.		a
Optical Extinction Ratio			—	—	10 –10	% dB		b
Output Optical Power at Logic "0" State		P_O ("0")	—	—	–45	dBm avg.		c
Center Wavelength		λ_C	1270	1308	1380	nm		d
Spectral Width ■ FWHMS ■ nm RMS		$\Delta\lambda$	 — —	 147 63	 — —	 nm nm	12	d
Optical Rise Time		t_r	0.6	1.9	3.0	ns	12, 13	d, e
Optical Fall Time		t_f	0.6	1.6	3.0	ns	12, 130	d, e
Duty Cycle Distortion Contributed by the Transmitter		DCD	—	—	0.6	ns p-p		f
Data Dependent Jitter Contributed by the Transmitter		DDJ	—	—	0.6	ns p-p		g
Random Jitter Contributed by the Transmitter		RJ	—	—	0.69	ns p-p		h

a. These optical power values are measured with the following conditions:
— The Beginning of Life (BOL) to the End of Life (EOL) optical power degradation is typically 1.5 dB per the industry convention for long wavelength LEDs. The actual degradation observed in Broadcom 1300-nm LED products is < 1 dB, as specified in this data sheet.
— Over the specified operating voltage and temperature ranges.
— With HALT Line State, (12.5-MHz square-wave), input signal.
— At the end of one meter of noted optical fiber with cladding modes removed.
The average power value can be converted to a peak power value by adding 3 dB. Higher output optical power transmitters are available on special request.

b. The Extinction Ratio is a measure of the modulation depth of the optical signal. The data "0" output optical power is compared to the data "1" peak output optical power and expressed as a percentage. With the transmitter driven by a HALT Line State (12.5-MHz square-wave) signal, the average optical power is measured. The data "1" peak power is then calculated by adding 3 dB to the measured average optical power. The data "0" output optical power is found by measuring the optical power when the transmitter is driven by a logic "0" input. The extinction ratio is the ratio of the optical power at the "0" level compared to the optical power at the "1" level expressed as a percentage or in decibels.

c. The transmitter provides compliance with the need for Transmit_Disable commands from the FDDI SMT layer by providing an Output Optical Power level of < –45 dBm average in response to a logic "0" input. This specification applies to either 62.5/125-µm or 50/125-µm fiber cables.

d. This parameter complies with the FDDI PMD requirements for the trade-offs between center wavelength, spectral width, and rise/fall times shown in Figure 12.

e. This parameter complies with the optical pulse envelope from the FDDI PMD shown in Figure 13. The optical rise and fall times are measured from 10% to 90% when the transmitter is driven by the FDDI HALT Line State (12.5-MHz square-wave) input signal.

f. Duty Cycle Distortion contributed by the transmitter is measured at a 50% threshold using an IDLE Line State, 125 MBd (62.5-MHz square-wave), input signal. See Transceiver Jitter Performance for further details.

g. Data Dependent Jitter contributed by the transmitter is specified with the FDDI test pattern described in FDDI PMD Annex A.5. See Transceiver Jitter Performancet for further details.

h. Random Jitter contributed by the transmitter is specified with an IDLE Line State, 125 MBd (62.5-MHz square-wave), input signal. See Transceiver Jitter Performance for further details.

Receiver Optical and Electrical Characteristics

(AFBR-5803Z/AFBR-5803TZ: T_A = 0°C to +70°C, V_{CC} = 3.135V to 3.5V or 4.75V to 5.25V.)
(AFBR-5803AZ/AFBR-5803ATZ: T_A = –10°C to +85°C, V_{CC} = 3.135V to 3.5V or 4.75V to 5.25V.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Figure	Note
Input Optical Power Minimum at Window Edge	$P_{IN\ Min.}$ (W)	—	–33.9	–31	dBm avg.	14	a
Input Optical Power Minimum at Eye Center	$P_{IN\ Min.}$ (C)	—	–35.2	–31.8	dBm avg.	14	b
Input Optical Power Maximum	$P_{IN\ Max.}$	–14	—	—	dBm avg.		a
Operating Wavelength	λ	1270	—	1380	nm		
Duty Cycle Distortion Contributed by the Receiver	DCD	—	—	0.4	ns p-p		c
Data Dependent Jitter Contributed by the Receiver	DDJ	—	—	1.0	ns p-p		d
Random Jitter Contributed by the Receiver	RJ	—	—	2.14	ns p-p		e
Signal Detect – Asserted	P_A	P_D + 1.5 dB	—	–33	dBm avg.	15	f, g
Signal Detect – Deasserted	P_D	–45	—	—	dBm avg.	15	h, i
Signal Detect – Hysteresis	$P_A – P_D$	1.5	—	—	dB	15	
Signal Detect Assert Time (off to on)	AS_Max	0	2	100	µs	15	f, g
Signal Detect Deassert Time (on to off)	ANS_Max	0	8	350	µs	15	h, i

a. This specification is intended to indicate the performance of the receiver section of the transceiver when Input Optical Power signal characteristics are present per the following definitions. The Input Optical Power dynamic range from the minimum level (with a window time-width) to the maximum level is the range over which the receiver is guaranteed to provide output data with a Bit Error Ratio (BER) better than or equal to 2.5×10^{-10}.
— At the Beginning of Life (BOL)
— Over the specified operating temperature and voltage ranges
— Input symbol pattern is the FDDI test pattern defined in FDDI PMD Annex A.5 with 4B/5B NRZI encoded data that contains a duty cycle baseline wander effect of 50 kHz. This sequence causes a near worst-case condition for inter-symbol interference.
— Receiver data window time-width is 2.13 ns or greater and centered at mid-symbol. This worst-case window time-width is the minimum allowed eye-opening presented to the FDDI PHY PM. Data indication input (PHY input) per the example in FDDI PMD Annex E. This minimum window time-width of 2.13 ns is based upon the worst-case FDDI PMD Active Input Interface optical conditions for peak-to-peak DCD (1.0 ns), DDJ (1.2 ns) and RJ (0.76 ns) presented to the receiver.
To test a receiver with the worst case FDDI PMD Active Input jitter condition requires exacting control over DCD, DDJ, and RJ jitter components that is difficult to implement with production test equipment. The receiver can be equivalently tested to the worst-case FDDI PMD input jitter conditions and meet the minimum output data window time-width of 2.13 ns. This is accomplished by using a nearly ideal input optical signal (no DCD, insignificant DDJ and RJ) and measuring for a wider window time-width of 4.6 ns. This is possible due to the cumulative effect of jitter components through their superposition (DCD and DDJ are directly additive and RJ components are rms additive). Specifically, when a nearly ideal input optical test signal is used and the maximum receiver peak-to-peak jitter contributions of DCD (0.4 ns), DDJ (1.0 ns), and RJ (2.14 ns) exist, the minimum window time-width becomes 8.0 ns – 0.4 ns – 1.0 ns – 2.14 ns = 4.46 ns, or conservatively 4.6 ns. This wider window time-width of 4.6 ns guarantees the FDDI PMD Annex E minimum window time-width of 2.13 ns under worst-case input jitter conditions to the Broadcom receiver.
— Transmitter operating with an IDLE Line State pattern, 125 MBd (62.5-MHz square-wave), input signal to simulate any cross-talk present between the transmitter and receiver sections of the transceiver.

b. All conditions of Note a apply except that the measurement is made at the center of the symbol with no window time-width.

c. Duty Cycle Distortion contributed by the receiver is measured at the 50% threshold using an IDLE Line State, 125 MBd (62.5-MHz square-wave), input signal. The input optical power level is –20 dBm average. See Transceiver Jitter Performance for further information.

d. Data Dependent Jitter contributed by the receiver is specified with the FDDI DDJ test pattern described in the FDDI PMD Annex A.5. The input optical power level is –20 dBm average. See Transceiver Jitter Performance for further information.

e. Random Jitter contributed by the receiver is specified with an IDLE Line State, 125 MBd (62.5-MHz square-wave), input signal. The input optical power level is at maximum "$P_{IN\ Min.}$ (W)". See Transceiver Jitter Performance for further information.

f. This value is measured during the transition from low to high levels of input optical power.

g. The Signal Detect output shall be asserted within 100 µs after a step increase of the Input Optical Power. The step will be from a low Input Optical Power, –45 dBm, into the range between greater than P_A, and –14 dBm. The BER of the receiver output will be 10^{-2} or better during the time, LS_Max (15 µs) after Signal Detect has been asserted. See Figure 15 for more information.

h. This value is measured during the transition from high to low levels of input optical power. The maximum value will occur when the input optical power is either –45 dBm average or when the input optical power yields a BER of 10^{-2} or larger, whichever power is higher.

i. Signal detect output shall be deasserted within 350 µs after a step decrease in the Input Optical Power from a level that is the lower of; –31 dBm or P_D + 4 dB (P_D is the power level at which signal detect was deasserted), to a power level of –45 dBm or less. This step decrease will have occurred in less than 8 ns. The receiver output will have a BER of 10^{-2} or better for a period of 12 µs or until signal detect is deasserted. The input data stream is the Quiet Line State. Also, signal detect will be deasserted within a maximum of 350 µs after the BER of the receiver output degrades above 10^{-2} for an input optical data stream that decays with a negative ramp function instead of a step function. See Figure 15 for more information.

Ordering Information

The AFBR-5803Z/5803TZ/5803AZ/5803ATZ 1300 nm products are available for production orders through the Broadcom Component Field Sales Offices and Authorized Distributors world wide.

Temperature ranges:

0°C to +70°C	AFBR-5803Z/5803TZ
–10°C TO +85°C	AFBR-5803AZ/5803ATZ

NOTE

- The "T" in the product numbers indicates a transceiver with a duplex ST connector receptacle.
- Product numbers without a "T" indicate transceivers with a duplex SC connector receptacle.

For product information and a complete list of distributors, please go to our web site: www.broadcom.com.

AV02-0606EN – March 24, 2017

BROADCOM®

Lead (Pb) Free
RoHS 6 fully
compliant

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Broadcom Limited:

AFBR-5803TZ AFBR-5803Z