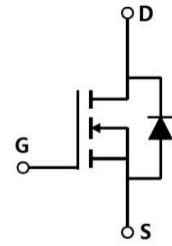


80V N-SGT Enhancement Mode MOSFET

General Description

IRF1405PBF-ML use advanced SGTMOSTM technology to provide low RDS(ON), low gate charge, fast switching. This device is specially designed to get better ruggedness and suitable to use in

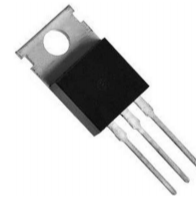


Features

- Low RDS(on) & FOM
- Extremely low switching loss
- Excellent stability and uniformity of Invertors

Applications

- Consumer electronic power supply Motor control
- Synchronous-rectification Isolated DC
- Synchronous-rectification applications



Absolute Maximum Ratings at T_j=25°C unless otherwise noted

| Parameter | Symbol | Value | Unit |
|--|----------------------|------------|------|
| Drain source voltage | VDS | 80 | V |
| Gate source voltage | VGS | ±20 | V |
| Continuous drain current ¹⁾ | ID | 130 | A |
| Pulsed drain current ²⁾ | ID, pulse | 390 | A |
| Power dissipation ³⁾ | P _d | 192 | W |
| Single pulsed avalanche energy ⁵⁾ | EAS | 400 | mJ |
| Operation and storage temperature | Tstg, T _j | -55 to 150 | °C |
| Thermal resistance, junction-case | RθJC | 0.65 | °C/W |
| Thermal resistance, junction-ambient ⁴⁾ | RθJA | 62.5 | °C/W |

80V N-SGT Enhancement Mode MOSFET

Electrical Characteristics at $T_j=25\text{ }^\circ\text{C}$ unless otherwise specified

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test condition |
|----------------------------------|---------------|------|-------|------|---------------|---|
| Drain-source breakdown voltage | BV_{DSS} | 80 | | | V | $V_{GS}=0\text{ V}$, $I_D=250\text{ }\mu\text{A}$ |
| Gate threshold voltage | $V_{GS(th)}$ | 2.0 | | 4.0 | V | $V_{DS}=V_{GS}$, $I_D=250\text{ }\mu\text{A}$ |
| Drain-source on-state resistance | $R_{DS(on)}$ | | 3.8 | 4.5 | m Ω | $V_{GS}=10\text{ V}$, $I_D=20\text{ A}$ |
| Gate-source leakage current | I_{GSS} | | | 100 | nA | $V_{GS}=20\text{ V}$ |
| | | | | -100 | | $V_{GS}=-20\text{ V}$ |
| Drain-source leakage current | I_{DSS} | | | 1 | μA | $V_{DS}=80\text{ V}$, $V_{GS}=0\text{ V}$ |
| Input capacitance | C_{iss} | | 8681 | | pF | $V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$ |
| Output capacitance | C_{oss} | | 6484 | | pF | |
| Reverse transfer capacitance | C_{rss} | | 8.55 | | pF | |
| Turn-on delay time | $t_{d(on)}$ | | 28.2 | | ns | $V_{GS}=10\text{ V}$, $V_{DS}=50\text{ V}$, $R_G=2.2\text{ }\Omega$, $I_D=22\text{ A}$ |
| Rise time | t_r | | 7.5 | | ns | |
| Turn-off delay time | $t_{d(off)}$ | | 81.9 | | ns | |
| Fall time | t_f | | 20.1 | | ns | |
| Total gate charge | Q_g | | 101.6 | | nC | $I_D=22\text{ A}$, $V_{DS}=50\text{ V}$, $V_{GS}=10\text{ V}$ |
| Gate-source charge | Q_{gs} | | 20.6 | | nC | |
| Gate-drain charge | Q_{gd} | | 28.7 | | nC | |
| Gate plateau voltage | $V_{plateau}$ | | 4.2 | | V | |
| Diode forward current | I_S | | | 130 | A | $V_{GS}<V_{th}$ |
| Pulsed source current | I_{SP} | | | 390 | | |
| Diode forward voltage | V_{SD} | | | 1.3 | V | $I_S=20\text{ A}$, $V_{GS}=0\text{ V}$ |
| Reverse recovery time | t_{rr} | | 82.1 | | ns | $I_S=10\text{ A}$, $di/dt=100\text{ A}/\mu\text{s}$ |
| Reverse recovery charge | Q_{rr} | | 248.4 | | nC | |
| Peak reverse recovery current | I_{rrm} | | 4.9 | | A | |

Note

- 1) Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating; pulse width limited by max. junction temperature.
- 3) P_d is based on max. junction temperature, using junction-case thermal resistance.
- 4) The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_a=25\text{ }^\circ\text{C}$.
- 5) $V_{DD}=50\text{ V}$, $R_G=25\text{ }\Omega$, $L=0.5\text{ mH}$, starting $T_j=25\text{ }^\circ\text{C}$.

Electrical Characteristics Diagrams

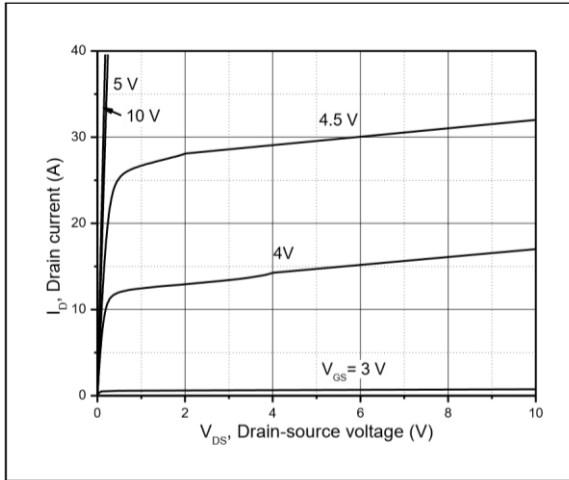


Figure 1, Typ. output characteristics

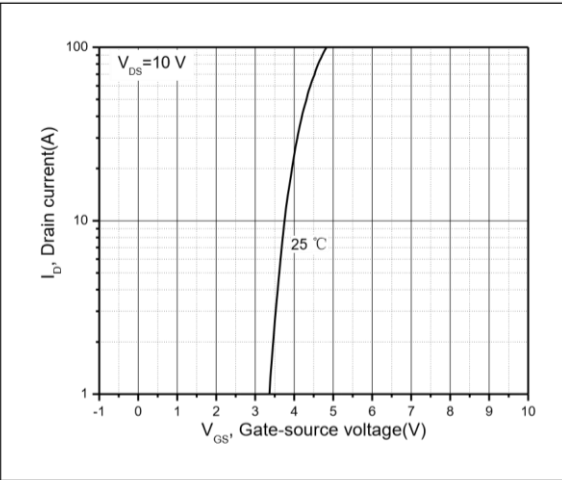


Figure 2, Typ. transfer characteristics

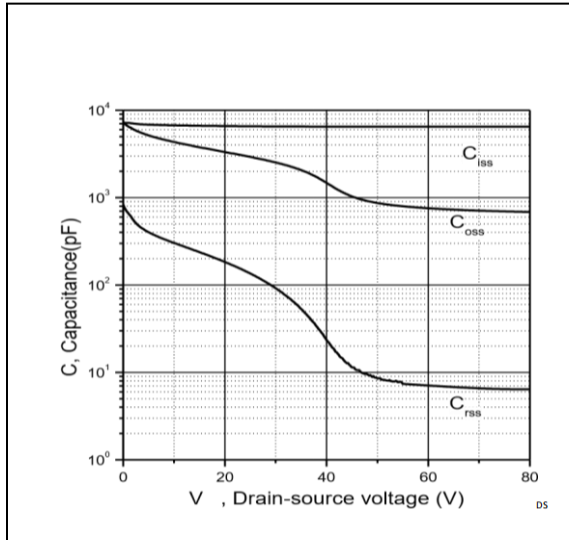


Figure 3, Typ. capacitances

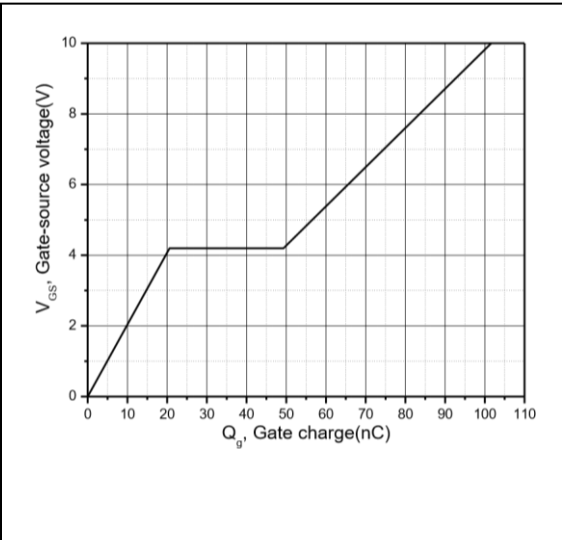


Figure 4, Typ. gate charge

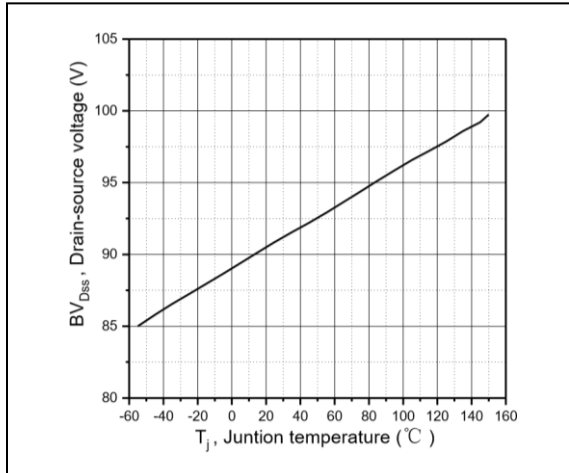


Figure 5, Drain-source breakdown voltage

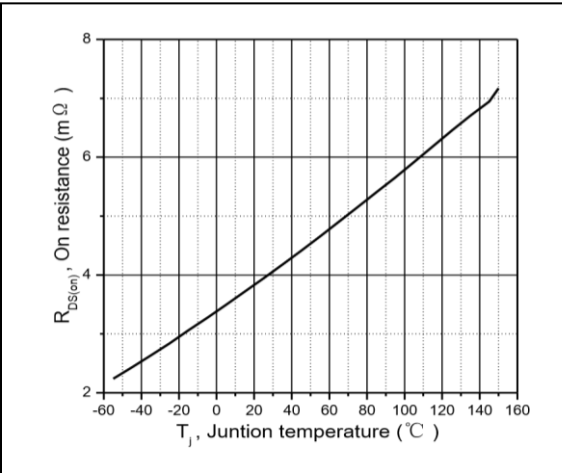


Figure 6, Drain-source on-state resistance

80V N-SGT Enhancement Mode MOSFET

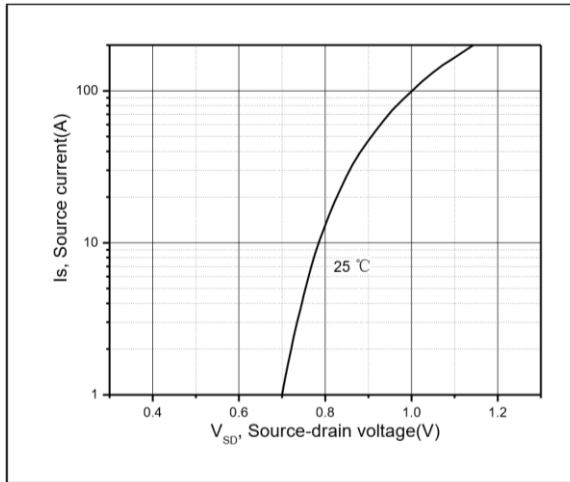


Figure 7, Forward characteristic of body diode

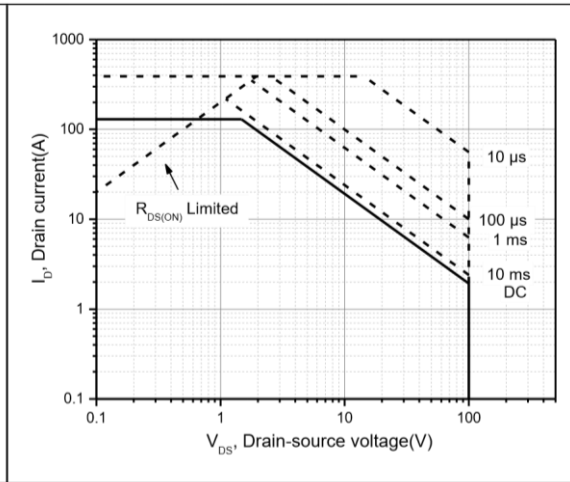


Figure 8, Safe operation area $T_C=25\text{ }^\circ\text{C}$

Test circuits and waveforms

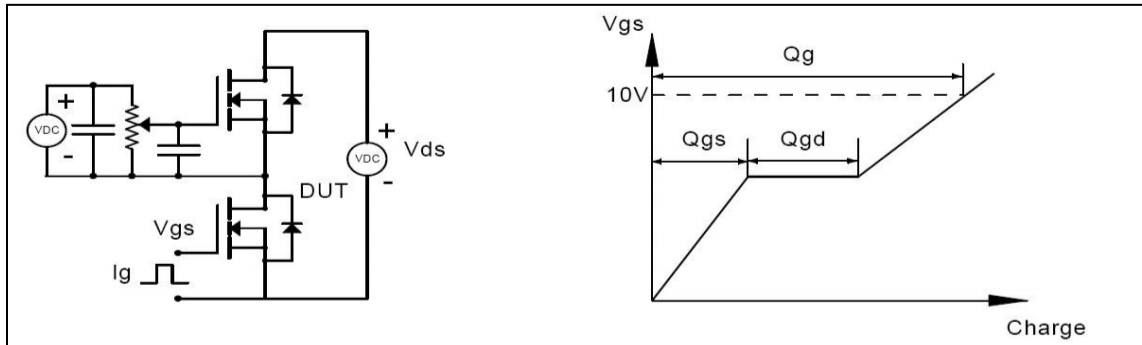


Figure 1, Gate charge test circuit & waveform

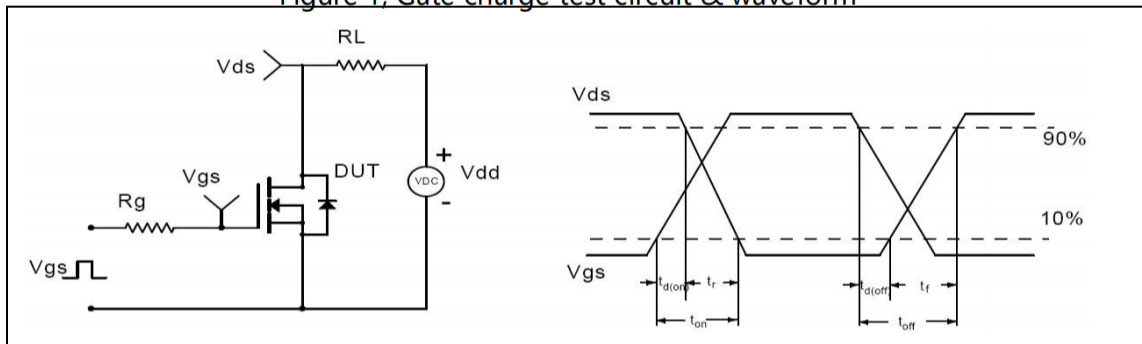


Figure 2, Switching time test circuit & waveforms

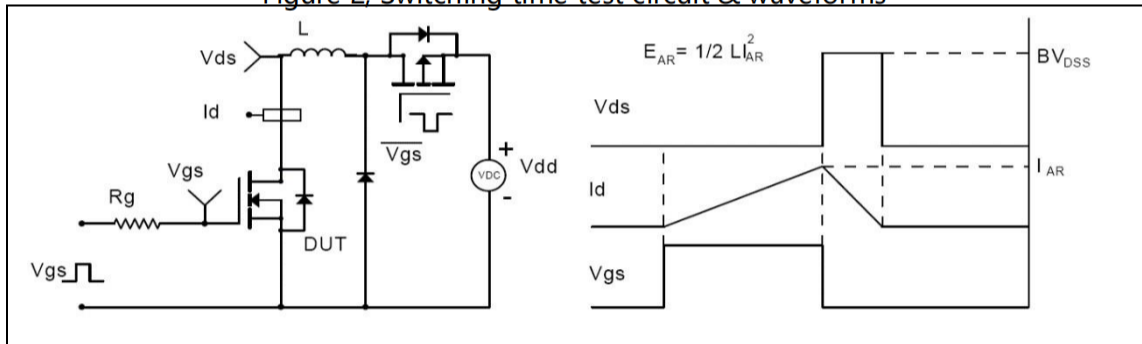


Figure 3, Unclamped inductive switching (UIS) test circuit & waveforms

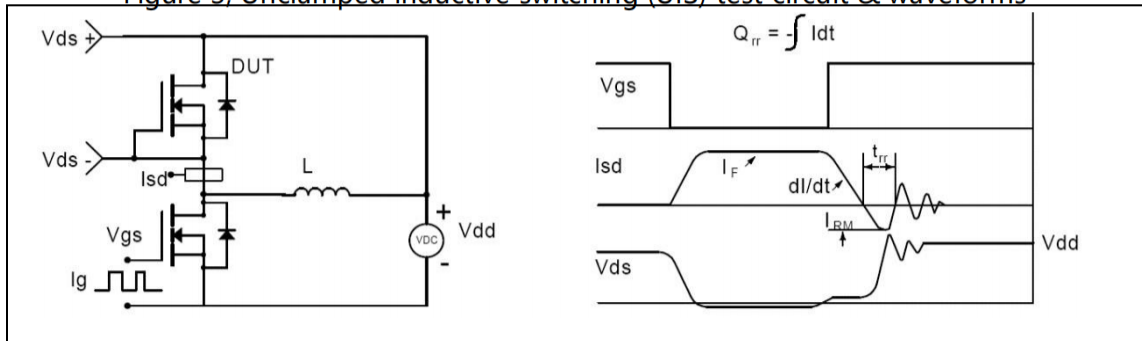
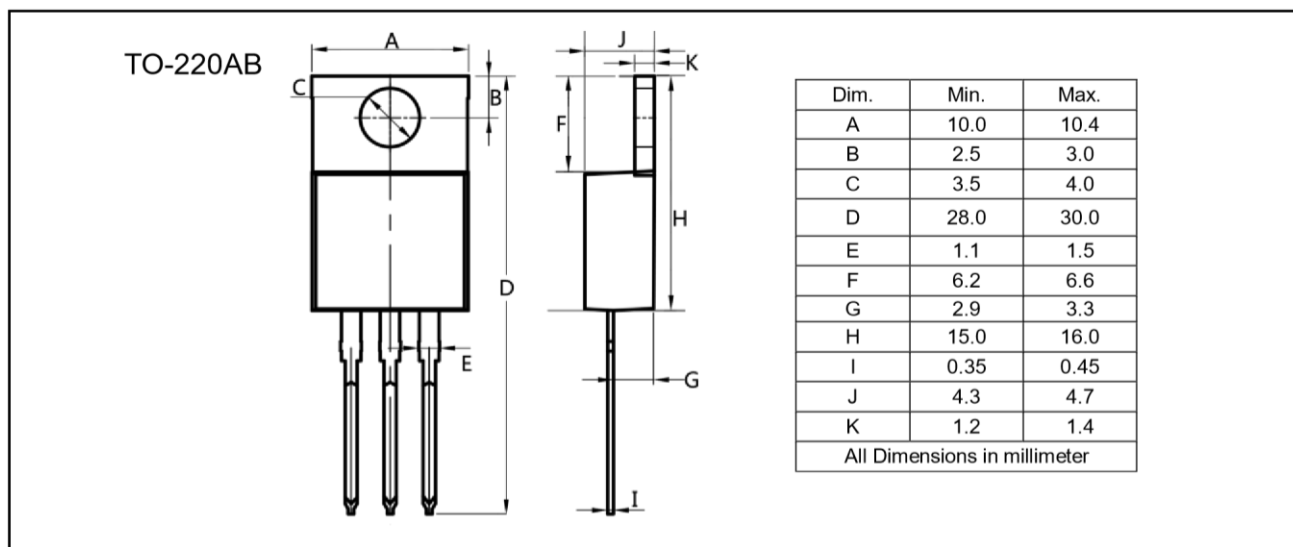


Figure 4, Diode reverse recovery test circuit & waveforms

80V N-SGT Enhancement Mode MOSFET



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