

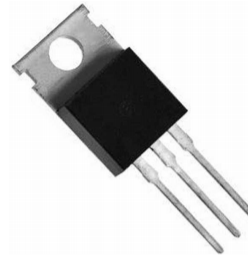
## N-Channel Trench Power MOSFET

### General Description

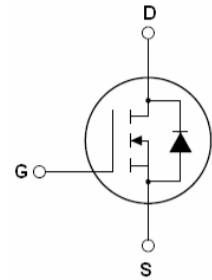
The IRF520PBF-ML combines advanced trench MOSFET technology with a low resistance package to provide extremely low  $R_{DS(ON)}$ . This device is ideal for power switching application and LED backlighting.

### Features

- $V_{DS}=100V$ ;  $I_D=10A$   
 $R_{DS(ON)}<200m\Omega @ V_{GS}=10V$
- Ultra Low On-Resistance
- High UIS and UIS 100% Test



To-220 Top View



Schematic Diagram

### Application

- Power switching application
- LED backlighting

Table 1. Absolute Maximum Ratings (TA=25°C)

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-Source Voltage ( $V_{GS}=0V$ )	100	V
$V_{GS}$	Gate-Source Voltage ( $V_{DS}=0V$ )	$\pm 20$	V
$I_{D(DC)}$	Drain Current (DC) at $T_c=25^\circ C$	10	A
$I_{D(DC)}$	Drain Current (DC) at $T_c=100^\circ C$	7.7	A
$I_{DM (pulse)}$	Drain Current-Continuous@ Current-Pulsed (Note 1)	44	A
$P_D$	Maximum Power Dissipation( $T_c=25^\circ C$ )	45	W
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)	16	mJ
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 To 175	$^\circ C$

Notes 1. Repetitive Rating: Pulse width limited by maximum junction temperature

2. EAS condition:  $T_J=25^\circ C, V_{DD}=50V, V_G=10V, R_G=25\Omega$

**Table 2. Thermal Characteristic**

Symbol	Parameter	Value	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	---	3.3	$^{\circ}C/W$

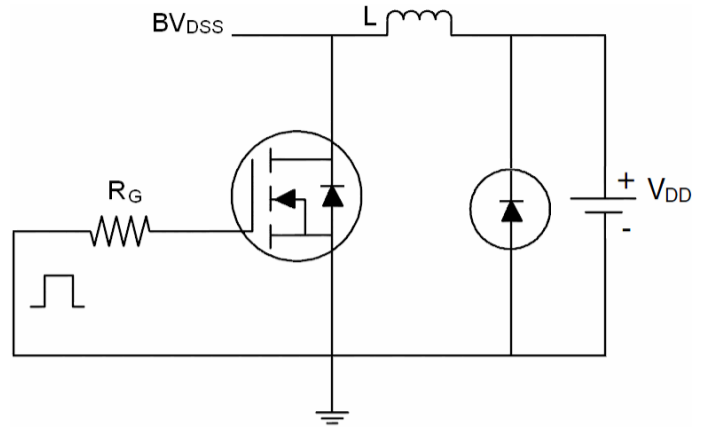
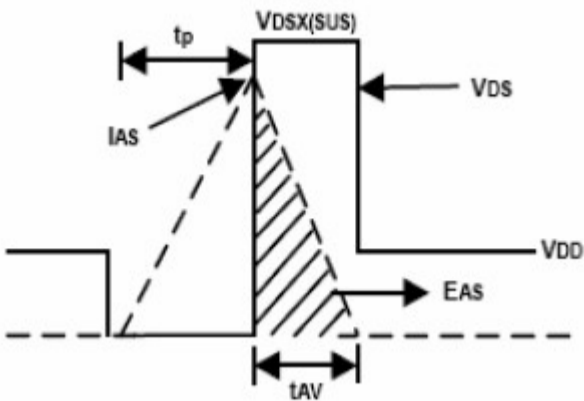
**Table 3. Electrical Characteristics (TA=25 $^{\circ}C$  unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>On/Off States</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	100			V
$I_{DSS}$	Zero Gate Voltage Drain Current(Tc=25 $^{\circ}C$ )	$V_{DS}=100V, V_{GS}=0V$			1	$\mu A$
$I_{DSS}$	Zero Gate Voltage Drain Current(Tc=100 $^{\circ}C$ )	$V_{DS}=100V, V_{GS}=0V$			5	$\mu A$
$I_{GSS}$	Gate-Body Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$			$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2		4	V
$R_{DS(on)}$	Drain-Source On-State Resistance	$V_{GS}=10V, I_D=7.5 A$			200	m $\Omega$
<b>Dynamic Characteristics</b>						
$g_{FS}$	Forward Transconductance	$V_{DS}=5V, I_D=4.5A$	5			S
$C_{iss}$	Input Capacitance	$V_{DS}=50V, V_{GS}=0V$ $f=1.0MHz$		690		PF
$C_{oss}$	Output Capacitance			44		PF
$C_{rss}$	Reverse Transfer Capacitance			30		PF
$Q_g$	Total Gate Charge	$V_{DS}=50V, I_D=4.5A$ $V_{GS}=10V$		13.4		nC
$Q_{gs}$	Gate-Source Charge			3.2		nC
$Q_{gd}$	Gate-Drain Charge			6.2		nC
<b>Switching Times</b>						
$t_{d(on)}$	Turn-on Delay Time	$V_{DS}=50V, R_L=8.6\Omega$ $V_{GS}=10V, R_G=3\Omega$		7		nS
$t_r$	Turn-on Rise Time			12		nS
$t_{d(off)}$	Turn-Off Delay Time			24		nS
$t_f$	Turn-Off Fall Time			11		nS
<b>Source-Drain Diode Characteristics</b>						
$I_{SD}$	Source-Drain Current(Body Diode)			15		A
$I_{SDM}$	Pulsed Source-Drain Current(Body Diode)			44		A
$V_{SD}$	Forward On Voltage <sup>(Note 1)</sup>	$T_J=25^{\circ}C, I_{SD}=1A, V_{GS}=0V$		0.75	1	V
$t_{rr}$	Reverse Recovery Time <sup>(Note 1)</sup>	$T_J=25^{\circ}C, I_F=4.5A$ $di/dt=500A/\mu s$		11		nS
$Q_{rr}$	Reverse Recovery Charge <sup>(Note 1)</sup>				14	
$t_{on}$	Forward Turn-on Time	Intrinsic turn-on time is negligible(turn-on is dominated by $L_S+L_D$ )				

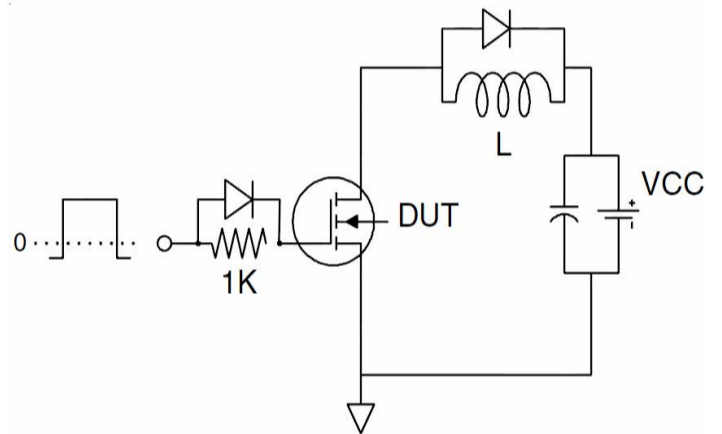
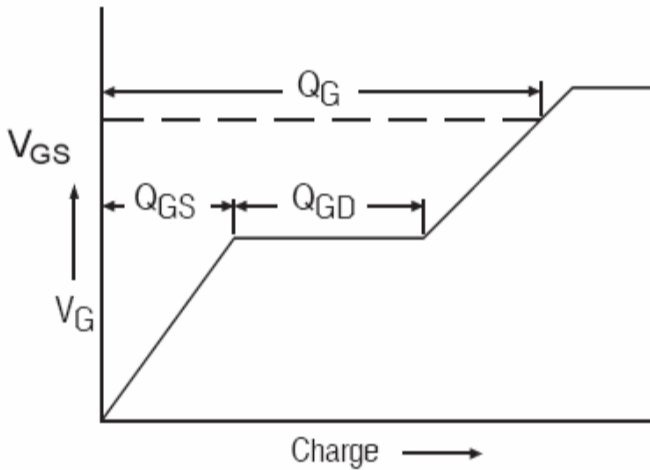
Notes 1. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 1.5\%$ , Starting  $T_J=25^{\circ}C$

## Test Circuit

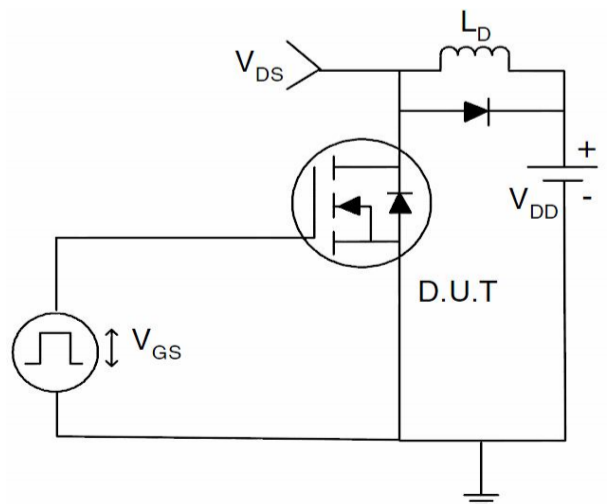
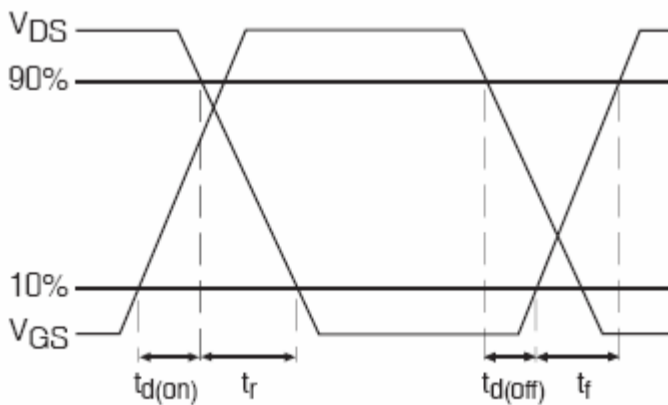
### 1) E<sub>AS</sub> Test Circuits



### 2) Gate Charge Test Circuit:



### 3) Switch Time Test Circuit:



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

Figure1. On-Region Characteristics

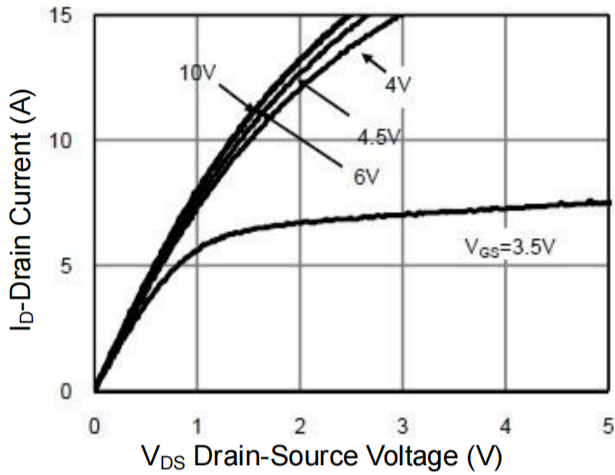


Figure 2: Transfer Characteristics

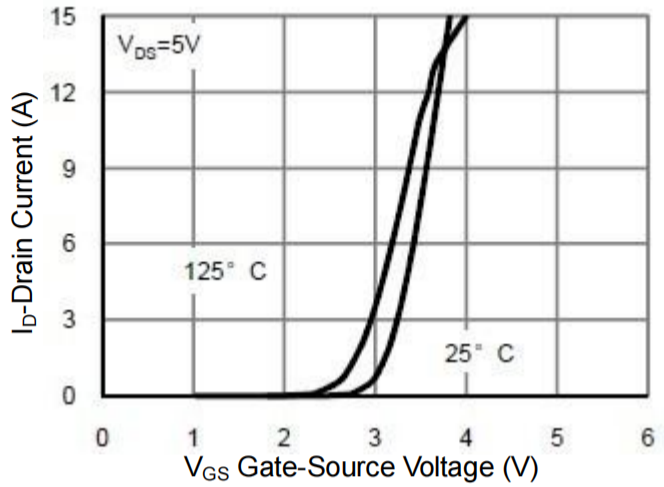


Figure3. ID vs Junction Temperature

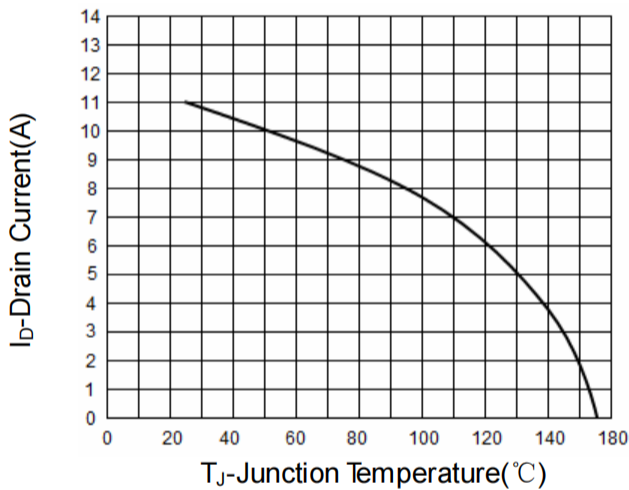


Figure4. On-Resistance vs. Junction Temperature

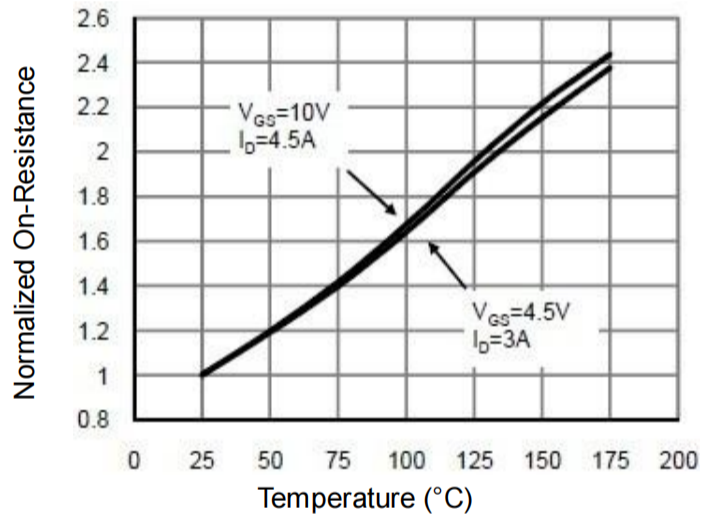


Figure5. On-Resistance vs. Gate-Source Voltage

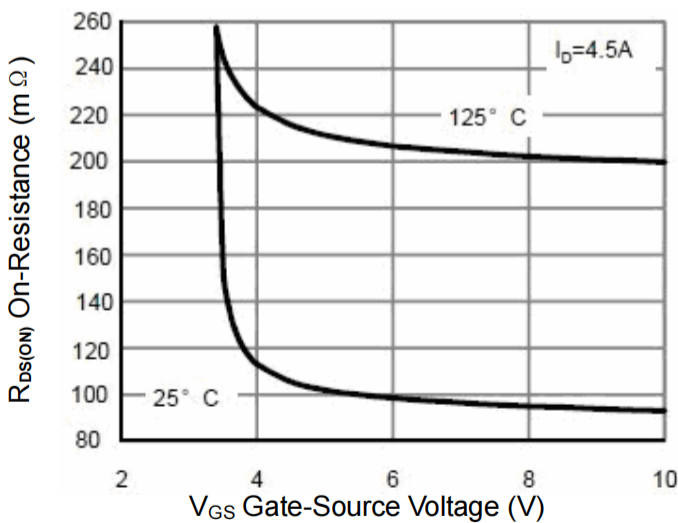


Figure6. Body-Diode Characteristics

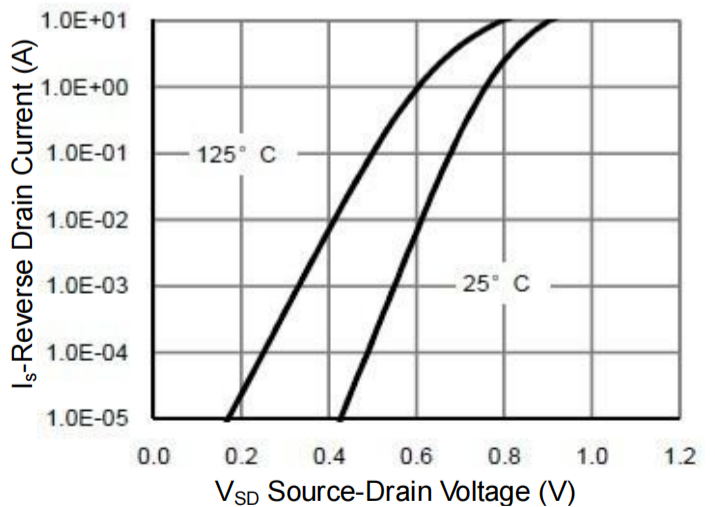


Figure7. Gate-Charge Characteristics

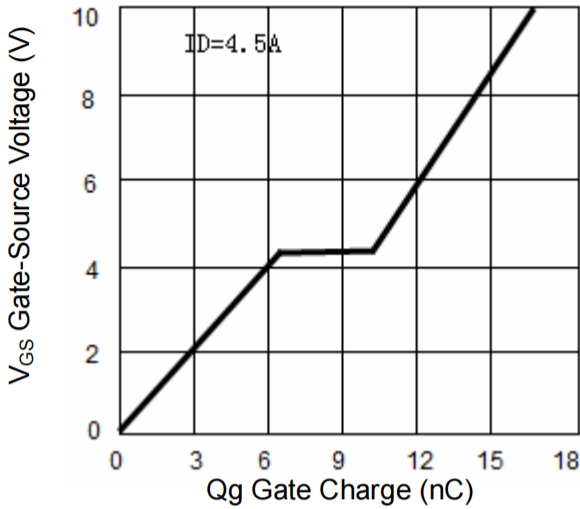


Figure 8. Capacitance Characteristics

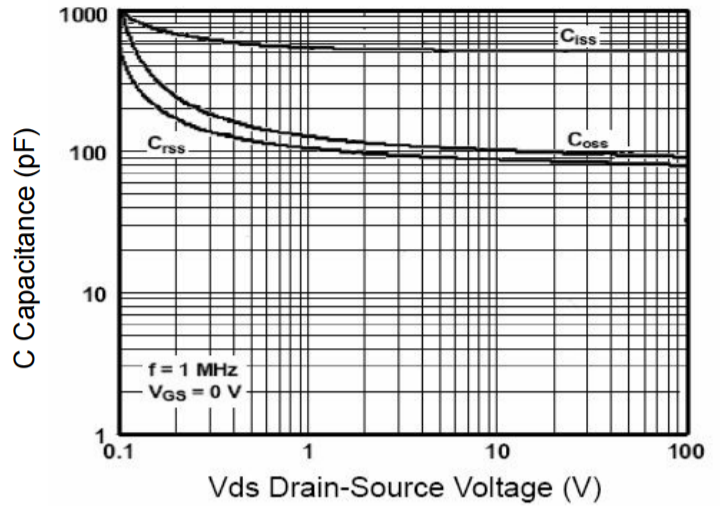


Figure 9. Maximum Forward Biased Safe Operating Area

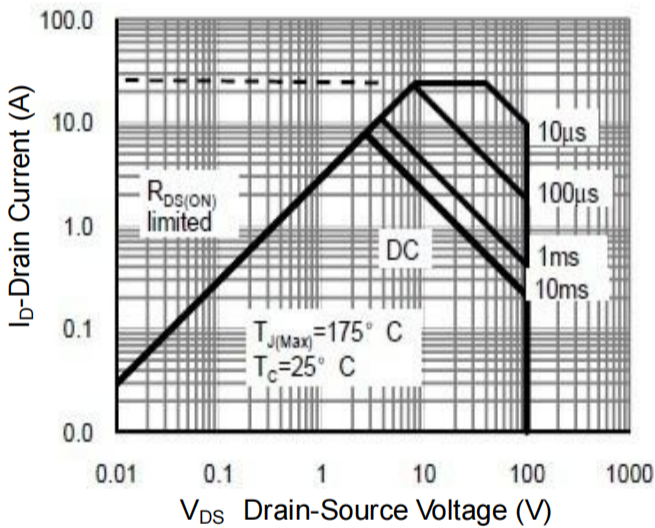


Figure10. Single Pulse Power Rating Junction-to-Case

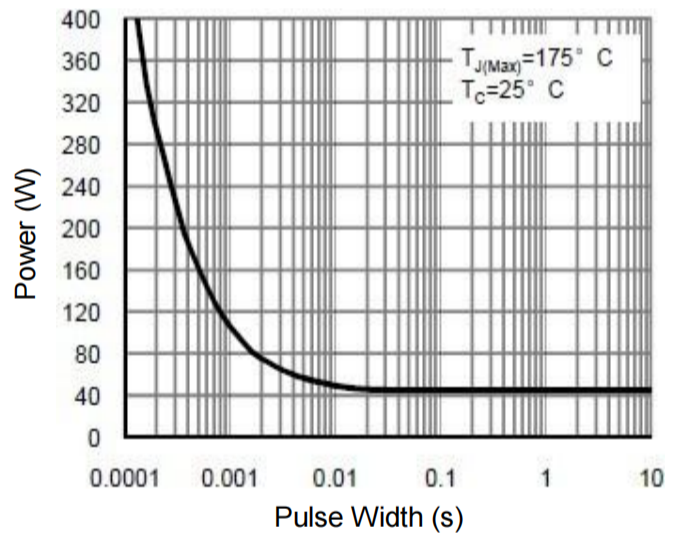
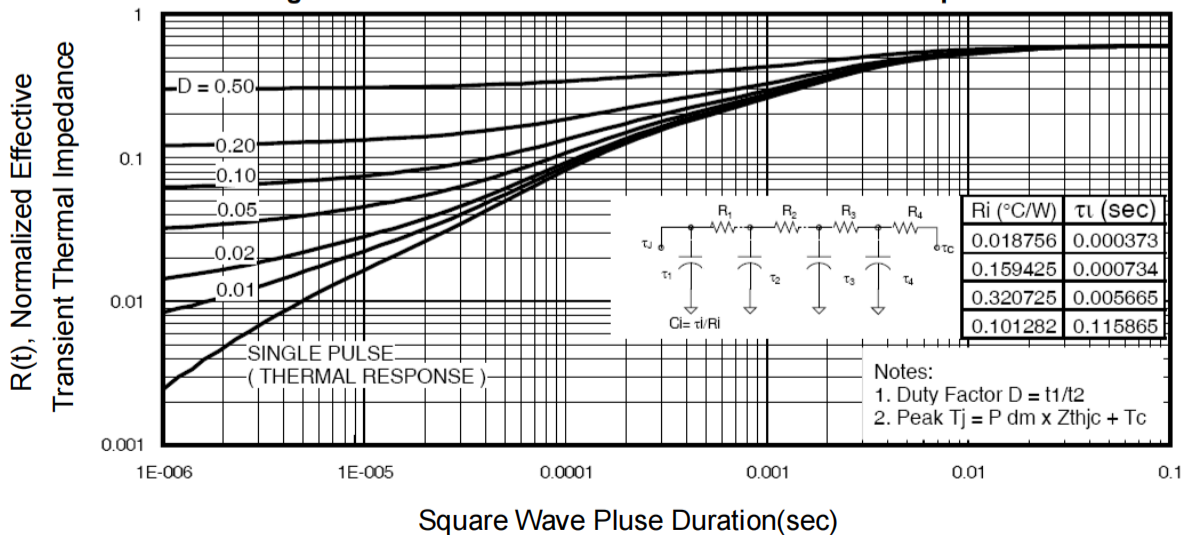
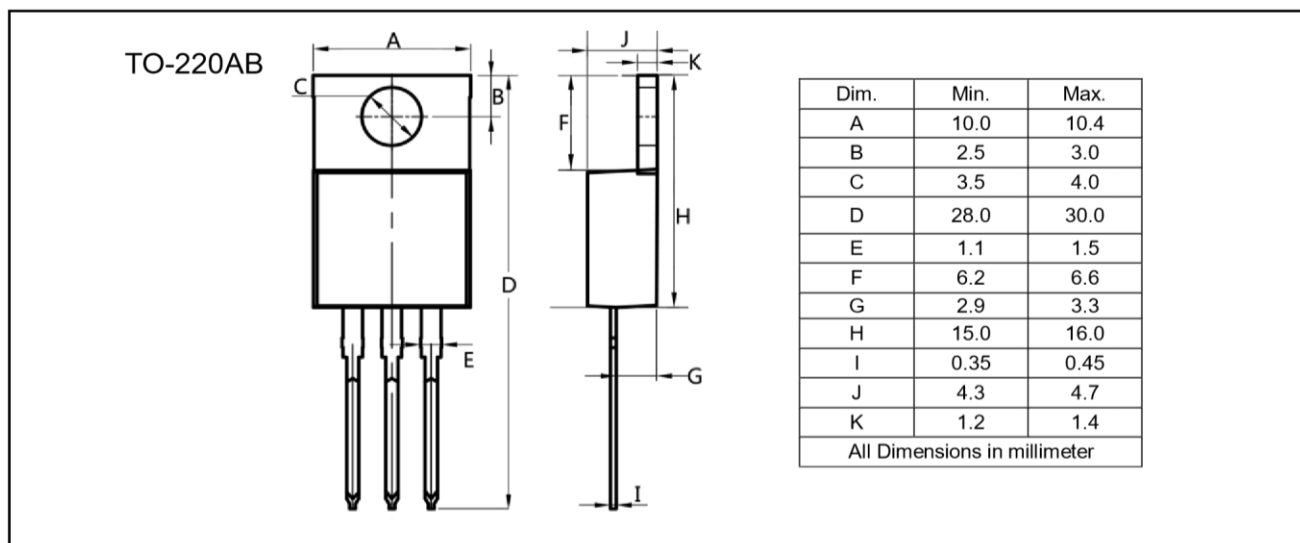


Figure11. Normalized Maximum Transient Thermal Impedance





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