

**Description**

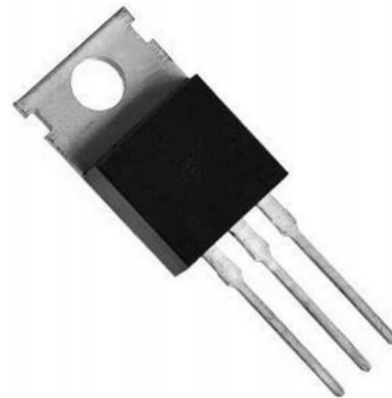
The IRF640NPBF-ML uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

**General Features**

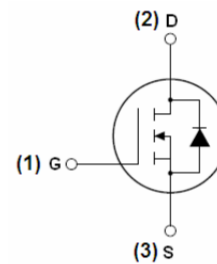
- $V_{DS} = 200V, I_D = 18A$   
 $R_{DS(ON)} < 180m\Omega @ V_{GS} = 10V$  (Typ: 140m $\Omega$ )
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

**Application**

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



TO-220C



Schematic Diagram

**Absolute Maximum Ratings ( $T_C = 25^\circ C$  unless otherwise noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	200	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	18	A
Drain Current-Continuous( $T_C = 100^\circ C$ )	$I_D(100^\circ C)$	13	A
Pulsed Drain Current	$I_{DM}$	72	A
Maximum Power Dissipation	$P_D$	150	W
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	250	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^\circ C$

**Thermal Characteristic**

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	1	°C/W
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**Electrical Characteristics ( $T_C=25^\circ\text{C}$  unless otherwise noted)**

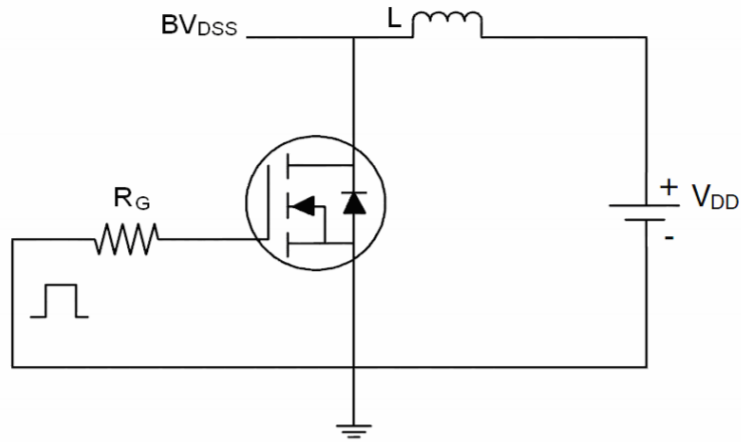
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	200	220	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=200V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> <sup>(Note 3)</sup>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=15A$	-	140	180	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=50V, I_D=11A$	25	-	-	S
<b>Dynamic Characteristics</b> <sup>(Note 4)</sup>						
Input Capacitance	$C_{iss}$	$V_{DS}=25V, V_{GS}=0V,$ $F=1.0\text{MHz}$		4200		PF
Output Capacitance	$C_{oss}$			163		PF
Reverse Transfer Capacitance	$C_{rss}$			75		PF
<b>Switching Characteristics</b> <sup>(Note 4)</sup>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=100V, I_D=15A$ $V_{GS}=10V, R_{GEN}=2.5\Omega$	-	10	-	nS
Turn-on Rise Time	$t_r$		-	18	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	22	-	nS
Turn-Off Fall Time	$t_f$		-	5	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=100V, I_D=15A,$ $V_{GS}=10V$		60		nC
Gate-Source Charge	$Q_{gs}$			19		nC
Gate-Drain Charge	$Q_{gd}$			17		nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage <sup>(Note 3)</sup>	$V_{SD}$	$V_{GS}=0V, I_S=11A$	-	-	1.2	V
Diode Forward Current <sup>(Note 2)</sup>	$I_S$	-	-	-	18	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ\text{C}, I_F = 15A$ $di/dt = 100A/\mu\text{s}$ <sup>(Note 3)</sup>	-	90	-	nS
Reverse Recovery Charge	$Q_{rr}$		-	300	-	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

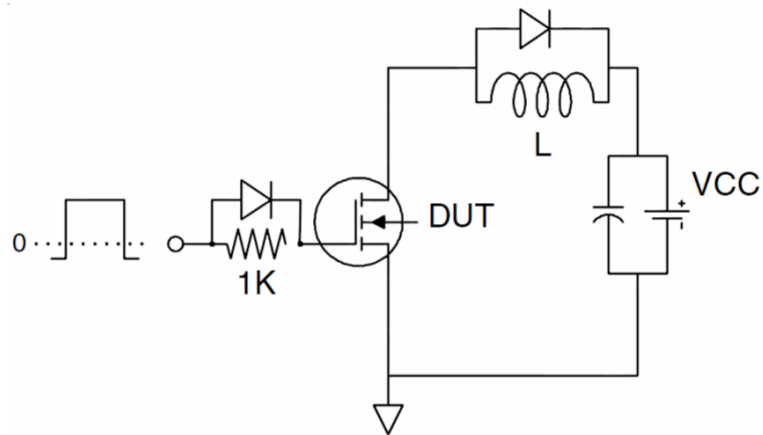
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition:  $T_J=25^\circ\text{C}, V_{DD}=50V, V_G=10V, L=0.5\text{mH}, R_g=25\Omega$

Test Circuit

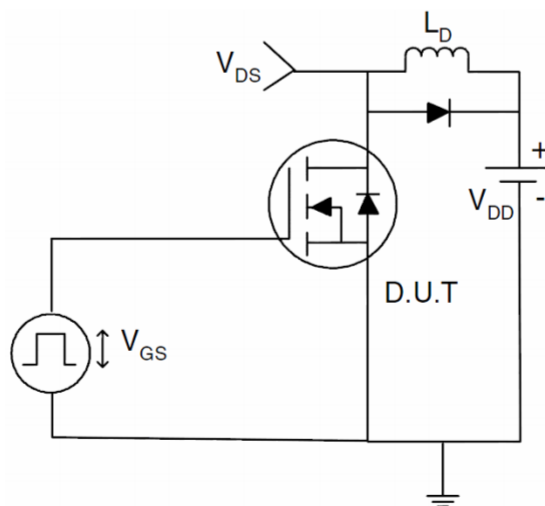
1) E<sub>AS</sub> test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

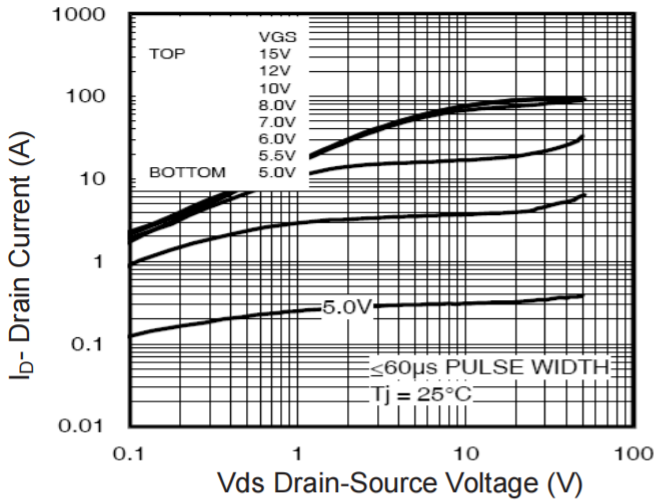


Figure 1 Output Characteristics

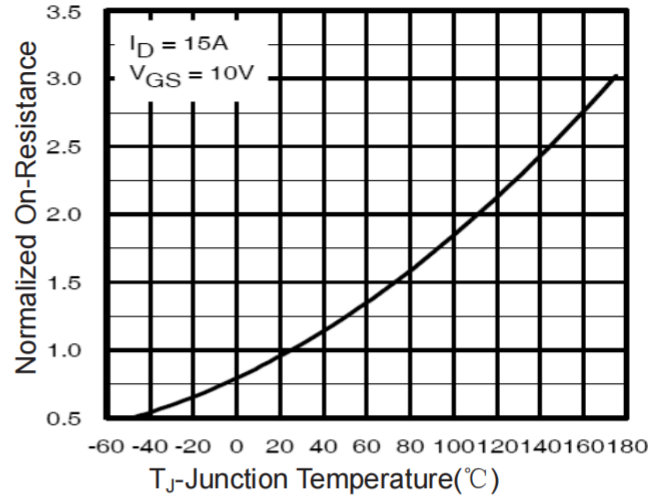


Figure 4 Rdson-Junction Temperature

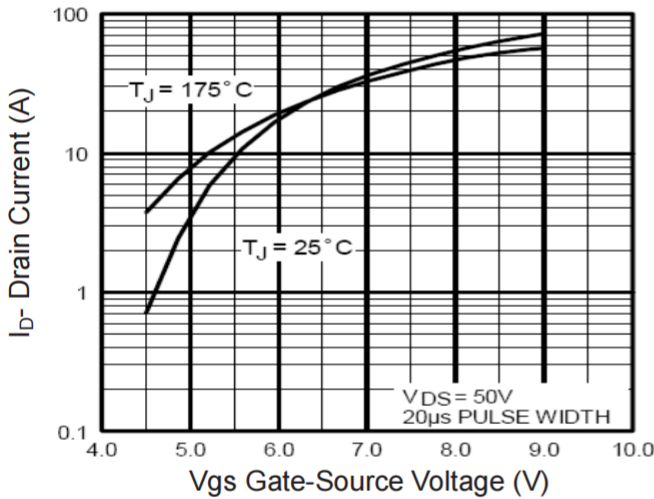


Figure 2 Transfer Characteristics

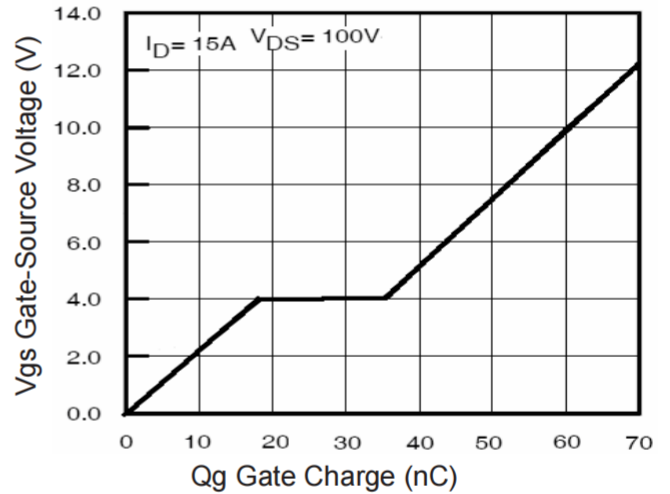


Figure 5 Gate Charge

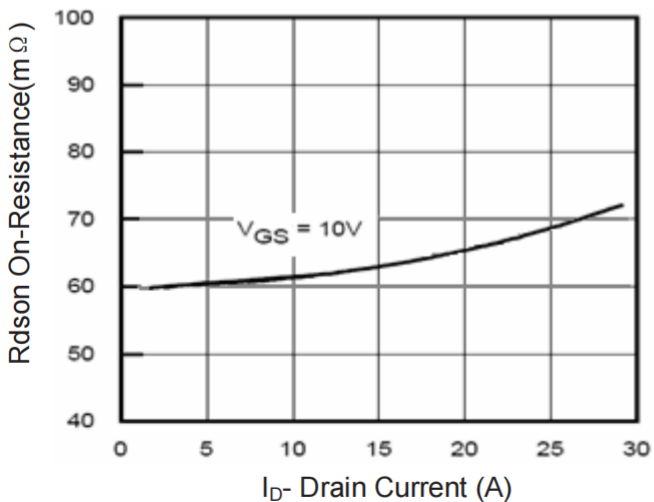


Figure 3 Rdson- Drain Current

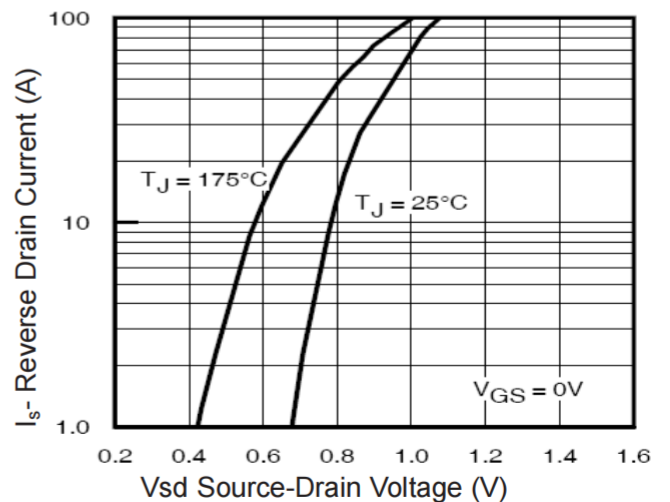


Figure 6 Source- Drain Diode Forward

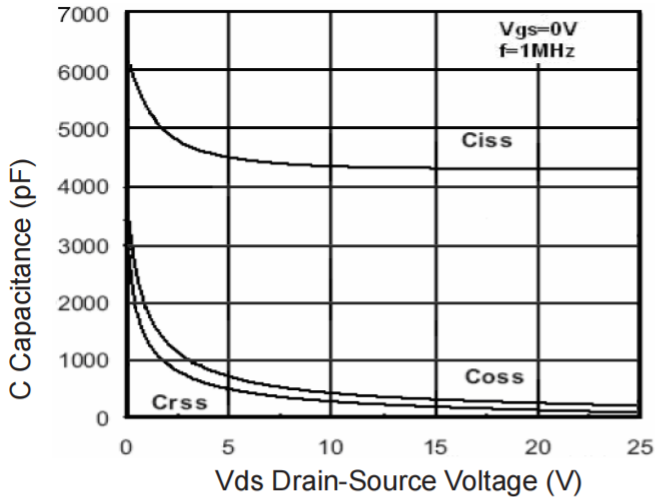


Figure 7 Capacitance vs Vds

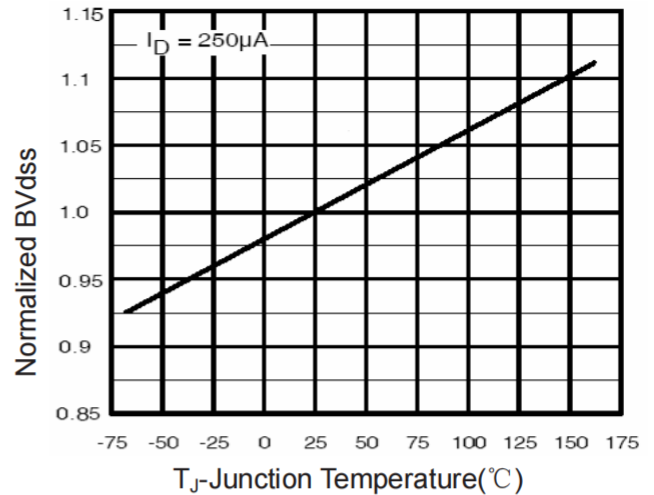


Figure 9  $BV_{DSS}$  vs Junction Temperature

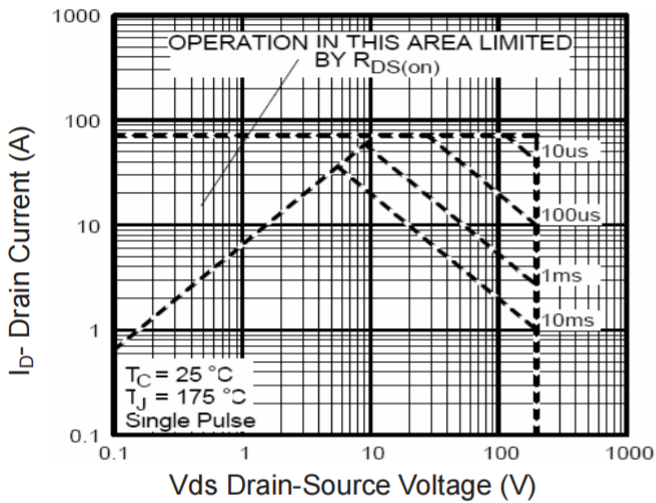


Figure 8 Safe Operation Area

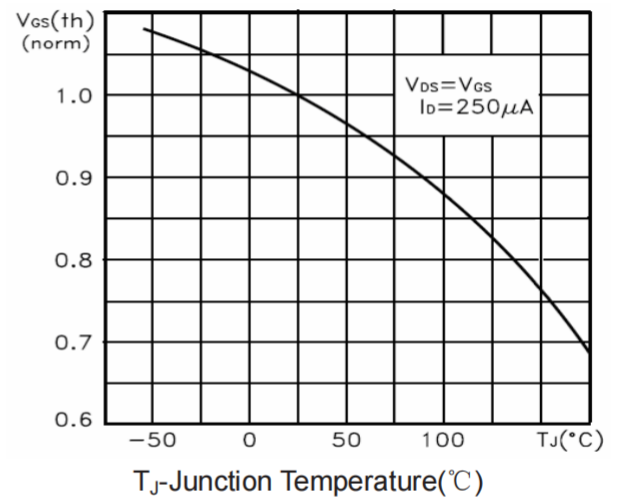


Figure 10  $V_{GS(th)}$  vs Junction Temperature

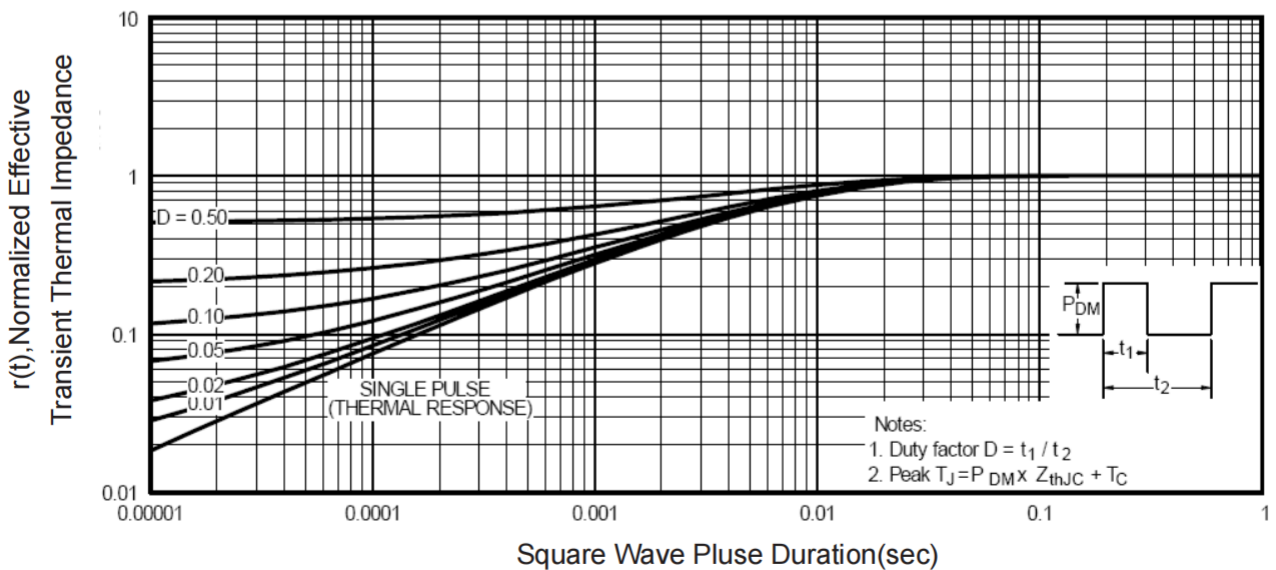


Figure 11 Normalized Maximum Transient Thermal Impedance

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