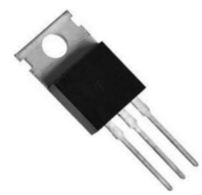
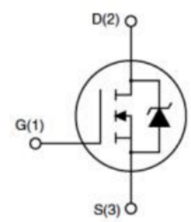
V_{DSS}	400	V
I_D	10	A
P_D (T_C=25℃)	40	W
$R_{DS(ON)}$ Typ	0.38	Ω





General Description:

IRF740PBF-ML, the silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher eficiency. The package form is TO-220F, which accords with the RoHS standard.

Features:

- ►**Fast Switching**
- ► **Low ON Resistance**(Rdson≤0. 38Ω)
- ► **Low Gate Charge** (Typical Data:32nC)
- ► **Low Reverse transfer capacitances**(Typical:8.4pF)
- ► **100% Single Pulse avalanche energy Test**

Applications:

Power switch circuit of adaptor and charger.

Absolute (Tc= 25℃ unless otherwise specified):

Symbol	Parameter	Rating	Units
V_{DSS}	Drain- to- Source Voltage	400	V
I_D	Continuous Drain Current	10	A
	Continuous Drain Current T_C = 100 °C	6.3	A
I_{DM} a1	Pulsed Drain Current	40	A
V_{GS}	Gate- to- Source Voltage	±30	V
E_{AS} a2	Single Pulse Avalanche Energy	580	mJ
dv/dt a3	Peak Diode Recovery dv/ dt	5.0	V/ns
P_D	Power Dissipation	40	W
	Derating Factor above 25°C	0.32	W/ ℃
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, －55 to 150	℃
T_L	Maximum Temperature for Soldering	300	℃

Electrical Characteristics（Tc= 25℃ unless otherwise specified）:

OFF Characteristics

Symbol	Parameter	Test Conditions	Rating Min.	Rating Typ.	Rating Max.	Units
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	500	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Bvdss Temperature Coefficient	ID=250uA, Reference25℃	--	0.6	--	V/℃
I_{DSS}	Drain to Source Leakage Current	V_{DS} =400V, V_{GS}= 0V, T_a = 25℃	--	--	1	μA
		V_{DS} =400V, V_{GS}= 0V, T_a = 125℃	--	--	100	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS} =+30V	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS} =-30V	--	--	-100	nA

ON Characteristics

Symbol	Parameter	Test Conditions	Rating Min.	Rating Typ.	Rating Max.	Units
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}= 10V, I_D=5A	--	0.38	0.42	Ω
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	2.0	--	4.0	V

Pulse width tp≤300μs, δ≤2%

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Rating Min.	Rating Typ.	Rating Max.	Units
g_{fs}	Forward Transconductance	V_{DS}= 15V, I_D =5A	--	10	--	S
C_{iss}	Input Capacitance	V_{GS} = 0V V_{DS} = 25V f = 1.0MHz	--	1620	--	pF
C_{oss}	Output Capacitance		--	154	--	
C_{rss}	Reverse Transfer Capacitance		--	8.4	--	

Resistive Switching Characteristics

Symbol	Parameter	Test Conditions	Rating Min.	Rating Typ.	Rating Max.	Units
$t_{d(ON)}$	Turn-on Delay Time	I_D = 10A V_{DD} = 250V R_G = 10Ω	--	26	--	ns
t_r	Rise Time		--	20	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	52	--	
t_f	Fall Time		--	21	--	
Q_g	Total Gate Charge	I_D = 10A V_{DD} =400V V_{GS} = 10V	--	32	--	nC
Q_{gs}	Gate to Source Charge		--	7.9	--	
Q_{gd}	Gate to Drain ("Miller") Charge		--	12	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)		--	--	10	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	40	A
V_{SD}	Diode Forward Voltage	I_S= 10A, V_{GS}=0V	--	--	1.5	V
trr	Reverse Recovery Time	I_S= 10A, T_j = 25C dI_F/dt=100A/us, V_{GS}=0V	--	411	--	ns
Qrr	Reverse Recovery Charge		--	2588	--	nC
I_{RRM}	Reverse Recovery Current		--	12.6	--	A
Pulse width tp≤300μs, δ ≤2%						

Symbol	Parameter	Typ.	Units
$R_{\theta JC}$	Junction- to- Case	3.13	C/ W
$R_{\theta JA}$	Junction- to- Ambient	62.5	C/ W

a1 ： Repetitive rating; pulse width limited by maximum junction temperature
a2 ： L= 10mH, I_D= 10 . 8A, Start T_J=25C
a3 ： I_{SD} = 10A,di/dt ≤100A/us, V_{DD} ≤ BV_{DS}, Start T_J=25C

Characteristics Curve:

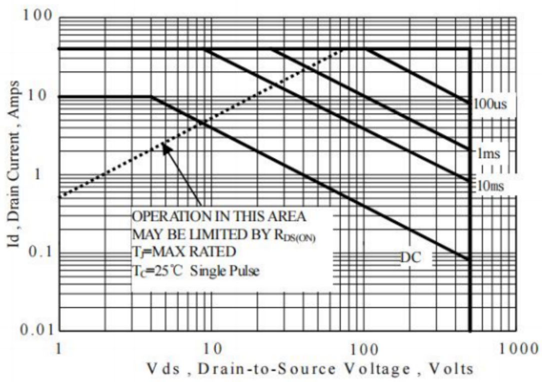


Figure 1 Maximum Forward Bias Safe Operating Area

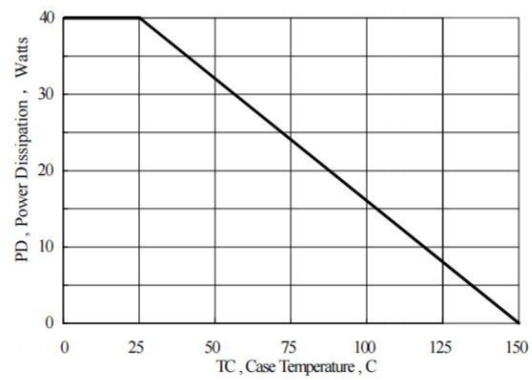


Figure 2 Maximum Power Dissipation vs Case Temperature

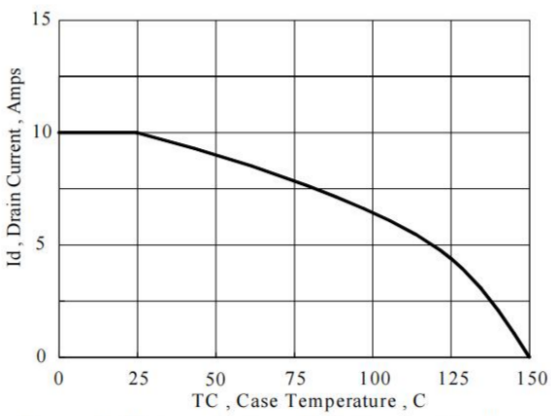


Figure 3 Maximum Continuous Drain Current vs Case Temperature

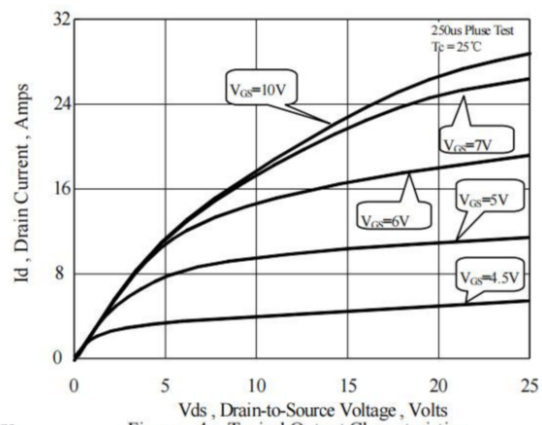


Figure 4 Typical Output Characteristics

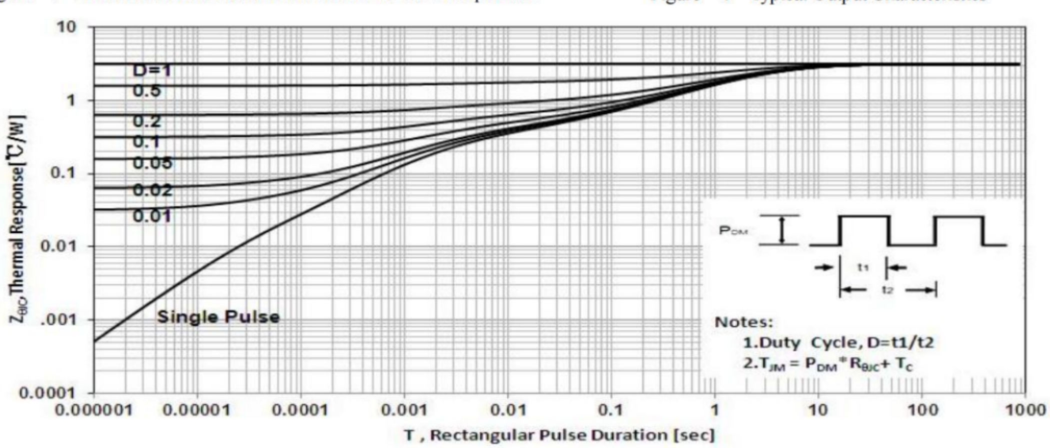


Figure 5 Maximum Effective Thermal Impendance , Junction to Case

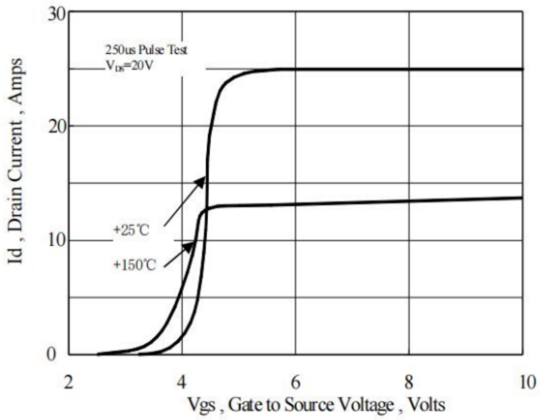


Figure 6 Typical Transfer Characteristics

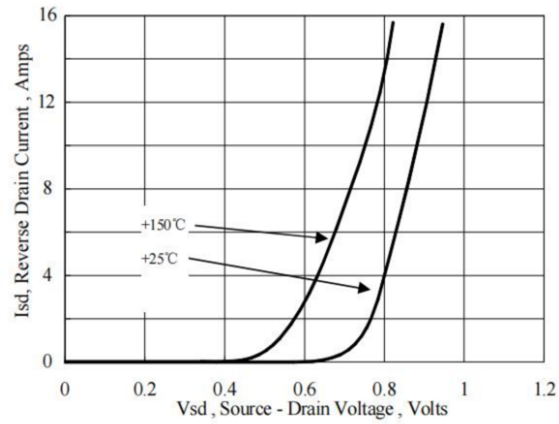


Figure 7 Typical Body Diode Transfer Characteristics

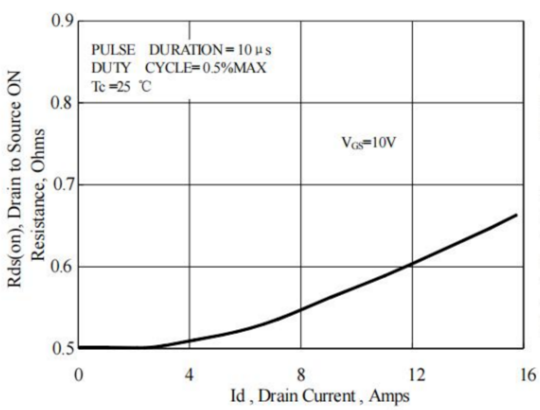


Figure 8 Typical Drain to Source ON Resistance
vs Drain Current

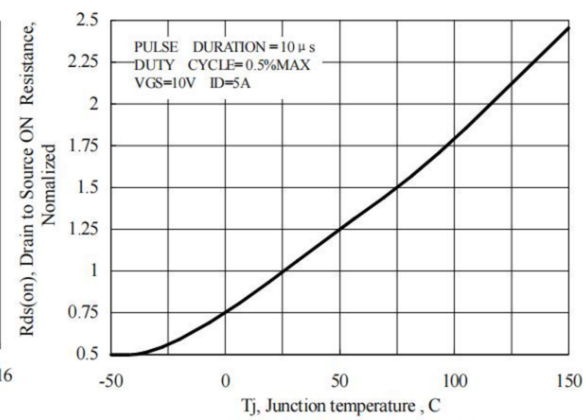


Figure 9 Typical Drian to Source on Resistance
vs Junction Temperature

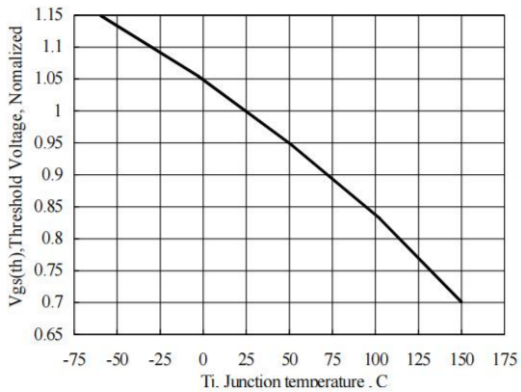


Figure 10 Typical Theshold Voltage vs Junction Temperature

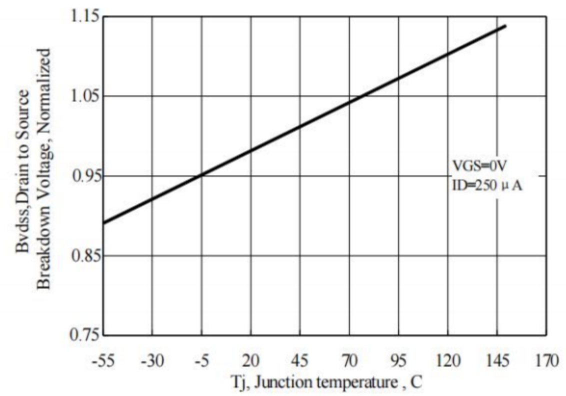


Figure 11 Typical Breakdown Voltage vs Junction Temperature

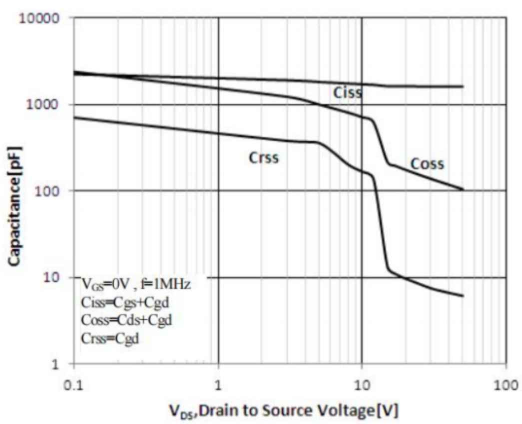


Figure 12 Typical Capacitance vs Drain to Source Voltage

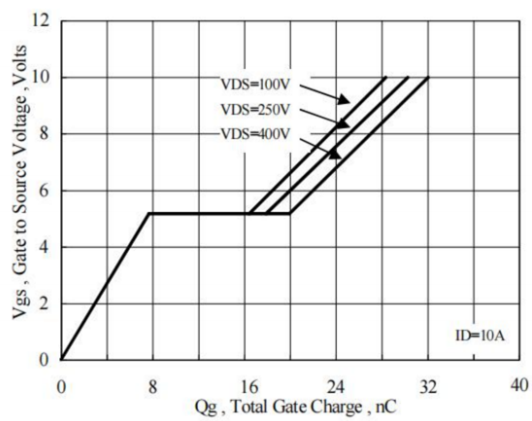


Figure 13 Typical Gate Charge vs Gate to Source Voltage

Test Circuit and Waveform

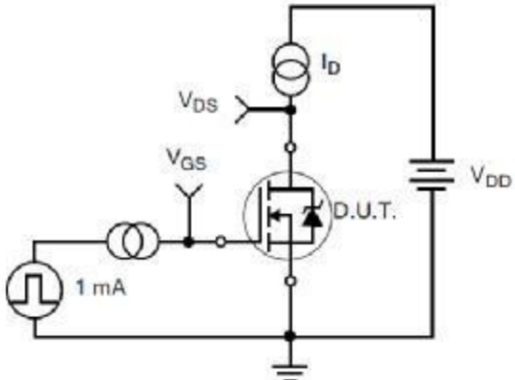


Figure 17. Gate Charge Test Circuit

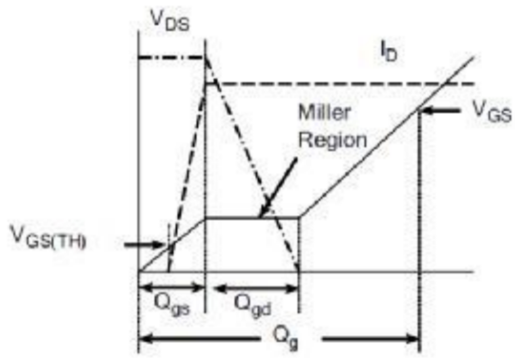


Figure 18. Gate Charge Waveform

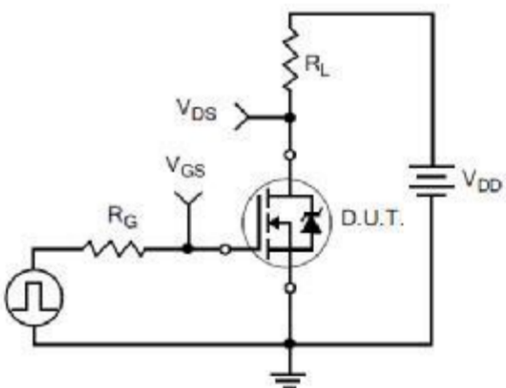


Figure 19. Resistive Switching Test Circuit

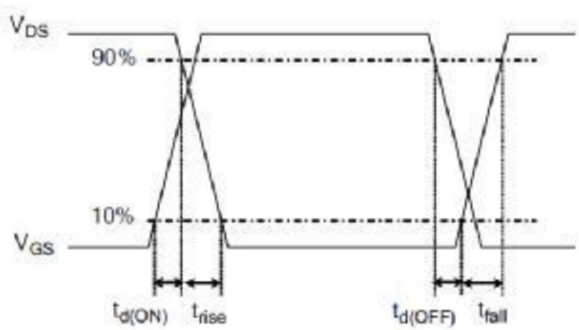


Figure 20. Resistive Switching Waveforms

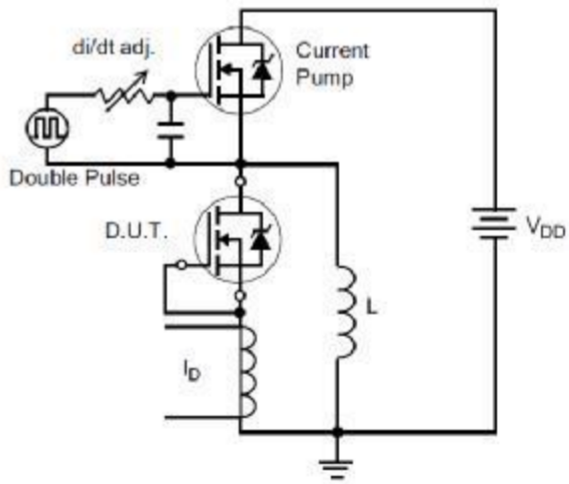


Figure 21. Diode Reverse Recovery Test Circuit

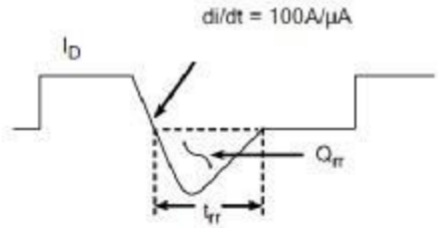


Figure 22. Diode Reverse Recovery Waveform

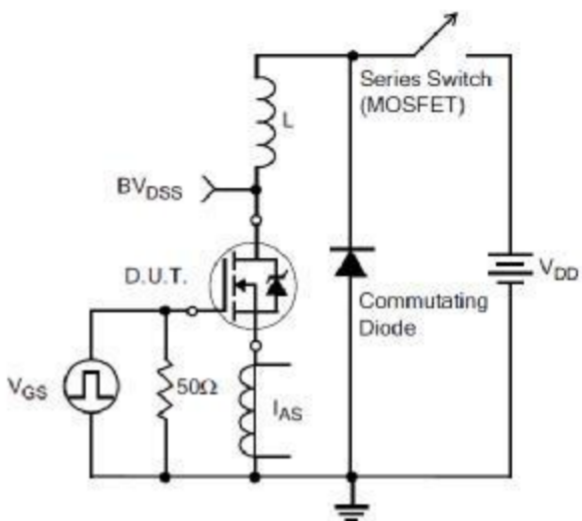
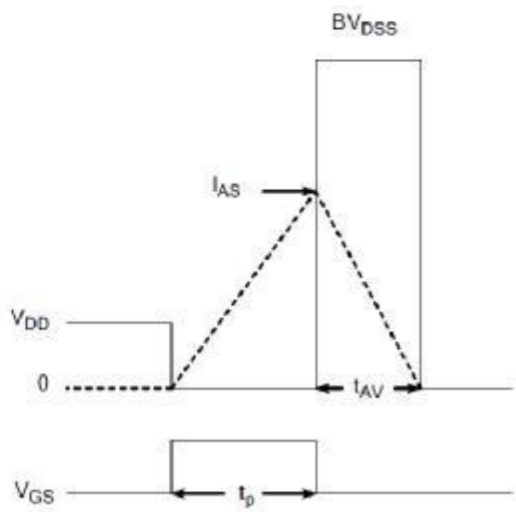


Figure 23. Unclamped Inductive Switching Test Circuit



$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

Figure 24. Unclamped Inductive Switching Waveforms

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