DESCRIPTION

The IRF7410TR is the P-Channel logic enhancement mode power field effect transistor is produced using high cell density advanced trench technology..

This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching

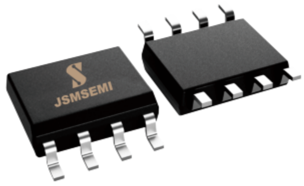
FEATURE

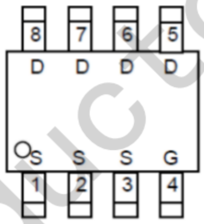
- ***-30V/-15A, $R_{DS(ON)}$=8mΩ (typ.)@V_{GS}=-10V***
- ***-30V/-10A, $R_{DS(ON)}$=10mΩ (typ.)@V_{GS}=-4.5V***
- Super high design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and Maximum DC current capability
- Full RoHS compliance
- SOP8 package design

APPLICATIONS

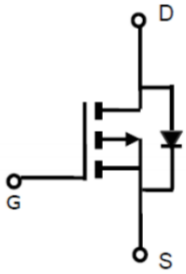
- High Frequency Point-of-Load Synchronous
- Newworking DC-DC Power System
- Load Switch

PIN CONFIGURATION





TOP VIEW
SOP-8



P-Channel

ABSOLUTE MAXIMUM RATINGS *(T_A = 25℃ Unless otherwise noted)*

Symbol	Parameter		Typical	Unit
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Continuous Drain Current (T_A=25℃)	V_{GS}=10V	-14	A
I_{DM}	Pulsed Drain Current		-70	A
I_S	Continuous Source Current (Diode Conduction)		-2.7	A
P_D	Power Dissipation	T_A=25℃	3.0	W
		T_A=70℃	2.1	
T_J	Operation Junction Temperature		150	℃
T_{STG}	Storage Temperature Range		-55~+150	℃
$R_{θJA}$	Thermal Resistance Junction to Ambient		85	℃/W

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress rating only and functional device operation is not implied

■ *ELECTRICAL CHARACTERISTICS(T_A=25℃ Unless otherwise noted)*

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-1.0	-1.3	-2.0	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-24V, V_{GS}=0			-1	uA
		V_{DS}=-24V, V_{GS}=0 T_J=55℃			-5	
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=-10V, I_D=-15A		8.5	11	mΩ
		V_{GS}=-4.5V, I_D=-10A		10	13	
Source-Drain Diode						
V_{SD}	Diode Forward Voltage	I_S=-1.0A, V_{GS}=0V		-0.71	-1.0	V
Dynamic Parameters						
Q_g	Total Gate Charge	V_{DS}=-15V		37.08	48.2	nC
Q_{gs}	Gate-Source Charge	V_{GS}=-4.5V		10.12	13.16	
Q_{gd}	Gate-Drain Charge	I_D=-15A		11.24	14.61	
C_{iss}	Input Capacitance	V_{DS}=-15V		3887		pF
C_{oss}	Output Capacitance	V_{GS}=0V		577		
C_{rss}	Reverse Transfer Capacitance	f=1MHz		425		
$T_{d(on)}$	Turn-On Time	V_{DS}=-15V		19.52	39.04	nS
T_r		I_D=-10A		10.12	20.34	
$T_{d(off)}$	Turn-Off Time	V_{GEN}=-10V		137.6	275.2	
T_f		R_G=6Ω		55.32	110.64	

Note: 1. Pulse test: pulse width<=300uS, duty cycle<=2%

2.Static parameters are based on package level with recommended wire bonding

TYPICAL CHARACTERISTICS (25℃ Unless Note)

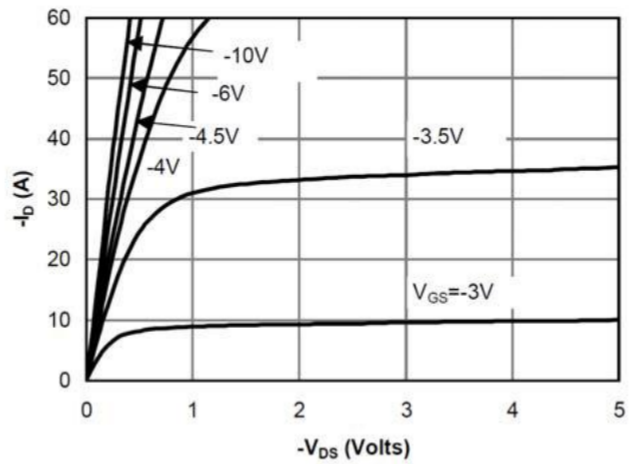


Fig 1: On-Region Characteristics

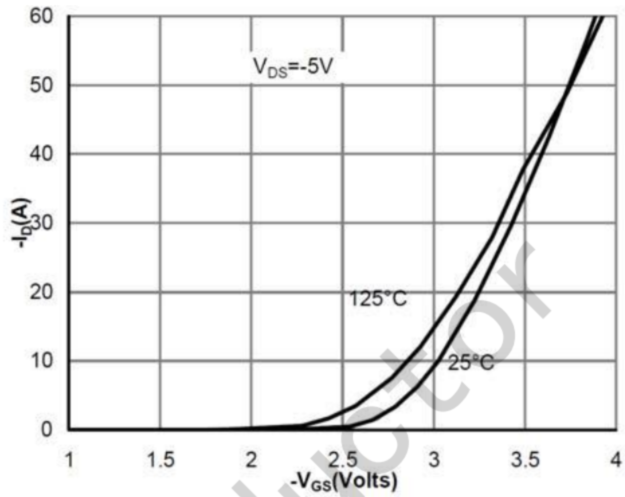


Figure 2: Transfer Characteristics

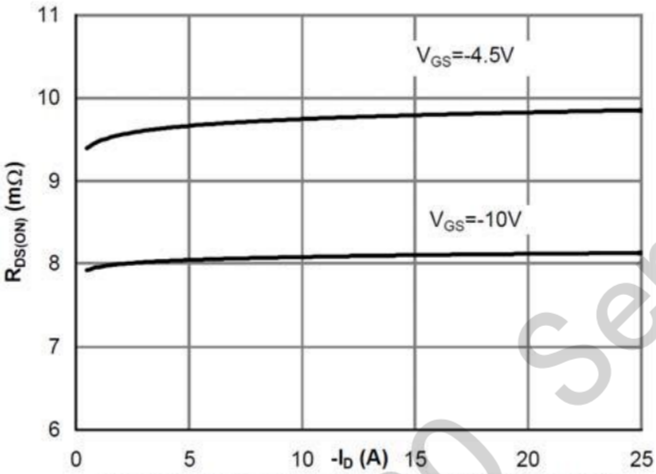


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

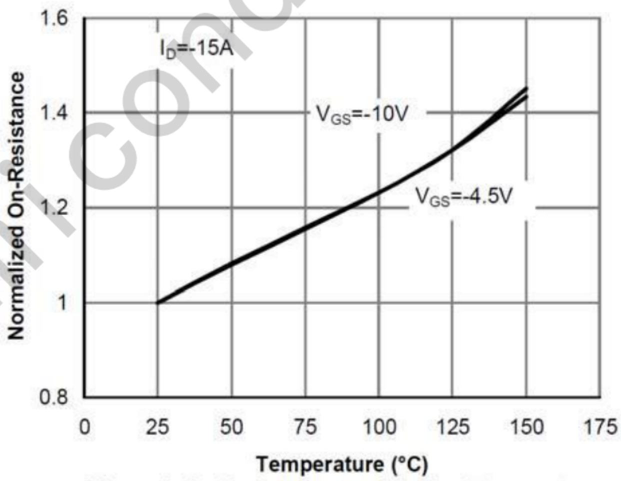


Figure 4: On-Resistance vs. Junction Temperature

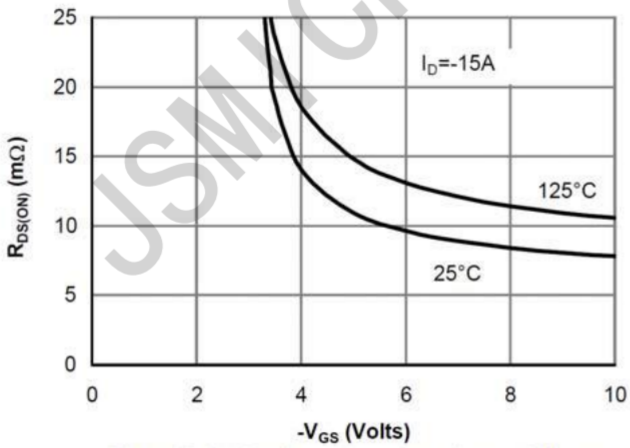


Figure 5: On-Resistance vs. Gate-Source Voltage

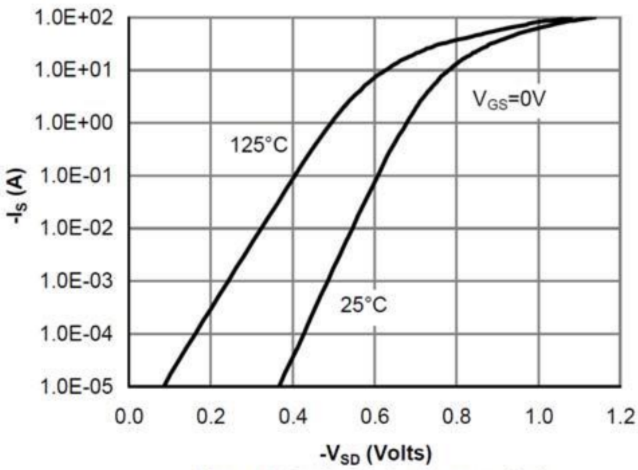


Figure 6: Body-Diode Characteristics

■ *TYPICAL CHARACTERISTICS (continuous)*

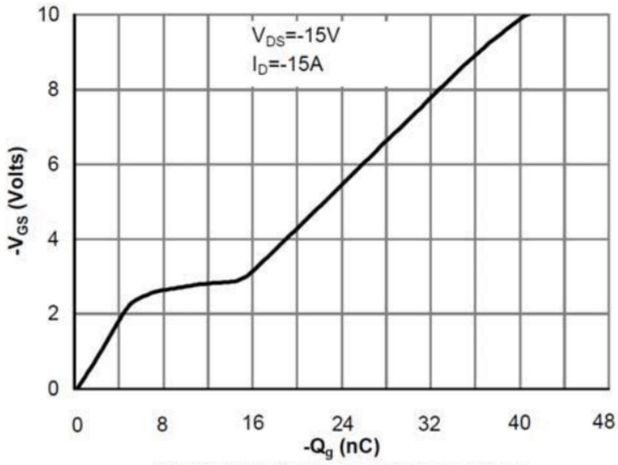


Figure 7: Gate-Charge Characteristics

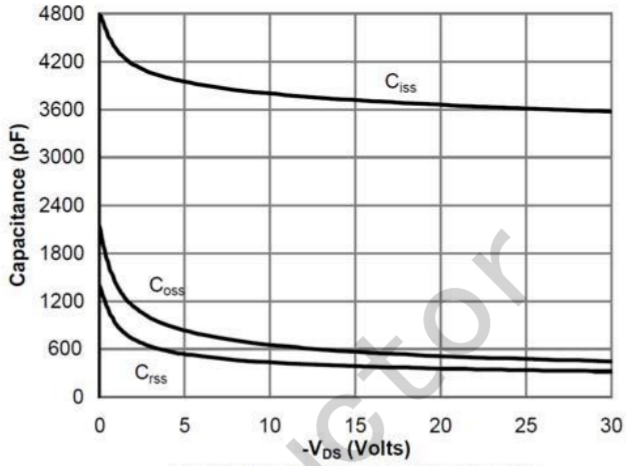


Figure 8: Capacitance Characteristics

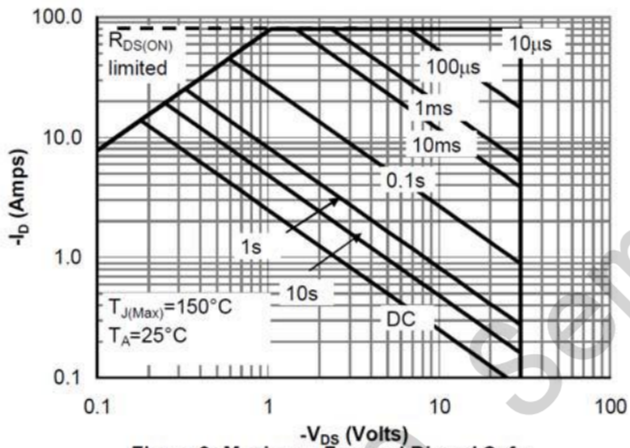


Figure 9: Maximum Forward Biased Safe Operating Area

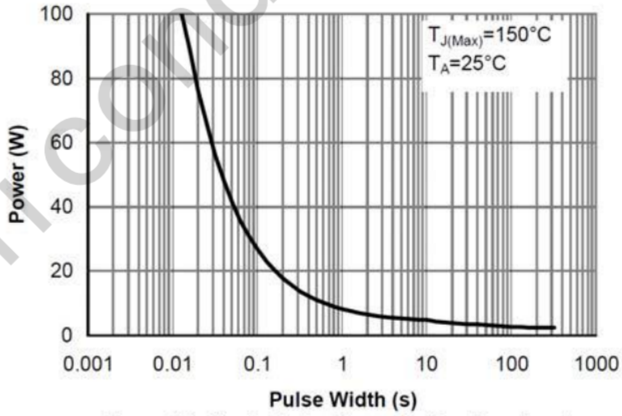


Figure 10: Single Pulse Power Rating Junction-to-Ambient

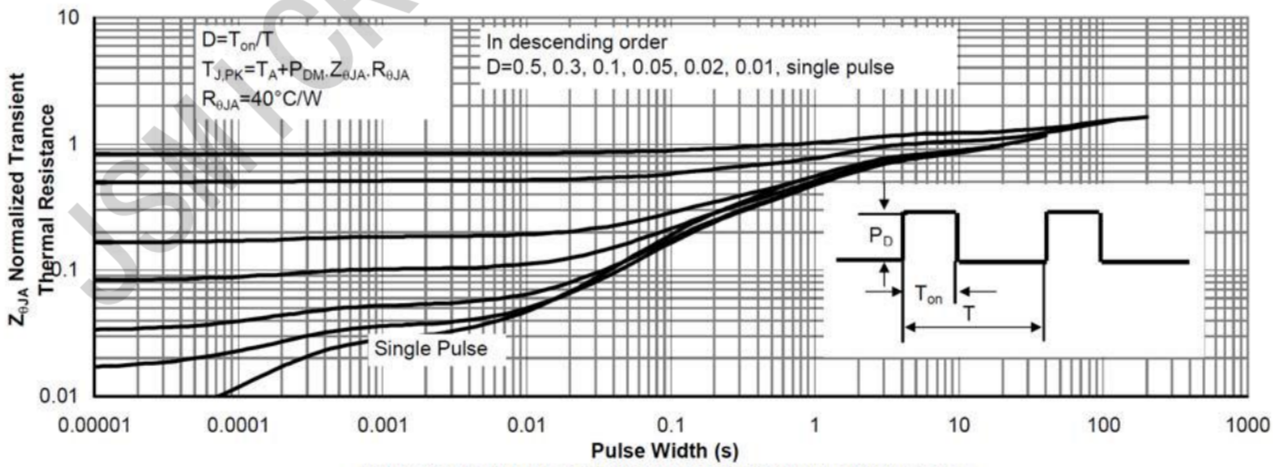
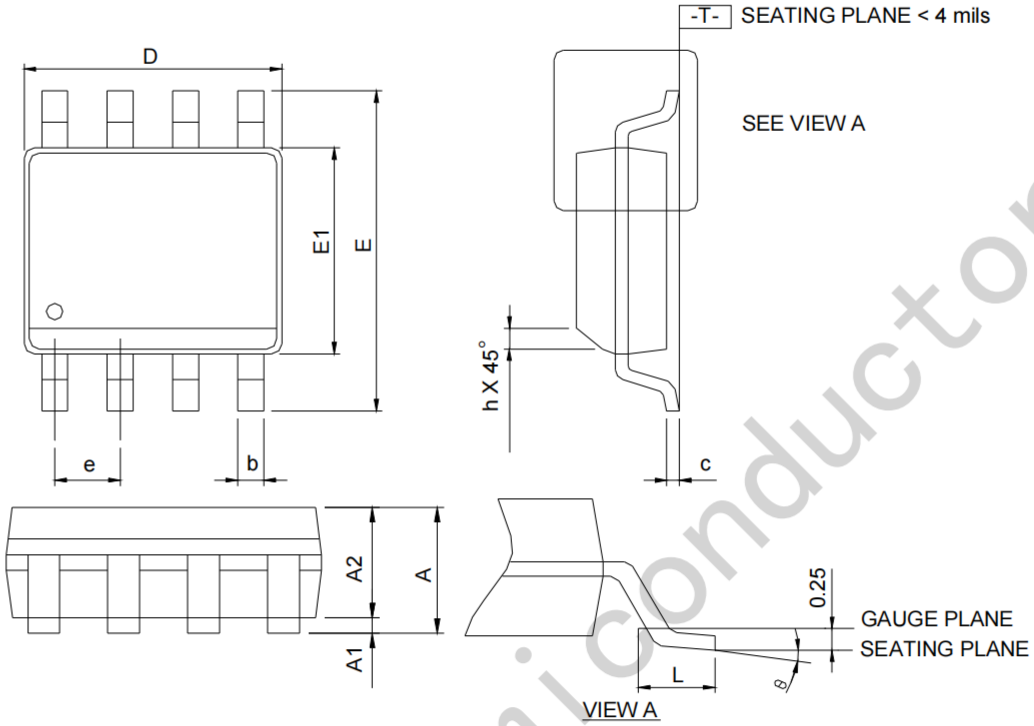


Figure 11: Normalized Maximum Transient Thermal Impedance

Package Information

SOP-8



SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.75	-	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	-	0.049	-
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AA.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

RECOMMENDED LAND PATTERN