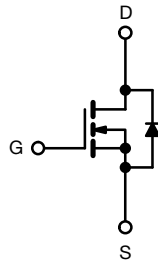
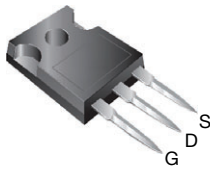


## Power MOSFET

TO-247AC



N-Channel MOSFET

### FEATURES

- Low figure-of-merit  $R_{on} \times Q_g$
- 100 % avalanche tested
- High peak current capability
- $dv/dt$  ruggedness
- Improved  $T_{rr}/Q_{rr}$
- Improved gate charge
- High power dissipations capability
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available

### PRODUCT SUMMARY

$V_{DS}$ (V) at $T_J$ max.	560	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10$ V	0.270
$Q_g$ max. (nC)	76	
$Q_{gs}$ (nC)	21	
$Q_{gd}$ (nC)	34	
Configuration	Single	

### ORDERING INFORMATION

Package	TO-247AC
Lead (Pb)-free	SiHG20N50C-E3
Lead (Pb)-free and halogen-free	SiHG20N50C-GE3

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	$V_{DS}$	500	V	
Gate-source voltage	$V_{GS}$	$\pm 30$		
Continuous drain current ( $T_J = 150$ °C) <sup>a</sup>	$V_{GS}$ at 10 V	$T_C = 25$ °C	20	A
		$T_C = 100$ °C	11	
Pulsed drain current <sup>b</sup>	$I_{DM}$	80		
Linear derating factor		1.8	W/°C	
Single pulse avalanche energy <sup>c</sup>	$E_{AS}$	361	mJ	
Maximum power dissipation	$P_D$	250	W	
Reverse diode $dv/dt$ <sup>d</sup>	$dv/dt$	5	V/ns	
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C	
Soldering recommendations (peak temperature) <sup>d</sup>	For 10 s	300		


#### Notes

- Limited by maximum junction temperature
- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 2.5$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 17$  A
- $I_{SD} \leq 18$  A,  $di/dt \leq 380$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150$  °C
- 1.6 mm from case

### THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	-	40	°C/W
Maximum junction-to-case (drain)	$R_{thJC}$	-	0.5	



SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	500	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA	-	0.7	-	V/°C
Gate-source threshold voltage (N)	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	3.0	-	5.0	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 30 V	-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V	-	-	25	μA
		V <sub>DS</sub> = 400 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C	-	-	250	
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A	-	0.225	0.270	Ω
Forward transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 10 A	-	6.4	-	S
<b>Dynamic</b>						
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1 MHz	-	2451	2942	pF
Output capacitance	C <sub>oss</sub>		-	300	360	
Reverse transfer capacitance	C <sub>rss</sub>		-	26	32	
Total gate charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 18 A, V <sub>DS</sub> = 400 V	-	65	76	nC
Gate-source charge	Q <sub>gs</sub>		-	21	-	
Gate-drain charge	Q <sub>gd</sub>		-	29	-	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 250 V, I <sub>D</sub> = 18 A, R <sub>g</sub> = 9.1 Ω	-	80	-	ns
Rise time	t <sub>r</sub>		-	27	-	
Turn-off delay time	t <sub>d(off)</sub>		-	32	-	
Fall time	t <sub>f</sub>		-	44	-	
Gate input resistance	R <sub>g</sub>	f = 1 MHz, open drain	-	1.1	-	Ω
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	20	A
Pulsed diode forward current	I <sub>SM</sub>		-	-	80	
Diode forward voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 18 A, V <sub>GS</sub> = 0 V	-	-	1.5	V
Reverse recovery time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = I <sub>S</sub> , di/dt = 100 A/μs, V <sub>R</sub> = 35 V	-	503	-	ns
Reverse recovery charge	Q <sub>rr</sub>		-	6.7	-	μC
Reverse recovery current	I <sub>RRM</sub>		-	30	-	A

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

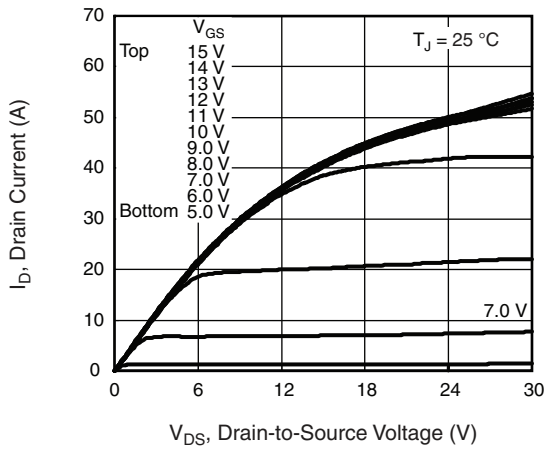


Fig. 1 - Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^\circ\text{C}$

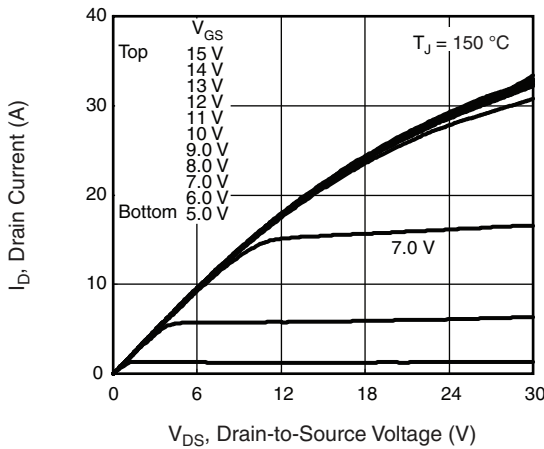


Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^\circ\text{C}$

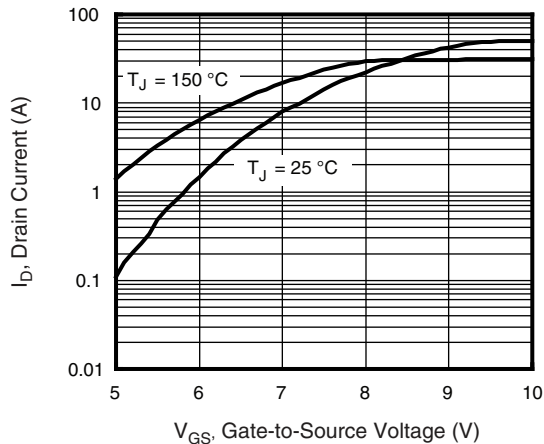


Fig. 3 - Typical Transfer Characteristics

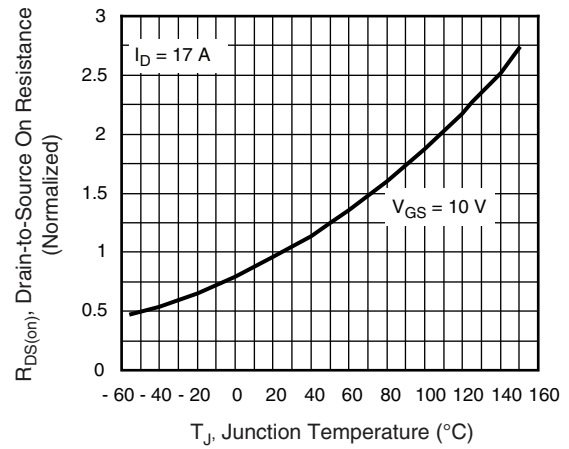


Fig. 4 - Normalized On-Resistance vs. Temperature

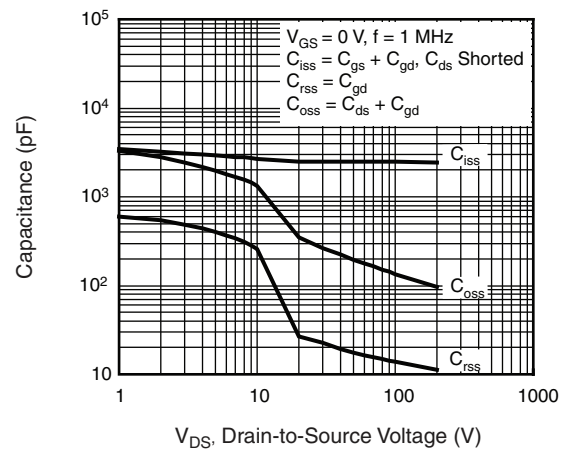


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

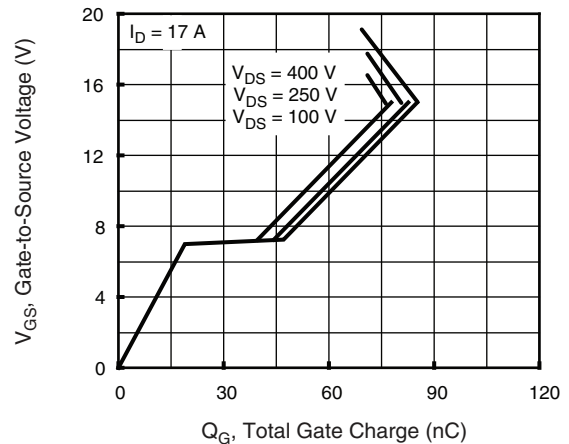


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

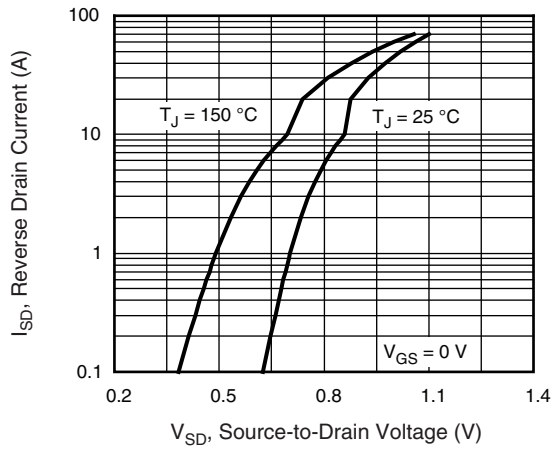


Fig. 7 - Typical Source-Drain Diode Forward Voltage

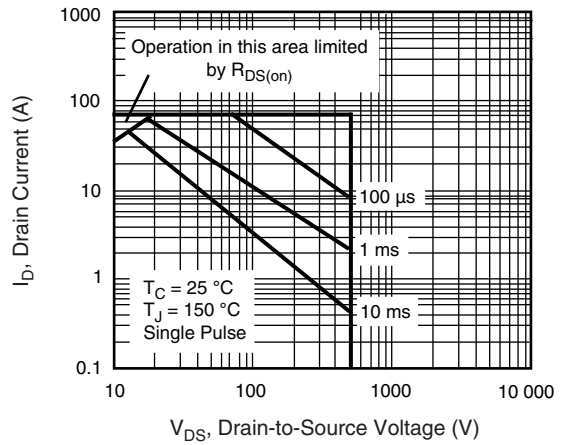


Fig. 8 - Maximum Safe Operating Area

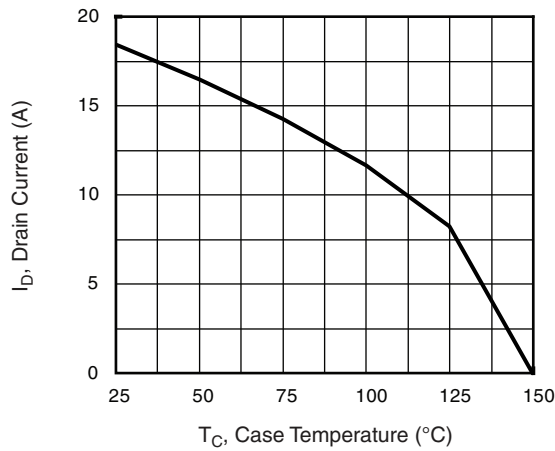


Fig. 9 - Maximum Drain Current vs. Case Temperature

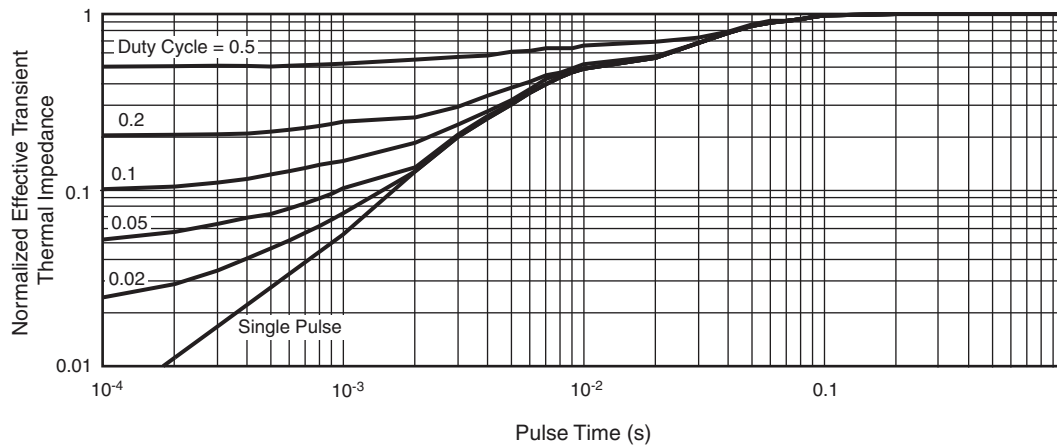


Fig. 10 - Normalized Thermal Transient Impedance, Junction-to-Case (TO-247)

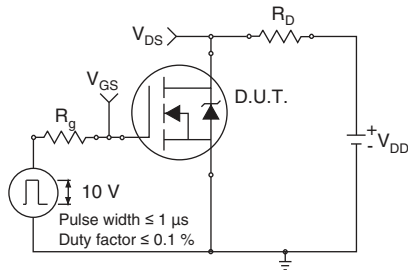


Fig. 11 - Switching Time Test Circuit



Fig. 15 - Basic Gate Charge Waveform

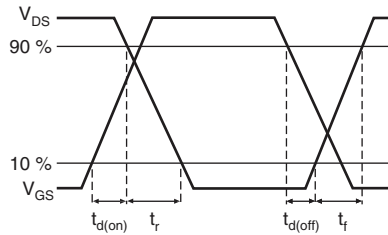


Fig. 12 - Switching Time Waveforms

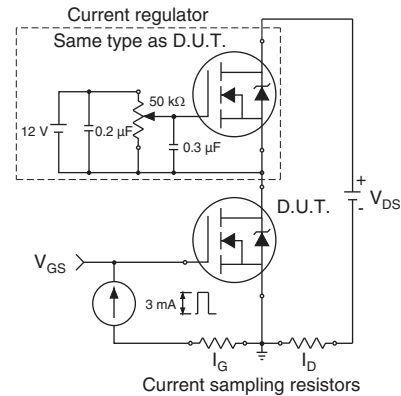


Fig. 16 - Gate Charge Test Circuit

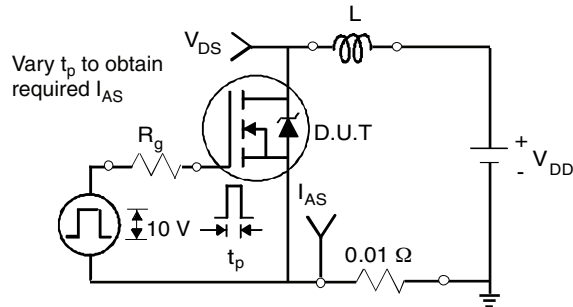


Fig. 13 - Unclamped Inductive Test Circuit

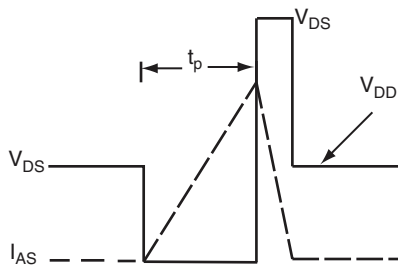
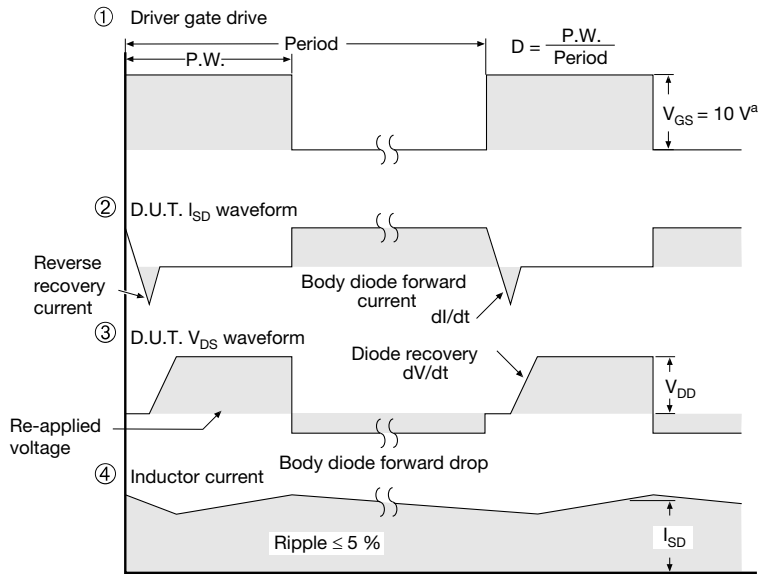
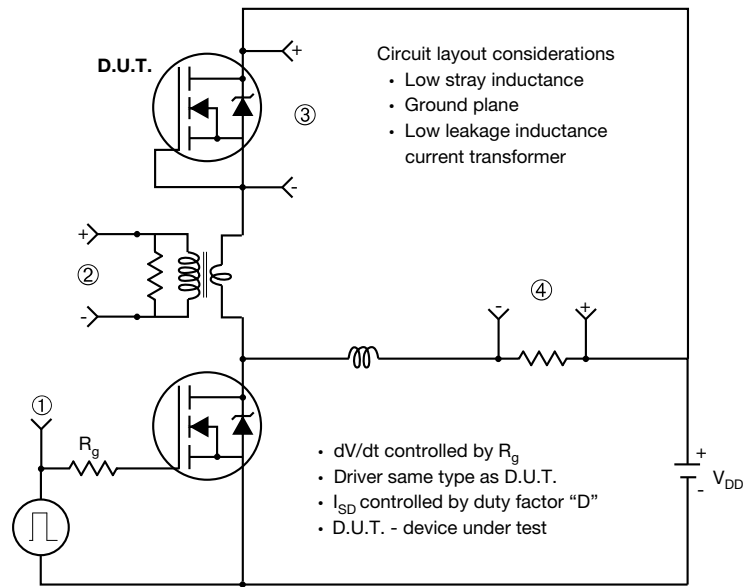


Fig. 14 - Unclamped Inductive Waveforms

**Peak Diode Recovery dV/dt Test Circuit**



**Note**

a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 17 - For N-Channel**

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# TO-247AC (High Voltage)

VERSION 1: FACILITY CODE = 9



Section C--C, D---D, E--E

DIM.	MILLIMETERS		NOTES
	MIN.	MAX.	
A	4.83	5.21	
A1	2.29	2.55	
A2	1.50	2.49	
b	1.12	1.33	
b1	1.12	1.28	
b2	1.91	2.39	6
b3	1.91	2.34	
b4	2.87	3.22	6, 8
b5	2.87	3.18	
c	0.55	0.69	6
c1	0.55	0.65	
D	20.40	20.70	4

DIM.	MILLIMETERS		NOTES
	MIN.	MAX.	
D1	16.25	16.85	5
D2	0.56	0.76	
E	15.50	15.87	4
E1	13.46	14.16	5
E2	4.52	5.49	3
e	5.44 BSC		
L	14.90	15.40	
L1	3.96	4.16	6
Ø P	3.56	3.65	7
Ø P1	7.19 ref.		
Q	5.31	5.69	
S	5.54	5.74	

### Notes

- (1) Package reference: JEDEC® TO247, variation AC
- (2) All dimensions are in mm
- (3) Slot required, notch may be rounded
- (4) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body
- (5) Thermal pad contour optional with dimensions D1 and E1
- (6) Lead finish uncontrolled in L1
- (7) Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm
- (8) Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition



**VERSION 2: FACILITY CODE = Y**



DIM.	MILLIMETERS		NOTES
	MIN.	MAX.	
A	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
c	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	-	

DIM.	MILLIMETERS		NOTES
	MIN.	MAX.	
D2	0.51	1.30	
E	15.29	15.87	
E1	13.72	-	
e	5.46 BSC		
Ø k	0.254		
L	14.20	16.25	
L1	3.71	4.29	
Ø P	3.51	3.66	
Ø P1	-	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

ECN: E19-0614-Rev. E, 08-Jan-2020  
 DWG: 5971

**Notes**

- (1) Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
- (7) Outline conforms to JEDEC outline TO-247 with exception of dimension c





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