Description：

CD4011 is a low-power, wide range working voltage 2-input NAND gate integrated circuit designed using CMOS technology. It integrates four independent 2-input NAND gate circuits internally, with high anti-interference and driving capabilities.

Features：

-Low input current: IIN ≤ 1uA, @ VIN=VDD=15V, Ta=25 ℃
- Low static power consumption: IDD ≤ 6uA, @ VDD=15V, Ta=25 ℃
-Wide operating voltage range: 3.0Vto15.0V
-Encapsulation form: DIP14, SOP14

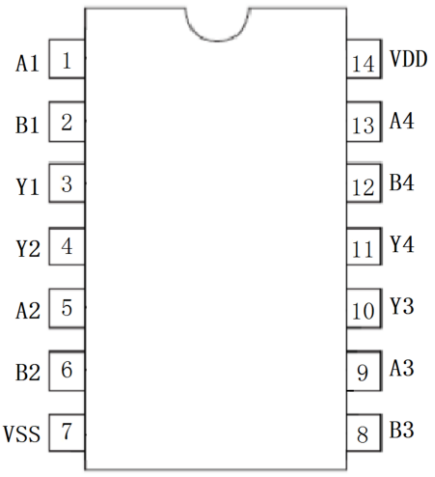
Application:

-Digital Logic Driven
-Industrial control applications
-Wireless doorbell
-Other application areas

Pin Assignment：

PIN NO. DIP14/SOP14	Definition	PIN NO. DIP14/SOP14	Definition
1	A1	14	VDD
2	B1	13	B4
3	Y1	12	A4
4	Y2	11	Y4
5	A2	10	Y3
6	B2	9	B3
7	VSS	8	A3

DIP14/SOP14

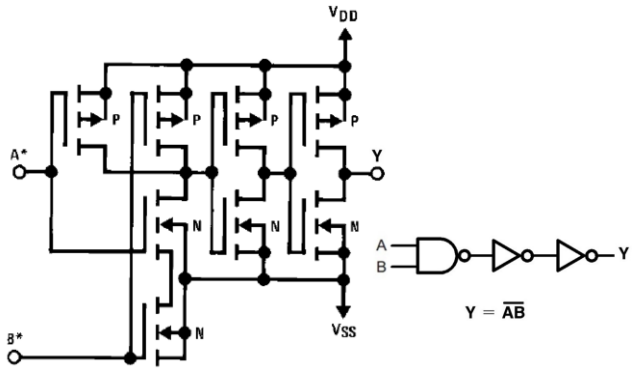


Absolute Maximum Ratings：

parameter	Symbol	Max	Unit
working voltage	V_{CC}	-0.5-20	V
Input/output voltage	V_{IN}、$V_{I/O}$	-0.5+VSS-VDD+0.5V	V
Dissipated power	P_D	500	mW
working temperature	T_A	0-70	℃
Storage temperature	T_S	-65-150	℃
Pin welding temperature	T_W	260,10s	℃

Note: Limit parameters refer to the limit values that cannot be exceeded under any conditions. If the limit value is exceeded, it may cause physical damage such as product degradation; At the same time, it cannot be guaranteed that the chip can function properly when approaching the limit parameters.

logic diagram



Truth table

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Recommended operating conditions

parameter	Symbol	Min	Typ	Max	Unit
working voltage	V_{DD}	2.5		15	V
Input and output voltage	V_{IN}、$V_{I/O}$	0		VDD	V
working temperature	T_A	0		60	℃

electrical characteristic

DC electrical characteristics:(Ta=25°C)

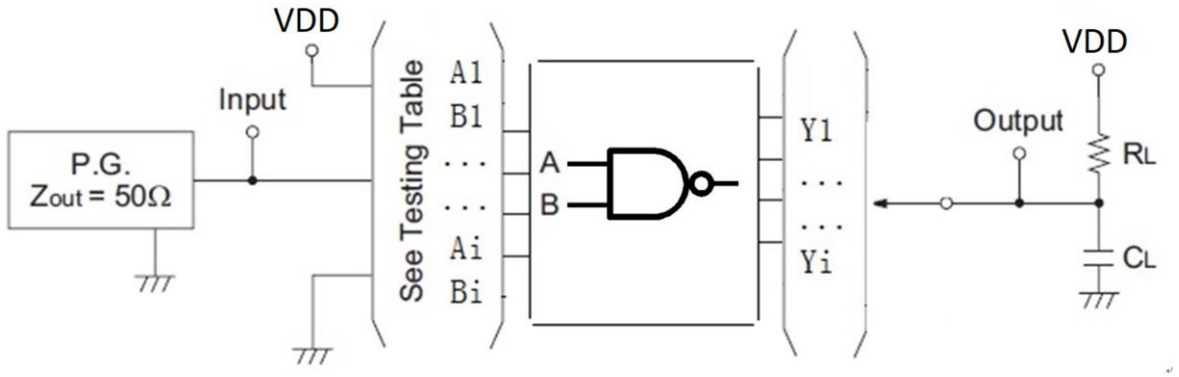
symbol	parameter	Test conditions		VDD（V）	min	typ	max	unit
V_{IH}	High level effective input voltage	$|I_O|\leqslant$1uA	Vo= 0.5V	5	3.5			V
			Vo= 1V	10	7.0			V
			Vo= 1.5V	15	11.0			V
V_{IL}	Low level effective input voltage	$|I_O|\leqslant$1uA	Vo= 4.5V	5			1.5	V
			Vo= 9V	10			3.0	V
			Vo=13.5V	15			4.0	V
V_{OH}	high level output voltage	$\|I_{OUT}\|$<1uA		5	4.95			V
				10	9.95			V
				15	14.95			V
V_{OL}	Low Level Output Voltage	$\|I_{OUT}\|$<1uA		5			0.05	V
				10			0.05	V
				15			0.05	V
I_{IN}	Input Current	V_{IN}=VDD or VSS		15		0.01	1.0	uA
I_{OH}	High Level Output Current	Vo= 4.6V		5		-1.0	-0.5	mA
		Vo= 9.5V		10		-2.1	-1.3	mA
		Vo= 13.5V		15		-8.0	-3.4	mA
I_{OL}	Low Level Output Current	Vo= 0.4V		5	0.5	2.2		mA
		Vo= 0.5V		10	1.3	5.1		mA
		Vo= 1.5V		15	3.4	19		mA
I_{DD}	Working current	V_{IN}=VDD or VSS		5		0.1	4	uA
				10		0.1	5	uA
				15		0.1	6	uA

AC electrical characteristics: Ta=25 ℃, RL=200k, CL=47pF, see test method.

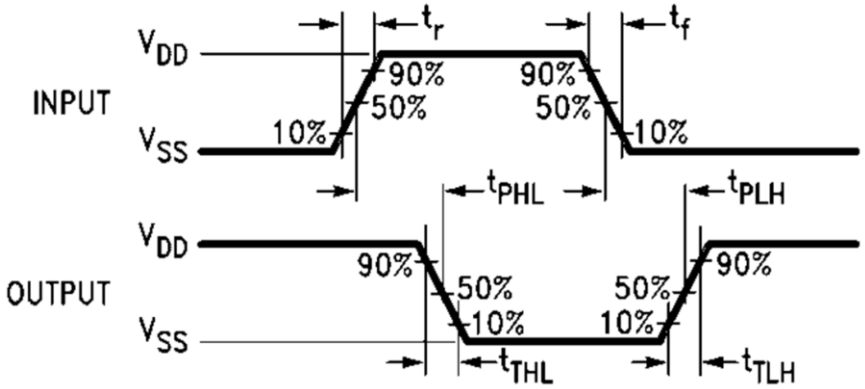
parameter	symbol	Test conditions	min	typ	max	unit
最大传输延迟时间 A、B to Y	t_{PHL}	VDD=5V		62		ns
	t_{PLH}			55		ns
	t_{PHL}	VDD=10V		35		ns
	t_{PLH}			35		ns
	t_{PHL}	VDD=15V		30		ns
	t_{PLH}			28		ns

test method

1. Test wiring diagram



2. Schematic diagram of waveform measurement

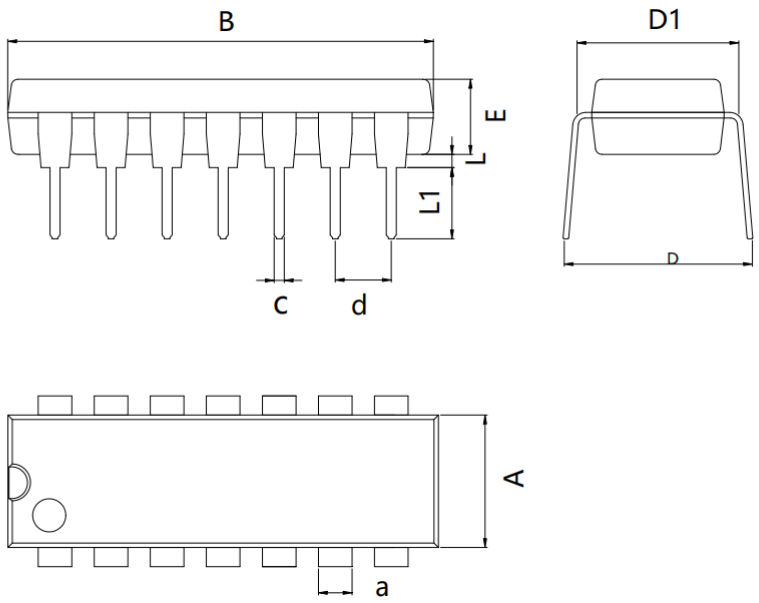


Note:

1. See Testing Table refers to the corresponding testing items in the A C electrical characteristics table;
2. The CL capacitor is an external patch capacitor (0603), connected n ear the output pin, and the capacitor ground is close to the chip VSS;
3. Input: Port input level, f=1MHz, D=50% square wave, tr=tf ⩽ 20ns;
4. Output: Y-end output test.

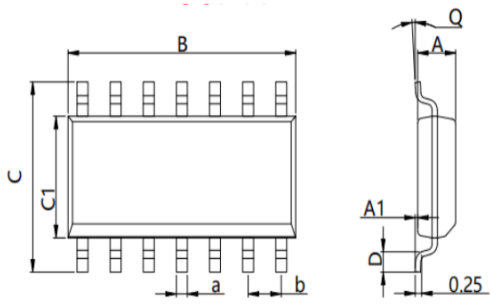
PACKAGE MECHANICAL DATA

DIP14



Dimensions In Millimeters(DIP14)										
Symbol:	A	B	D	D1	E	L	L1	a	C	d
Min:	6.10	18.94	8.40	7.42	3.10	0.50	3.00	1.50	0.40	2.54 BSC
Max:	6.68	19.56	9.00	7.82	3.55	0.70	3.60	1.55	0.50	

SOP14



Dimensions In Millimeters(SOP14)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	8.55	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	8.75	6.20	4.00	0.80	8°	0.45	