Description：

CD4013 is a D-type flip-flop designed using advanced CMOS technology. It consists of two identical and independent D-type data triggers. Each trigger has independent data, setting, reset, and clock inputs, as well as Q and $\overline{Q}$ outputs. The two high-level effective setting and reset input terminals are independent of the clock input. During the rising edge of the clock pulse, the logic level of the D input terminal is output to the Q output terminal. These functions can be used for shift register applications and for counter and switching applications by connecting the Q output to the data input.

Features：

-Low input current: IIN ≤ 1uA, @ VIN=VDD=15V, Ta=25 ℃
- Wide operating voltage range: 3.0V to 15.0V
-Low static power consumption: typical value IDD=0.01uA, @ VDD=15V, Ta=25 ℃
- asynchronous setting reset function
-Encapsulation form: DIP14, SOP14

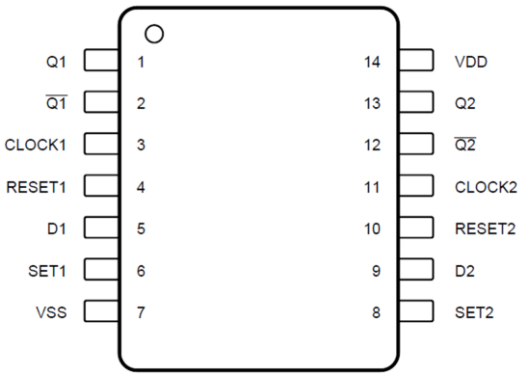
Application:

-Power transmission
-Building automation
-Power grid infrastructure
-Other application areas
-Health and fitness equipment
-Testing and Measurement
-Telecommunications infrastructure

Pin Assignment：

pin no.	Symbol	Definition	pin no.	Symbol	Definition
1	Q1	Positive output 1	14	VDD	VDD
2	$\overline{Q1}$	Reverse output 1	13	Q2	Positive output 2
3	CLOCK1	CLOCK1	12	$\overline{Q2}$	Reverse output 2
4	RESET1	Reset terminal 1	11	CLOCK2	CLOCK2
5	D1	Data input 1	10	RESET2	Reset terminal 2
6	SET1	Set 1 end	9	D2	Data input 2
7	VSS	VSS	8	SET2	Set 2 end

DIP14/SOP14

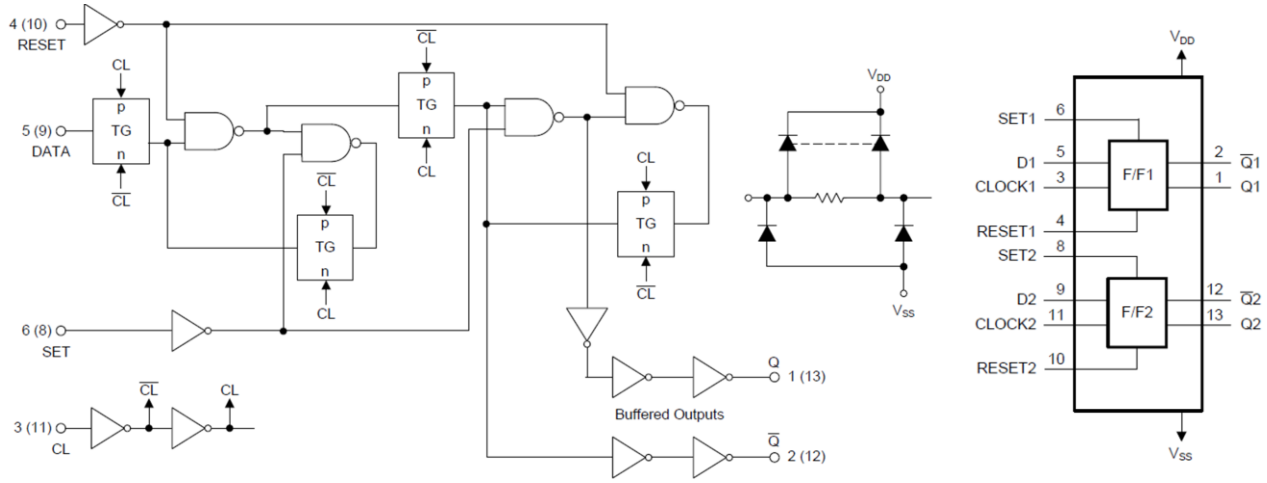


Absolute Maximum Ratings：

parameter	Symbol	Max	Unit
working voltage	V_{CC}	-0.5-18	V
Input/output voltage	V_{IN}、$V_{I/O}$	-0.5+VSS-VDD+0.5V	V
Input current	I_I	±10	mA
Dissipated power	P_D	500	mW
working temperature	T_A	0-70	℃
Storage temperature	T_S	-65-150	℃
Pin welding temperature	T_W	260,10s	℃

Note: Limit parameters refer to the limit values that cannot be exceeded under any conditions. If the limit value is exceeded, it may cause physical damage such as product degradation; At the same time, it cannot be guaranteed that the chip can function properly when approaching the limit parameters.

logic diagram



Truth table

INPUTS				OUTPUTS	
CLOCK	SET	RESET	D	Q	$\overline{Q}$
↑	L	L	L	L	H
↑	L	L	H	H	L
↓	L	L	×	Q_0	$\overline{Q}$
×	L	H	×	L	H
×	H	L	×	H	L
×	H	H	×	H	H

Note: L represents low level; H represents high level; ↓ represents the descending edge; ↑ represents the rising edge; X represents any level.

Recommended operating conditions

parameter	symbol	VDD(V)	min	typ	max	unit
working voltage	V_{DD}		3		15	V
Input and output voltage	V_{IN}、$V_{I/O}$		0		VDD	V
Data Setup Time	ts	5	40			ns
		10	20			
		15	15			
Clock pulse width	tw	5	140			ns
		10	60			
		15	40			
Reset and set pulse width (RESET or SET)	tw	5	180			ns
		10	80			
		15	50			

electrical characteristic

DC electrical characteristics:(Ta=25℃)

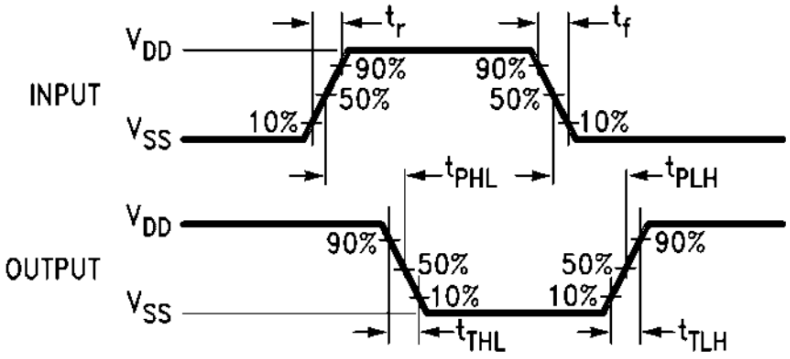
symbol	parameter	Test conditions		VDD（V)	min	typ	max	unit
V_{IH}	High level effe ctive input voltage	$|I_O|\leqslant$1uA	Vo= 0.5V	5	3.5			V
			Vo= 1V	10	7.0			V
			Vo= 1.5V	15	11.0			V
V_{IL}	Low level effective input voltage	$|I_O|\leqslant$1uA	Vo= 4.5V	5			1.5	V
			Vo= 9V	10			3.0	V
			Vo=13.5V	15			4.0	V
V_{OH}	High level output voltage	$\|I_{OUT}\|$<1uA		5	4.95			V
				10	9.95			V
				15	14.95			V
V_{OL}	Low level output voltage	$\|I_{OUT}\|$<1uA		5			0.05	V
				10			0.05	V
				15			0.05	V
I_{IN}	Input current	V_{IN}=VDD or VSS		15		0.01	1.0	uA
I_{OH}	High level output current	Vo= 4.6V		5		-1.6		mA
		Vo= 2.5V		5		-7.2		mA
		Vo= 9.5V		10		-3.4		mA
		Vo= 13.5V		15		-12.5		mA
I_{OL}	Low level output current	Vo= 0.4V		5		1.5		mA
		Vo= 0.5V		10		2.5		mA
		Vo= 1.5V		15		8.3		mA
I_{DD}	Working current	V_{IN}=VDD or VSS		5		0.01	2	uA
				10		0.01	5	uA
				15		0.01	10	uA

AC electrical characteristics: Ta=25 ℃, RL=20k, CL=51pF, see testing method.

parameter	symbol	Test conditions	min	typ	max	unit
CLOCK to Q or $\overline{Q}$	t_{PHL} t_{PLH}	VDD=5V		100		ns
		VDD=10V		60		ns
		VDD=15V		30		ns
Set to Q or reset to $\overline{Q}$	t_{PLH}	VDD=5V		80		ns
		VDD=10V		50		ns
		VDD=15V		25		ns
Set to $\overline{Q}$ or reset to Q	t_{PHL}	VDD=5V		100		ns
		VDD=10V		60		ns
		VDD=15V		30		ns
Transition time	t_{THL} t_{TLH}	VDD=5V		40		ns
		VDD=10V		30		ns
		VDD=15V		20		ns

test method

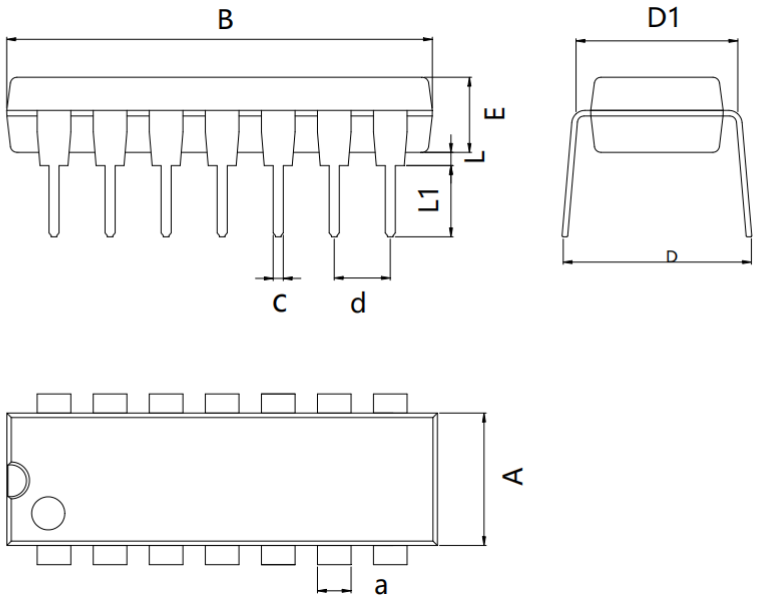
1. Measurement wiring and waveform diagram



Note: 1. Refers to the corresponding test items in the AC electrical characteristics table;
2. The CL capacitor is an external patch capacitor (0603), connected near the output pin, and the capacitor ground is close to the chip VSS;
3. Input: Port input level, f=1MHz, D=50% square wave, tr=tf ≤ 20ns;
4. Output: Y-end output test.

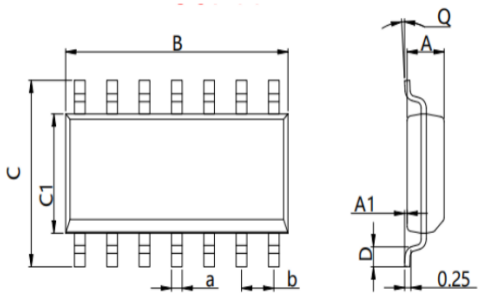
PACKAGE MECHANICAL DATA

DIP14



Dimensions In Millimeters(DIP14)										
Symbol:	A	B	D	D1	E	L	L1	a	C	d
Min:	6.10	18.94	8.40	7.42	3.10	0.50	3.00	1.50	0.40	2.54 BSC
Max:	6.68	19.56	9.00	7.82	3.55	0.70	3.60	1.55	0.50	

SOP14



Dimensions In Millimeters(SOP14)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	8.55	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	8.75	6.20	4.00	0.80	8°	0.45	