Description:

CD4016 is a low-power, wide range operating voltage bidirectional electronic switch integrated circuit designed using advanced CMOS technology. It integrates four independent switching circuits internally, with extremely small switch on resistance and extremely low leakage current, and has high anti-interference and driving capabilities.

Features:

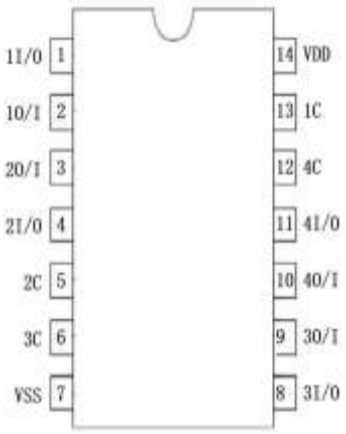
-Low input current: IIN ≤ 1uA, @ VIN=VDD=15V, Ta=25 ℃
-Low static power consumption: IDD=0.01uA, Typ@ VDD=15V, Ta=25 ℃
-Wide working voltage range: 3.0V to 15.0V
-Packaging form: DIP14, SOP14

Application:

-Electronic switch
-Industrial control applications
-Bidirectional I/O port
-Other application areas

Packaging form and pin function definition

PIN NO.	Pin Definition	Pin Description	PIN NO.	Pin Definition	Pin Description
1	1I/O	1st bidirectional I/O port	14	VDD	Power supply positive
2	1O/I	1st bidirectional O/I port	13	1C	1st switch control terminal
3	2O/I	2nd bidirectional O/I port	12	4C	4th switch control terminal
4	2I/O	2nd bidirectional I/O port	11	4I/O	4th bidirectional O/I port
5	2C	2nd switch control terminal	10	4O/I	4th bidirectional O/I port
6	3C	3rd switch control terminal	9	3O/I	Third two-way O/I port
7	VSS	Power supply ground	8	3I/O	Third two-way O/I port

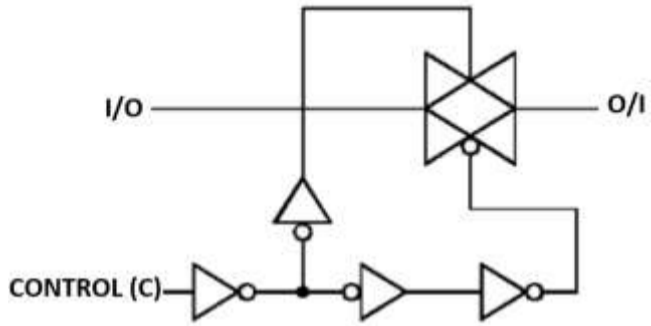


Absolute Maximum Ratings:

parameter	symbol	Limit value	unit
working voltage	V_{CC}	-0.5-18	V
Input/output voltage	V_{IN}、$V_{I/O}$	-0.5+VSS-VDD+0.5V	V
Input/output clamp current	I_{IK}、$I_{I/OK}$	±20	mA
Single pin output current	I_{OUT}	±25	mA
Single pin connected to VCC or GND current	I_{CC}	±50	mA
Dissipated power	P_D	500	mW
working temperature	T_A	0-70	℃
Storage temperature	T_S	-65-150	℃
Pin welding temperature	T_W	260,10s	℃

Note: Limit parameters refer to the limit values that cannot be exceeded under any conditions. If the limit value is exceeded, it may cause physical damage such as product degradation; At the same time, it cannot be guaranteed that the chip can function properly when approaching the limit parameters.

logic diagram



Truth table

CONTROL	SWITCH FUNCTION
H	ON
L	OFF

Working conditions

paramater	symbol	min	typ	max	unit
working voltage	V_{DD}	3		15	V
Input and output voltage	V_{IN}、$V_{I/O}$	0		VDD	V
working temperature	T_A	0		60	℃

electrical properties

DC electrical characteristics: (Ta=25℃)

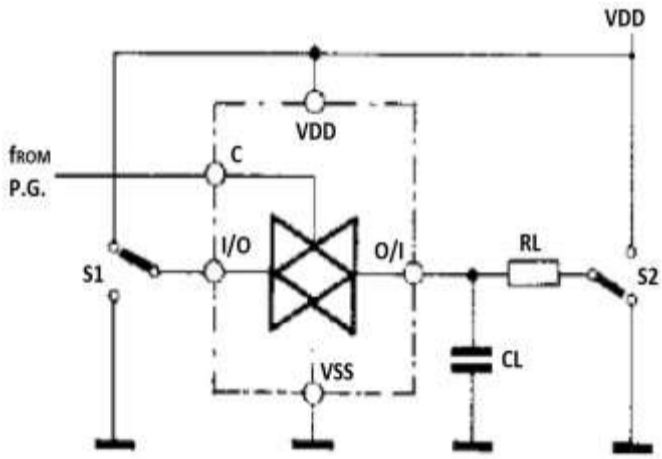
symbol	item	test conditions	VDD (V)	min	typ	max	unit
V_{IHC}	High level effective input voltage	V_{IS} = V_{SS} and V_{DD} , V_{OS} = V_{DD} and V_{SS} or 15V, $\|I_{IS}\|$=10uA	5	3.5			V
			10	7.0			V
			15	11.0			V
V_{ILC}	Low level effective input voltage	V_{IS} = V_{SS} and V_{DD} , V_{OS} = V_{DD} and V_{SS} or 15V, $\|I_{IS}\|$=10uA	5			1.5	V
			10			3.0	V
			15			4.0	V
I_{INC}	Input current	V_C=15V or 0V	15		0.01	1.0	uA
R_{ON}	Switch conduction resistance	V_C =V_{IHC} $V_{I/O}$ =V_{SS} or V_{DD} $I_{I/O}$=100uA	5		180		Ω
			10		110		Ω
			15		90		Ω
△R_{ON}	Any two sets of conduction resistance differences	V_C =V_{IHC} $V_{I/O}$ =V_{SS} or V_{DD} $I_{I/O}$=100uA	5		15		Ω
			10		10		Ω
			15		5		Ω
I_{OFF}	Input/Output Leakage current	V_C= V_{ILC}, V_{IS} = 0 or VDD, V_{OS} = VDD or 0V	15		0.01	1	uA
I_{IZ}	Switch input leakage current	V_C= V_{IHC}, V_{IS} = 0 or VDD, V_{OS} =OPEN	15		0.01	1	uA
I_{DD}	Static current	V_{IN}=VDD or VSS	5		0.01	1	uA
			10		0.01	2	uA
			15		0.01	5	uA

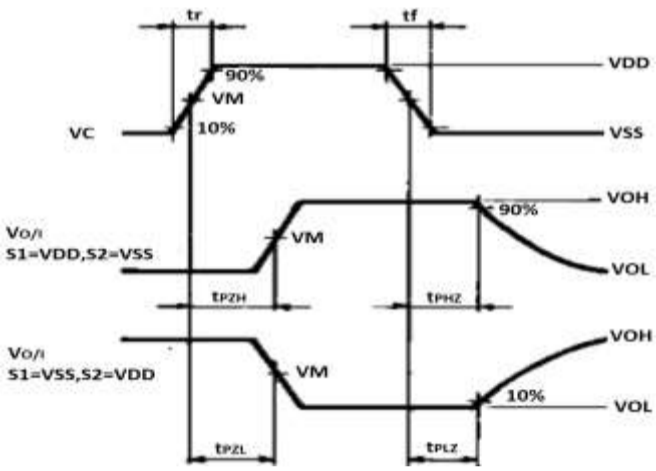
AC electrical characteristics: Ta=25℃ , R_L=1k, C_L=47pF, t_r=t_f≤20ns。

item	symbol	test condition	min	typ	max	unit
$V_{IN\_I/O}$ to $V_{O/I}$ phase Lag time	ϕI/O	VDD=5V		60		ns
		VDD=10V		20		ns
		VDD=15V		15		ns
delay time C_{IN} to Output=H to L	t_{PZH} t_{PZL}	VDD=5V		90		ns
		VDD=10V		70		ns
		VDD=15V		45		ns
delay time C_{IN} to Output=L to H	t_{PHZ} t_{PLZ}	VDD=5V		65		ns
		VDD=10V		35		ns
		VDD=15V		25		ns
CONTROL to Output Crosstalk ripple	V_{op-p}	VDD=5V		100		ns
		VDD=10V		200		ns
		VDD=15V		280		ns

test method

1、Test wiring diagram and waveform diagram





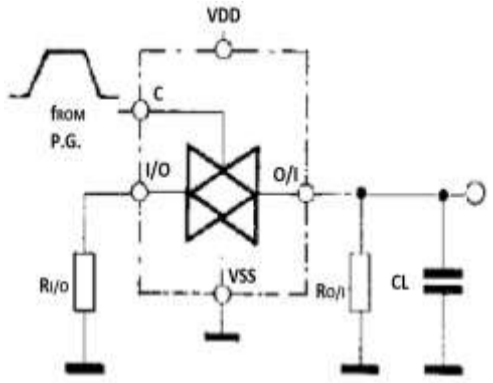
Note: 1. Corresponding test items in the table of AC electrical characteristics;

2. The CL capacitor is an external patch capacitor (0805), which is connected near the output pin and grounded near the chip VSS;

3. Input port level, f=1MHz, D=50% square wave, tr=tf ≤ 20ns;

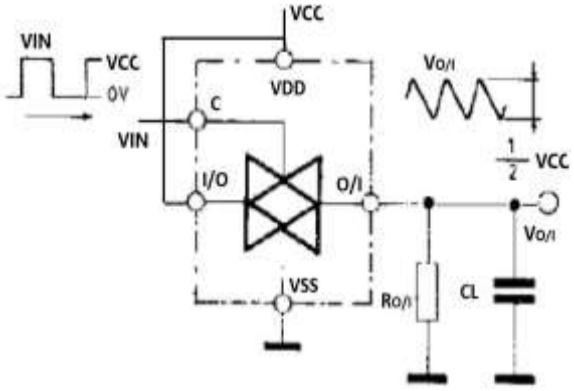
4. Test the output level.

CONTROL to Output（I/O O/I）
Crosstalk ripple



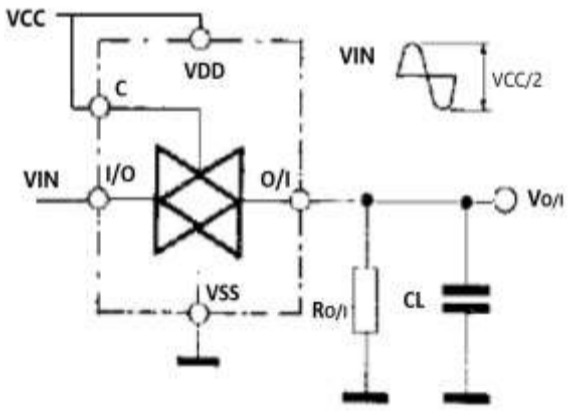
$R_{I/O}=R_{O/I}=600R$ CL=50Pf, f_c=1MHz，$t_r=t_f\leqslant 20ns$

CONTROL to Output（O/I） Crosstalk ripple



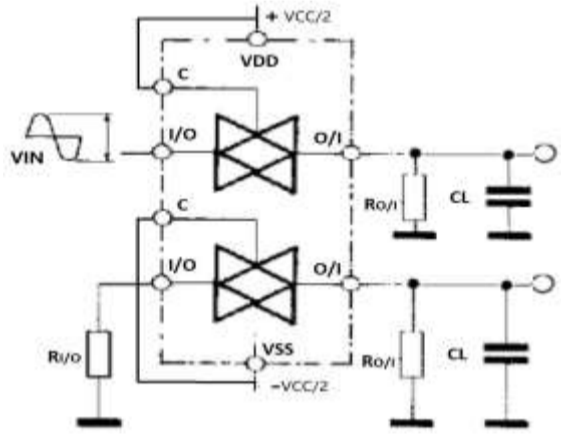
$R_{O/I}$=1K CL=15pF f_c=1MHz， $t_r=t_f\leqslant 20ns$

$VIN_{\_I/O}$ to $V_{O/I}$ Phase lag time



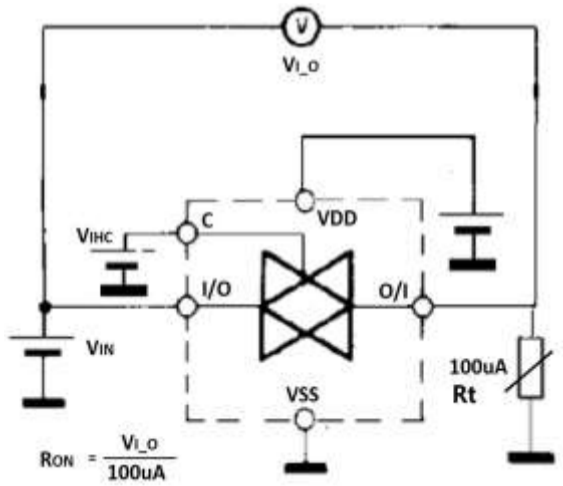
$R_{O/I}$=10K CL=50pF

Cross talk ripple between two switches

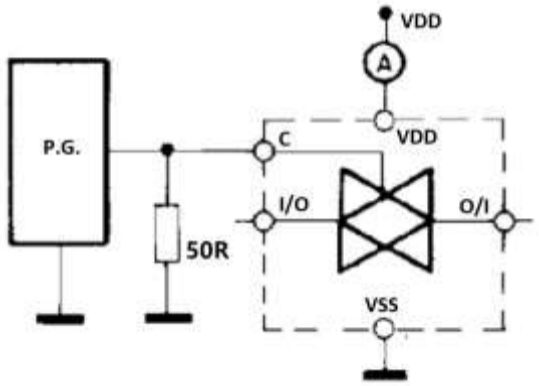


$R_{O/I}$=10K CL=50pF

RON Conduction resistance

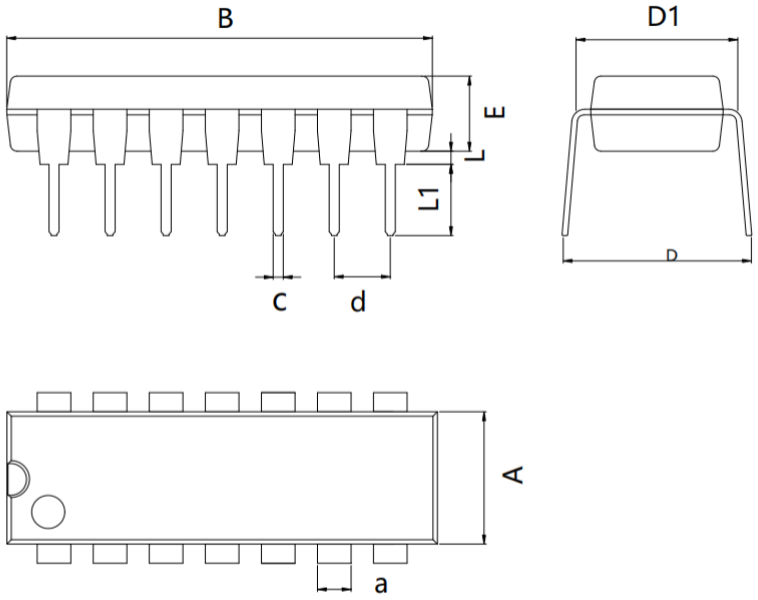


IDD current



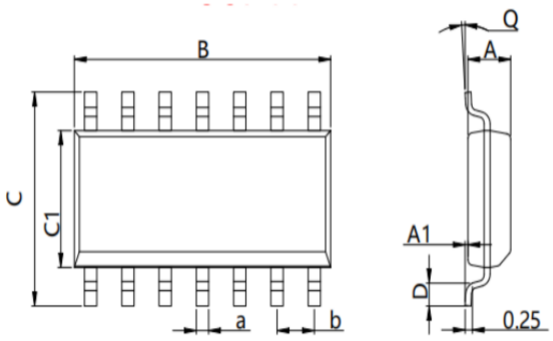
PACKAGE MECHANICAL DATA

DIP14



Dimensions In Millimeters(DIP14)										
Symbol:	A	B	D	D1	E	L	L1	a	C	d
Min:	6.10	18.94	8.40	7.42	3.10	0.50	3.00	1.50	0.40	2.54 BSC
Max:	6.68	19.56	9.00	7.82	3.55	0.70	3.60	1.55	0.50	

SOP14



Dimensions In Millimeters(SOP14)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	8.55	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	8.75	6.20	4.00	0.80	8°	0.45	