

Description:

CD4027 is a single monolithic chip integrated circuit containing two identical complementary-symmetry J-K master-slave flip-flops. Each flip-flop has provisions for individual J, K, Set, Reset, and Clock input signals. Buffered Q and \bar{Q} signals are provided as outputs. This input-output arrangement provides for compatible operation with the CD4013B dual D type flip-flop.

The CD4027 is useful in performing control register, and toggle functions. Logic levels present at the J and K inputs along with internal self-steering control the state of each flip-flop; changes in the flip-flop state are synchronous with the positive-going transition of the clock pulse. Set and reset functions are independent of the clock and are initiated when a high level signal is present at either the Set or Reset input.

Features

- Set - Reset capability
- Static flip-flop operation retains state indefinitely with clock level either "High" or "Low"
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 18V
- Maximum input current of 1 μ A at 18V and 25 $^{\circ}$ C
- 5V, 10V, and 15V parametric ratings

Absolute Maximum Ratings

Symbol	Parameter	MIN	MAX	Unit
V _{DD}	DC Supply Voltage Range (Voltage Referenced to VSS Terminals)	-0.5	20	V
V _I	Input Voltage Range, All Inputs	0.5	V _{DD} +0.5	V
P _D	Power Dissipation		500	mW
T _J	Junction Temperature		125	$^{\circ}$ C
T _{OP}	Operating Temperature	-40	85	$^{\circ}$ C

Absolute maximum ratings are those values beyond which the device could be permanently damaged. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions.

Pin Assignment:

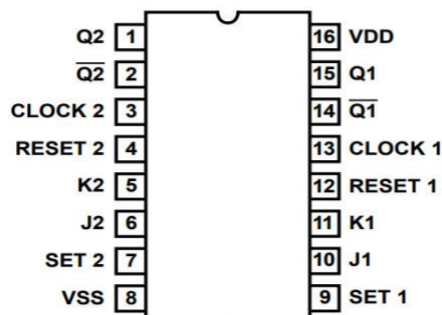


Figure 2.1 Top View

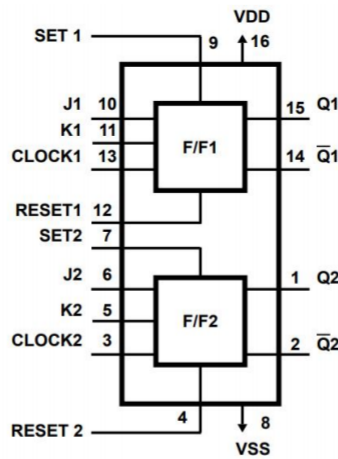


Figure 2.2 Functional Diagram

PIN No.	NAME	I/O	FUNCTION
1	Q2	O	Q Output for Channel 2
2	$\overline{Q2}$	O	Inverted Q Output for Channel 2
3	CLOCK2	I	Clock Input for Channel 2
4	RESET2	I	Reset Input for Channel 2
5	K2	I	K Input for Channel 2
6	J2	I	J Input for Channel 2
7	SET2	I	Set Input for Channel 2
8	VSS		Ground
9	SET1	I	Set Input for Channel 1
10	J1	I	J Input for Channel 1
11	K1	I	K Input for Channel 1
12	RESET1	I	Reset Input for Channel 1
13	CLOCK1	I	Clock Input for Channel 1
14	$\overline{Q1}$	O	Inverted Q Output for Channel 1
15	Q1	O	Q Output for Channel 1
16	VDD		Supply Voltage

Logic Diagram

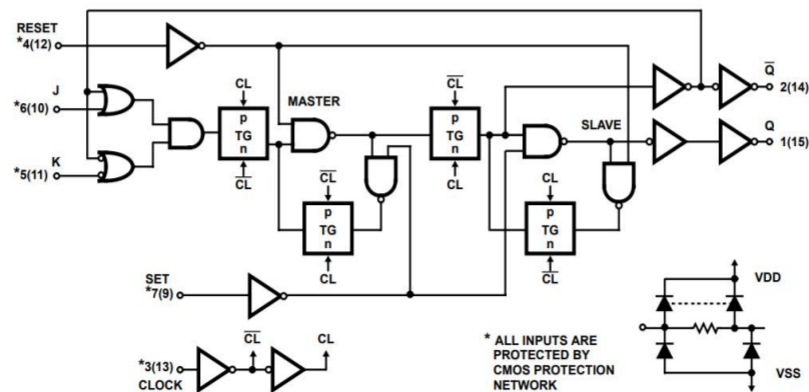


Figure 3.1: CD4027 Logic Diagram(One of Two Identical J-K Flip-Flops)

TruthTable

Clock	Present State				Next State		
	Input			Output	Output		
	J	K	S	R	Q	Q	\bar{Q}
↑	1	X	0	0	0	1	0
↑	X	0	0	0	1	1	0
↑	0	X	0	0	0	0	1
↑	X	1	0	0	1	0	1
↓	X	X	0	0	X	No Change	
X	X	X	1	0	X	1	0
X	X	X	0	1	X	0	1
X	X	X	1	1	X	1	1

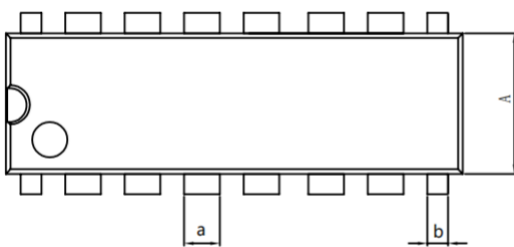
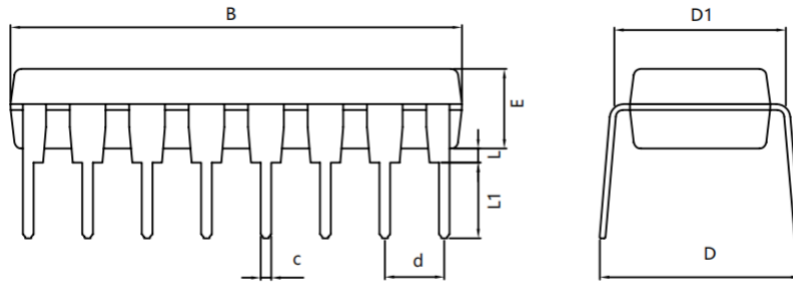
X = Don't Care, 1 ≡ High State, 0 ≡ Low State, ↑=positive-going transition, ↓=negative-going transition

Electrical Characteristics**DC Specifications**(T_a=25°C, voltages are referenced to VSS (ground=0V), unless otherwise specified)

Symbol	Parameter	Test Condition			MIN	TYP	MAX	Unit
		VO	VIN	VDD				
I _{DD}	Supply Current	--	0,5	5	--	0	1	uA
		--	0,10	10	--	0	1	uA
		--	0,18	18	--	0	1	uA
I _{OL}	Low Level Output Current	0.4	0,5	5	1	3	--	mA
		0.5	0,10	10	4	8	--	mA
		1.5	0,15	15	15	30	--	mA
I _{OH}	High Level Output Current	4.6	0,5	5	-0.5	-1.5	--	mA
		2.5	0,5	5	-3	-7	--	mA
		9.5	0,10	10	-2	-4	--	mA
		13.5	0,15	15	-7	-14	--	mA
V _{OL}	Low Level Output Voltage	--	0,5	5	--	0	0.05	V
		--	0,10	10	--	0	0.05	V
		--	0,15	15	--	0	0.05	V
V _{OH}	High Level Output Voltage	--	0,5	5	4.95	5	--	V
		--	0,10	10	9.95	10	--	V
		--	0,15	15	14.95	15	--	V
V _{IL}	Low Level Input Voltage	0.5,4.5	--	5	--	--	1.5	V
		1,9	--	10	--	--	3	V
		1.5,13.5	--	15	--	--	4	V
V _{IH}	High Level Input Voltage	0.5,4.5	--	5	3.5	--	--	V
		1,9	--	10	7	--	--	V
		1.5,13.5	--	15	11	--	--	V
I _{IN}	Input Leakage Current	--	0,18	18	--	0	±1	uA

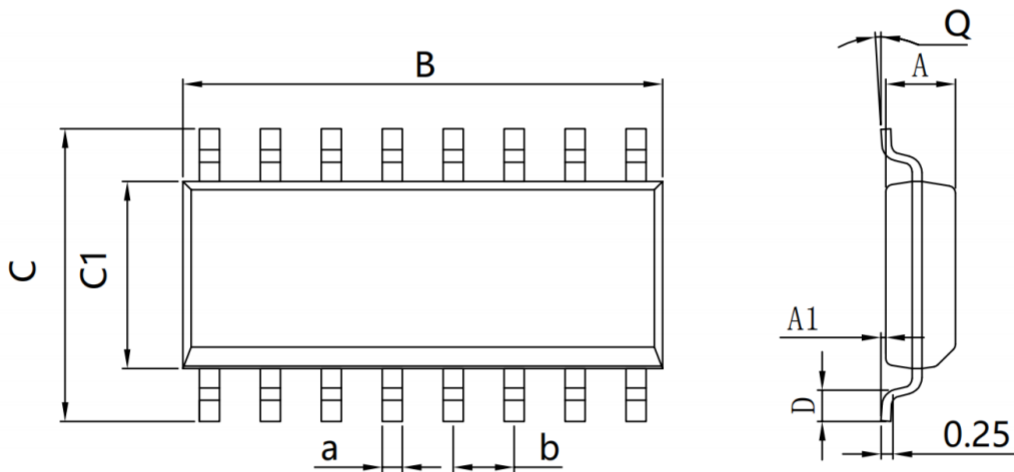
Pin Assignment:

DIP16



Dimensions In Millimeters					
Symbol :	Min :	Max :	Symbol :	Min :	Max :
A	6.100	6.680	L	0.500	0.800
B	18.940	19.560	a	1.524 TYP	
D	8.200	9.200	b	0.889 TYP	
D1	7.42	7.820	c	0.457 TYP	
E	3.100	3.550	d	2.540 TYP	
L	0.500	0.800			

SOP16



Dimensions In Millimeters					
Symbol :	Min :	Max :	Symbol :	Min :	Max :
A	1.225	1.570	D	0.400	0.950
A1	0.100	0.250	Q	0°	8°
B	9.800	10.00	a	0.420 TYP	
C	5.800	6.250	b	1.270 TYP	
C1	3.800	4.000			