CD 4049B (50B) 6-reverse (same as) phase buffer

summary

The CD 4049B and CD 4050B six-buffers are single-chip wide voltage range CMOS integrated circuits, so they have the advantages of low power consumption, anti-interference, and strong use flexibility. The device has the characteristic of realizing the logic level conversion with only one power supply voltage V DD. When these devices are used as a logic-level conversion, the input signal high-level V IH can exceed the supply voltage V DD. The device is used as a level conversion from CMOS to DTL and TTL, or as a CMOS current driver, and they can drive 2 DTL / TTL loads at V DD =5.0V.

1. Characteristics

Wide working voltage range: 3.0 ~ 15V;

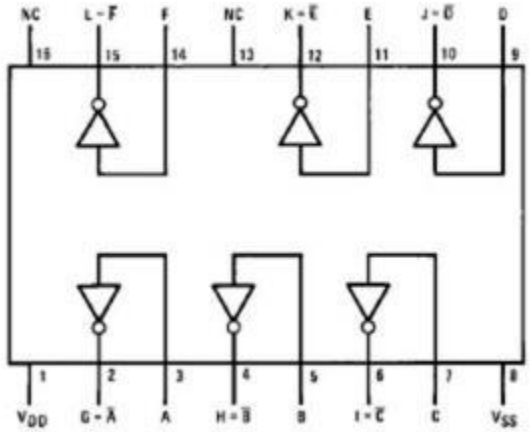
V DD =5.0V drives 2 TTL loads within the operating temperature range;

Make high current / current capacity;

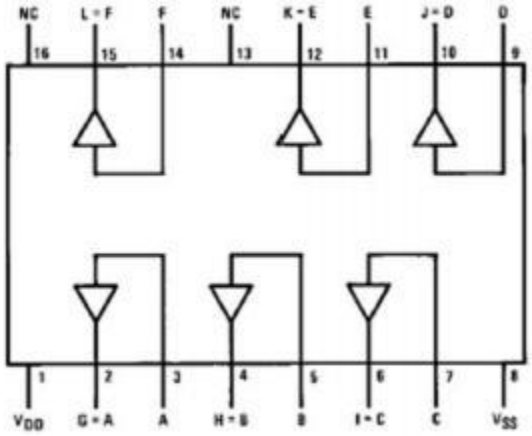
Make the dedicated input protection network allow an input voltage greater than V DD.

2. Top view

Order the CD 4049B

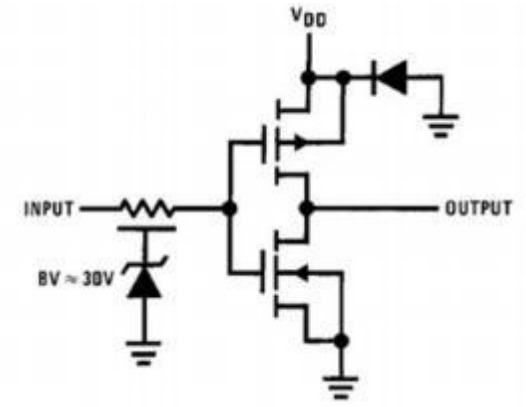


Order the CD 4050B

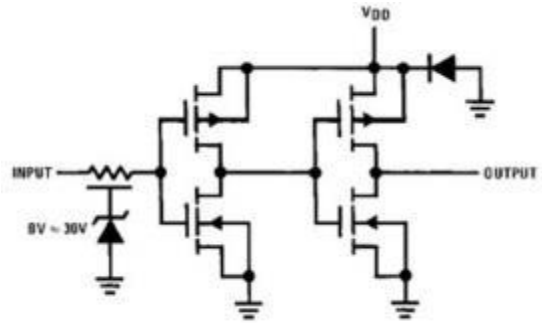


3. Schematic diagram

Order the CD 4049B 1 / 6 unit



Order the CD 4050B 1 / 6 unit



4. Limit parameters

parameter	symbol	condition	numeric value		unit
supply voltage	V DD		-0.5 ~ +18		V
input voltage	V IN		-0.5 ~ +18		V
Any output tube pin voltage	V OUT		-0.5 ~ VD D +0.5		V
Storage temperature range	t S		-65 ~ +150		℃
power dissipation	PD		DIP	700	mW
			S OP	500	
welding temperature	t L	10 Seconds	260		℃

5. Recommended working conditions

parameter	symbol	scope	unit
supply voltage	VDD	3~15	V
input voltage	VIN	0~15	V
Output voltage of any pin	VOUT	0~VDD	V
Operating temperature range is CD4049B, CD4050B	T A	- 10~70	℃

explanatory note:

1. "Absolute maximum value" refers to the near state, under which the safe use of the circuit cannot be guaranteed. The Recommended Working Scope and Electrical Parameters tables provide the actual operating status of the circuit.

2. Unless otherwise specified, V SS =0V

6. DC current parameters

(Note 3)

symbol	parameter	condition	-40℃		25℃			85℃		unit
			minimum	maximum	minimum	typical case	maximum	minimum	maximum	
ID D	Static drive current	VDD =5V VDD =10V VDD =15V		4 8 16		0.03 0.05 0.07	4 8 16		30 60 120	μA
V OL	Low-level output voltage	VIH =VDD，VIL=0V，｜IO｜<1μA VDD =5V VDD =10V VDD =15V		0.05 0.05 0.05		0 0 0	0.05 0.05 0.05		0.05 0.05 0.05	V
V OH	high level output voltage	VIH =VDD，VIL=0V，｜IO｜<1μA VDD =5V VDD =10V VDD =15V	4.95 9.95 14.95		4.95 9.95 14.95	5 10 15		4.95 9.95 14.95		V
V IL	Low-level input voltage (CD4050 only)	｜IO｜<1μA VDD =5V，VO =0.5V VDD =10V，VO =1.0V VDD =15V，VO =1.5V		1.5 3. 04.		2.25 4.5 6.75	1.5 3. 04.		1.5 3. 04.	V
V IL	Low-level input voltage (CD4049 only)	｜IO｜<1μA VDD =5V，VO =4.5V VDD =10V，VO =9V VDD =15V，VO =13.5V		0 1.0 2. 03.		1.5 2. 53.	0 1.0 2. 03.		0 1.0 2. 03.	V
VI H	High-level input voltage (CD4050 only)	｜IO｜<1μA VDD =5V，VO =4.5V VDD =10V，VO =9V VDD =15V，VO =13.5V	3.5 7.0 11.0	0	3.5 7.0 11.0	5 2.75 5.5 8.25	0	3.5 7.0 11.0	0	V
VI H	high level input voltage (CD4049 only)	｜IO｜<1μA VDD =5V，VO =0.5V VDD =10V，VO =1.0V VDD =15V，VO =1.5V	4.0 8.0 12.0		4.0 8.0 12.0	3.5 7.5 11.5		4.0 8.0 12.0		V
I OL	Low Level Output current (Note 4)	VDD =5V，VO =0.4V VDD =10V，VO =0.5V VDD =15V，VO =1.5V	0.61 1.5 4		0.51 1.3 3.4	1 2.8 6.8		0.42 1.1 2.8		mA

IO H	High-level output current (Note 4)	VDD =5V,VO =4.6V VDD =10V,VO =9.5V	-0.61 - 1.5		-0.51 - 1.3	- 1 -2.6		-0.42 - 1.1		mA
		VDD =15V,VO=13.5V	-4		-3.4	-6.8		-2.8		
IIN	input currenton	VDD =15V,VIN =0V VDD =15V,VIN =15V		-0.30 .3		-0.30 .3	- 10^{-5} 10^{-5}		- 1.01 .0	μA

explanatory note:

3. Unless otherwise specified, V SS =0V

4. These are the limits of the output current. The continuous output current is rated at 12mA. When IOL and IO H exceed a test output, the output current is not allowed to exceed this value.

7. AC current parameters

(Note 5)

Order the CD 4049

T A = 25℃, R L = 200K Ω, C L =50pF, tr=t f =20ns, unless any other note:

symbol	parameter	condition	least value	representative value	crest value	unit
t PHL	Transmission delay time (high level to low level)	VDD = 5V VDD = 10V VDD = 15V		30 20 15	65 40 30	nS
t PLH	Transmission delay time (low to high level)	VDD = 5V VDD = 10V VDD = 15V		45 25 20	85 45 35	nS
tT HL	Transition time (high level to low level)	VDD = 5V VDD = 10V VDD = 15V		30 20 15	60 40 30	nS
C IN	input capacitance	Enter any value		15	22.5	p F

Note: 5. The AC current parameters depend on the relevant DC test.

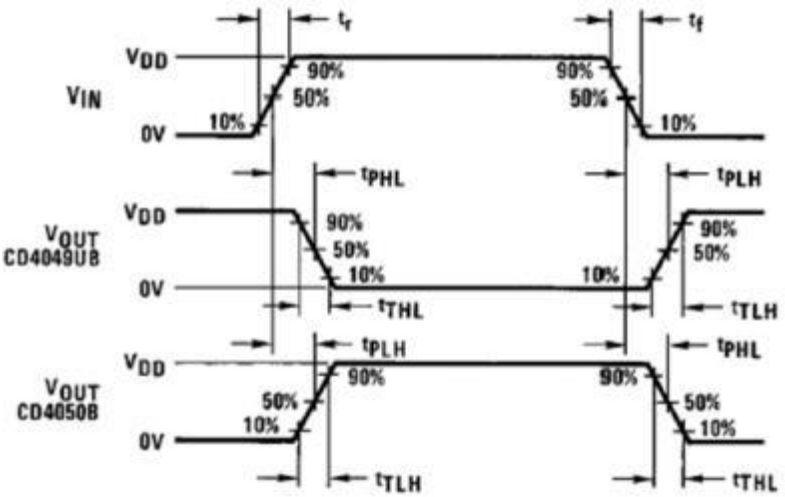
Order the CD 4050

T A = 25℃, R L = 200K Ω, C L =50pF, tr=tf=20ns, unless any other note:

symbol	parameter	condition	least value	representative value	crest value	unit
t PHL	Transmission delay time (high level to low level)	VDD = 5V VDD = 10V VDD = 15V		60 25 20	110 55 30	nS
t PLH	Transmission delay time (low to high level)	VDD = 5V VDD = 10V VDD = 15V		60 30 25	120 55 45	nS
tT HL	Transition time (high level to low level)	VDD = 5V VDD = 10V VDD = 15V		30 20 15	60 40 30	nS
C IN	input capacitance	Enter any value		5	7.5	p F

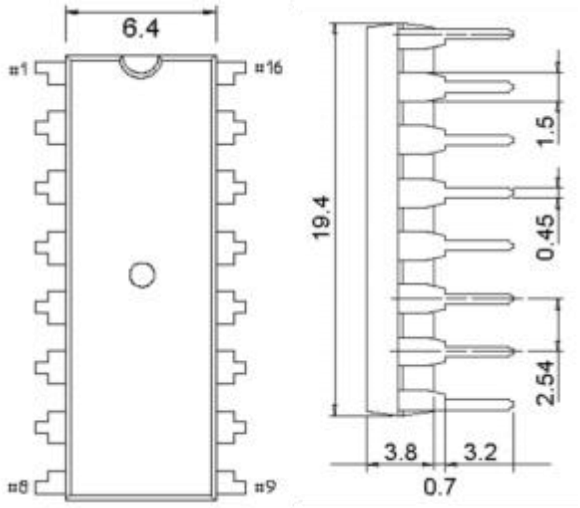
Note: 6. The AC current parameters depend on the relevant DC test.

8. The Waveform chart



9. Package size diagram

Make the DIP 16 package dimension diagram



Make the SOP 16 package dimension diagram