8-channel multiplexer

Description

CD4051B is a single 8-channel multiplexer designed using advanced CMOS technology. It is an a nalog switch with a single pole eight throw configuration. It has three binary channel control inputs (A, B , C) and one enable input INH. Binary input signal, controlling one of the 8 channels to open and the re maining channels to close.

Feature

-Low input current：I_{IN}≤1uA,@V_{IN}=V_{DD}-V_{SS}=15V,Ta=25℃

-Low static power consumption：I_{DD}=0.2uA(TYP)@V_{DD}-V_{SS}=15V,Ta=25℃

-Low pass resistance: 60 Ω (typical) @ VDD-VS=VDD-VEE=15V, Ta=25 ℃

-Channel leakage current: ± 100nA (typical) @ VDD-VEE=15V

-Wide working voltage VDD-VSS range: 3V~15V

-Switching from break to pass eliminates channel overlap and opens

-Analog switch with single pole eight throw configuration

-Packaging form: DIP16, SOP16

Application

-Analog and digital multiplexing and demultiplexing

-signal gating

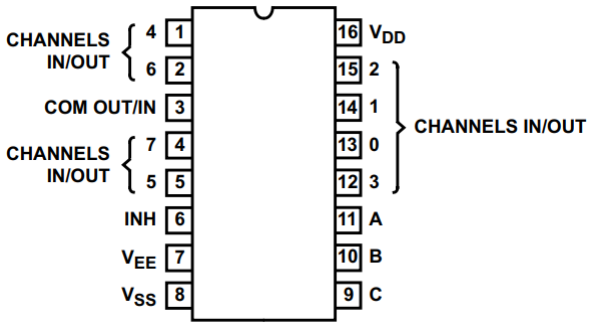
-Logic level conversion of digital addressing signals

-Other application areas

Absolute Maximum Ratings

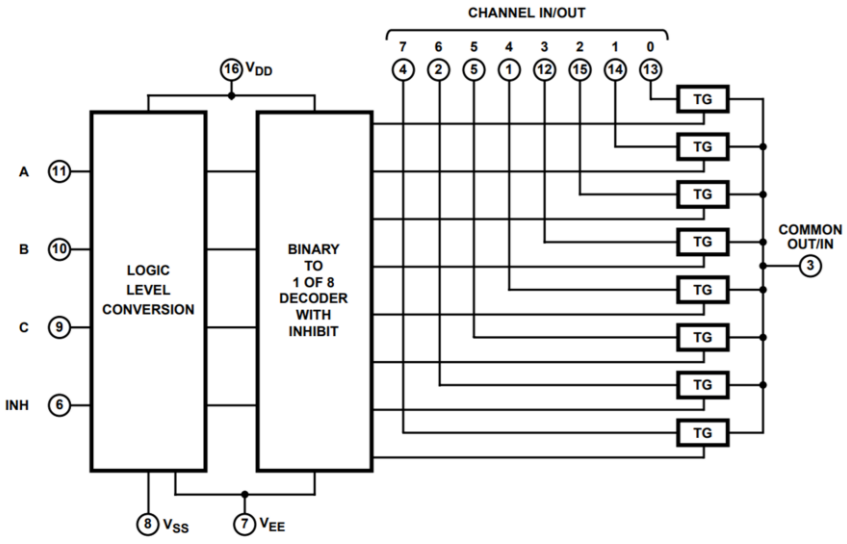
parameter	symbol	MAX	unit
DC power supply voltage	V_{DD}-V_{SS}	-0.5～18	V
Simulated power supply voltage	V_{DD}-V_{EE}	18	V
input voltage	V_{IN}	-0.5+V_{SS}～V_{DD}+0.5V	V
consumption	P_D	500	mW
operation temperature	T_A	-40~85	℃
storage temperature	T_S	-65-150	℃
welding temperature	T_W	260,10s	℃

Pin Definition



PIN	SYMBOL	FUNCTION	PIN	SYMBOL	FUNCTION
1	4	Channel 4	16	V_{DD}	Positive power input
2	6	Channel 6	15	2	Channel 2
3	COM OUT/IN	Common out/in	14	1	Channel 1
4	7	Channel 7	13	0	Channel 0
5	5	Channel 5	12	3	Channel 3
6	INH	enable control	11	A	Channel select A
7	V_{EE}	Negative power input	10	B	Channel select B
8	Vss	Ground	9	C	Channel select C

logic diagram



truth table

INPUTS				OUTPUTS
INH	C	B	A	“ ON ” CHANNEL(S)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1		╳	╳	None

╳: Arbitrary value

Recommended Operating Conditions

parameter	symbol	MIN	TYP	MAX	UNIT
DC power supply voltage	$V_{DD}-V_{SS}$	3		15	V
Control input voltage	V_{IS}	0		$V_{DD}-V_{SS}$	V
Simulated power supply voltage	$V_{DD}-V_{EE}$	0		15	V
Analog input/output voltage	V_{IN}、V_{OUT}	0		$V_{DD}-V_{EE}$	V
operation temperature	T_A	-40		85	℃

electrical characteristic

DC electrical characteristics: ($V_{IS}=V_{IN}-V_{SS}$,$V_{EE}=V_{SS}$,RL = 3kΩ, T_A=25℃ Unless otherwise specified)

symbol	parameter	Test conditions		VDD（V）	MIN	TYP	MAX	UNIT
V_{IH}	High level effective input voltage	$V_{IH}=V_{DD}$ through 1k	$V_{EE}=V_{SS}$, RL=1kΩ to V_{SS}, I_{IS}<2uA on all OFF Channels	5	3.5			V
				10	7			V
				15	11			V
V_{IL}	Low level effective input voltage	$V_{IL}=V_{DD}$ through 1k		5			1.5	V
				10			3	V
				15			4	V
R_{ON}	Conduction resistance	$0 \leqslant V_{IS} \leqslant V_{DD}$		5		150		Ω
				10		80		
				15		60		
$\triangle R_{ON}$	The difference in conducting resistance between adjacent channels			5		15		Ω
				10		10		
				15		5		
I_{OFF}	Leakage current	Input/output channel closed,INH=V_{∞}		18			±100	nA
I_{IN}	Input Current	$V_{IN}=V_{DD}$ or V_{SS}		18		0.01	±0.1	uA
I_{DD}	quiescent current	$V_{IN}=V_{DD}$ or V_{SS}		5		0.01	5	uA
				10		0.01	10	uA
				15		0.01	20	uA
C_{IN}	Input capacitance	Any input terminal				5	7.5	pF
C_{IS}	Channel input capacitance					5		pF
C_{OS}	output capacitance					9		pF
C_{IOS}	Conducting capacitance					0.2		pF

AC electrical characteristics: ($V_{SS}=V_{EE}$,Ta=25℃， tr=tf=20ns,tpd containt t_{PHL}、t_{PLH}， See testing method, unless otherwise specified)

parameter	symbol	Test conditions	VDD	MIN	TYP	MAX	UNIT
Transmission delay time Signal Input to Output	tpd	$V_{IS}=V_{DD}$, RL=200k, CL=50pF	5		15		ns
			10		10		ns
			15		7		ns
Transmission delay time Address-to-Signal OUT (Channels ON or OFF)	tpd	CL=50pF, RL=10k	5		100		ns
			10		80		ns
			15		50		ns

AC electrical characteristics: (Continues,)

parameter	symbol	Test conditions	VDD	MIN	TYP	MAX	UNIT
Transmission delay time Inhibit-to-Signal OUT (Channel Turning ON)	tpd	C_L=50pF, R_L=1k	5		100		ns
			10		50		ns
			15		30		ns
Transmission delay time Inhibit-to-Signal OUT (Channel Turning OFF)	tpd	C_L=50pF, R_L=10k	5		100		ns
			10		50		ns
			15		30		ns

test method

1、test chart

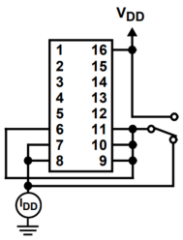


Fig.1 Static current

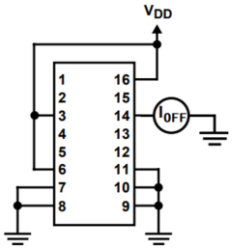


Fig.2 Close leakage current of adjacent channels

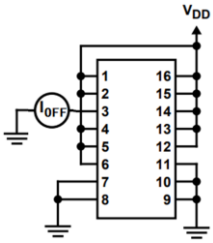


Fig.3 All channels closed l eakage current

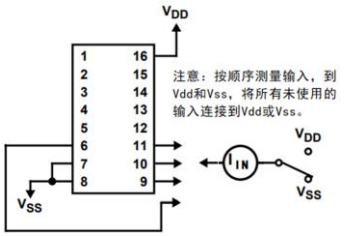


Fig.4 Input curr ent

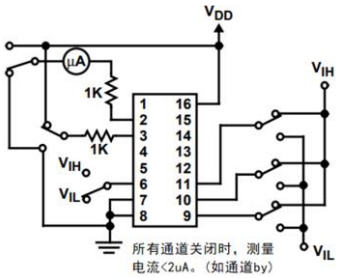


Fig.5 Input logic level vol tage

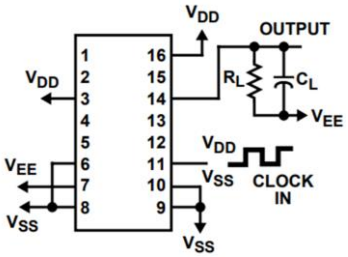


Fig.6 Propagation Delay - Channel Contro l Input to Switch Output

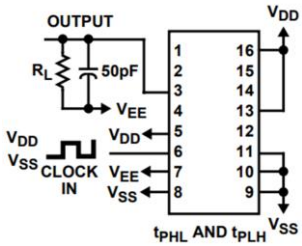


Fig.7 Propagation Delay - Enable Inp ut to Switch Output

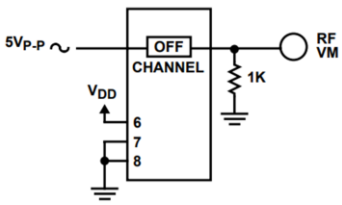


Fig.8 All channels off signal crosstalk

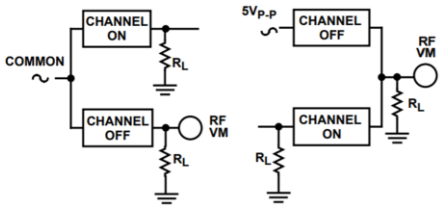
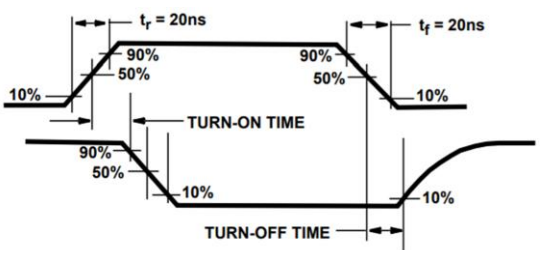
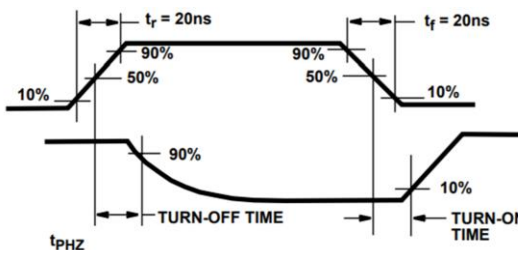


Fig.9 Signal crosstalk on the same channel

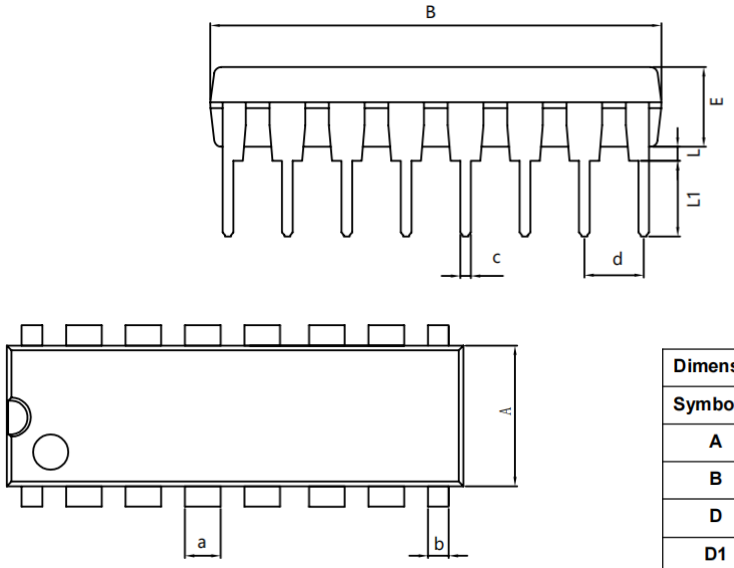
2. Diagram of waveform measurement





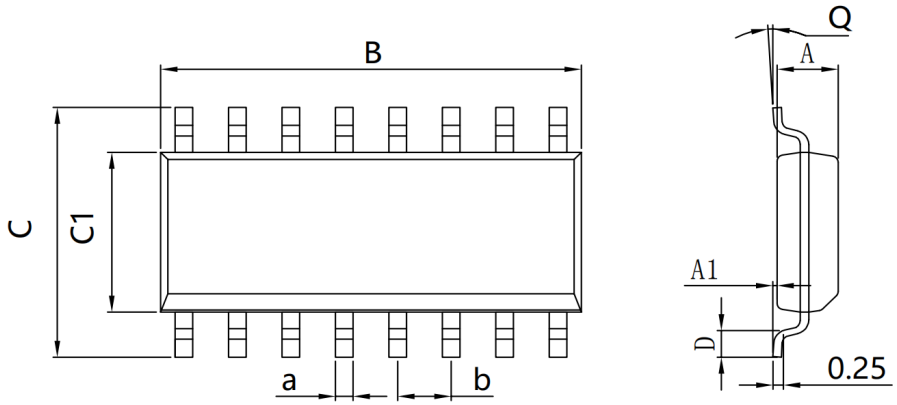
Pin Assignment：

DIP16



Dimensions In Millimeters					
Symbol：	Min：	Max：	Symbol：	Min：	Max：
A	6.100	6.680	L	0.500	0.800
B	18.940	19.560	a	1.524 TYP	
D	8.200	9.200	b	0.889 TYP	
D1	7.42	7.820	c	0.457 TYP	
E	3.100	3.550	d	2.540 TYP	
L	0.500	0.800			

SOP16



Dimensions In Millimeters					
Symbol：	Min：	Max：	Symbol：	Min：	Max：
A	1.225	1.570	D	0.400	0.950
A1	0.100	0.250	Q	0°	8°
B	9.800	10.00	a	0.420 TYP	
C	5.800	6.250	b	1.270 TYP	
C1	3.800	4.000			