Description：

CD4053 is a 3-channel dual channel analog multiplexer designed with advanced CMOS technology. It is an analog switch with a single pole double throw configuration. It has three independent channel control inputs A, B, C and one enable input INH. Channel control input signals A, B, and C respectively control one of the two channels of the 3-channel switch to turn on and the other channel to turn off.

Features：

-Low input current: IIN ≤ 1uA, @ VIN=VDD-VSS=15V, Ta=25
-Low static power consumption: IDD=0.2uA (typical) @ VDD-VSS=15V, Ta=25 ℃
-Low pass resistance: 90 ohms (typical) @ VDD-VSS=VDD-VEE=15V, Ta=25 ℃

-Wide operating voltage VDD-VSS range: 3V~15V
-Switching between first disconnect and then connect eliminates channel overlap and opens
-Simulation switch with single pole double throw configuration
-Packaging form: DIP16, SOP16

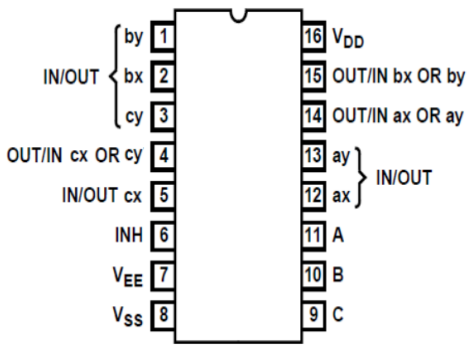
Application:

-Analog and digital multiplexing and demultiplexing
-Signal gating
-Logic level conversion of digital addressing signals
-Other application areas

Pin Assignment：

pin no.	Symbol	Definition	pin no.	Symbol	Definition
1	IN/OUT by	by Channel	16	V_{DD}	VDD
2	IN/OUT bx	bx Channel	15	OUT/IN bx OR by	B channel common end
3	IN/OUT cy	cy Channel	14	OUT/IN ax OR ay	A channel common end
4	OUT/IN cx OR cy	C channel common end	13	IN/OUT ay	ay Channel
5	IN/OUT cx	cx Channel	12	IN/OUT ax	ax Channel
6	INH	enable control	11	A	Channel control input A
7	V_{EE}	Simulated switch negative power supply	10	B	Channel control input B
8	V_{SS}	GND	9	C	Channel control input C

DIP16/SOP16

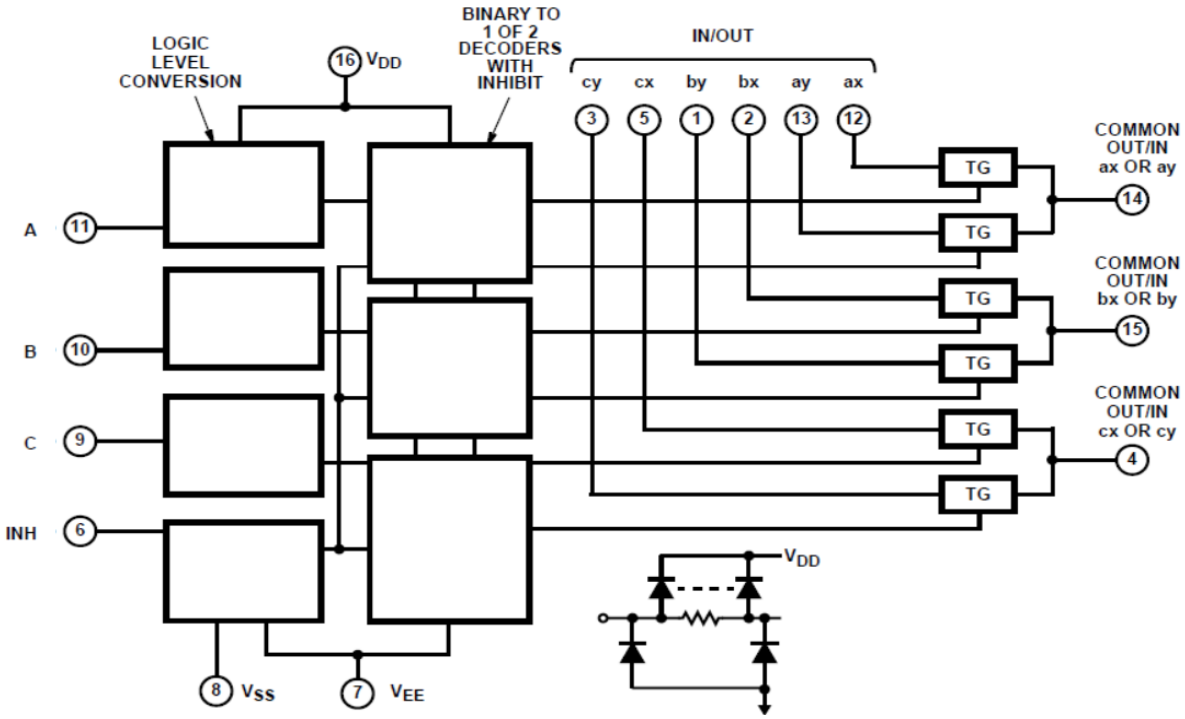


Absolute Maximum Ratings：

parameter	Symbol	Max	Unit
working voltage	V_{CC}	-0.5-18	V
Input/output voltage	V_{IN}、$V_{I/O}$	-0.5+VSS-VDD+0.5V	V
Input current	I_I	±10	mA
Dissipated power	P_D	500	mW
working temperature	T_A	0-70	℃
Storage temperature	T_S	-65-150	℃
Pin welding temperature	T_W	260,10s	℃

Note: Limit parameters refer to the limit values that cannot be exceeded under any conditions. If the limit value is excee ded, it may cause physical damage such as product degradation; At the same time, it cannot be guaranteed that the chi p can function properly when approaching the limit parameters.

logic diagram



Truth table

INPUTS		OUTPUTS
INH	A or B or C	ONCHANNEL
0	0	ax or bx or cx
0	1	ay or by or cy
1	×	None

×:Arbitrary value

Recommended operating conditions

parameter	Symbol	Min	typ	Max	unit
DC power supply voltage	$V_{DD}-V_{SS}$	3		15	V
Control input voltage	V_{IS}	0		$V_{DD}-V_{SS}$	V
Simulate power supply voltage	$V_{DD}-V_{EE}$	0		15	V
Simulate input and output voltage	V_{IN}、V_{OUT}	0		$V_{DD}-V_{EE}$	V
working temperature	T_A	0		60	℃

electrical characteristic

DC electrical characteristics:(Ta=25)

symbol	parameter	Test conditions		VDD（V）	Min	typ	Max	unit
V_{IH}	High level effective input voltage	$V_{IH}=V_{DD}$ through 1k	$V_{EE}=V_{SS}$, RL=1kΩ to V_{SS}, I_{IS}<2uA on all OFF Channels	5	3.5			V
				10	7			V
				15	11			V
V_{IL}	Low level effective input voltage	$V_{IL}=V_{DD}$ through 1k		5			1.5	V
				10			3	V
				15			4	
R_{ON}	On resistance	$0 \leqslant V_{IS} \leqslant V_{DD}$		5		180		Ω
				10		115		
				15		90		
$\triangle R_{ON}$	Adjacent channels conducting electricity Resistance difference			5		15		Ω
				10		10		
				15		5		
I_{OFF}	Leakage current	Input/output channel closed, INH=V_{DD}		18			±100	nA
I_{IN}	Input Current	$V_{IN}=V_{DD}$ or V_{SS}		18		0.01	±0.1	uA
I_{DD}	quiescent current	$V_{IN}=V_{DD}$ or V_{SS}		5		0.01	5	uA
				10		0.01	10	uA
				15		0.01	20	uA
C_{IN}	Input capacitance	Any input terminal				5	7.5	pF
C_{IS}	Channel input capacitor					5		pF
C_{OS}	output capacitance					9		pF
C_{IOS}	Conductive capacitor					0.2		pF

AC electrical characteristics: (VSS=VEE, Ta=25 , tr=tf=20ns, tpd includes tPHL, tPLH, see test method, unless otherwise specified)

parameter	symbol	Test conditions	VDD	Min	typ	Max	unit
Transmission delay time Signal Input to Output	tpd	$V_{IS}=V_{DD}$, RL=200k, CL=50pF	5		15		ns
			10		10		ns
			15		7		ns
Transmission delay time Address-to-Signal OUT (Channels ON or OFF)	tpd	CL=50pF, RL=10k	5		100		ns
			10		80		ns
			15		50		ns

AC electrical characteristics:(Continues,)

Transmission delay time Inhibit-to-Signal OUT (Channel Turning ON)	tpd	C_L=50pF, R_L=1k	5		100		ns
			10		50		ns
			15		30		ns
Transmission delay time Inhibit-to-Signal OUT (Channel Turning OFF)	tpd	C_L=50pF, R_L=10k	5		100		ns
			10		50		ns
			15		30		ns

Test Method 1:

test chart

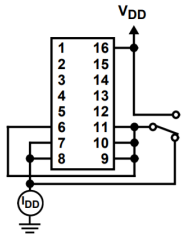


Fig.1 Static current

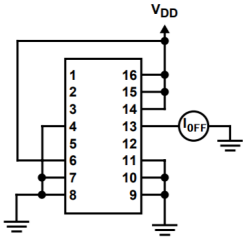


Fig.2 Close leakage current of adjacent channels

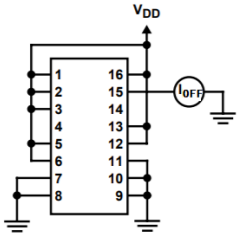


Fig.3 All channels closed leakage current

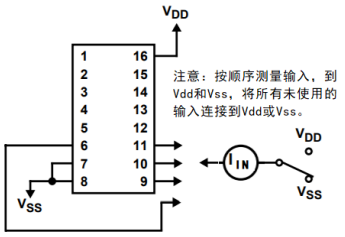


Fig.4 Input current

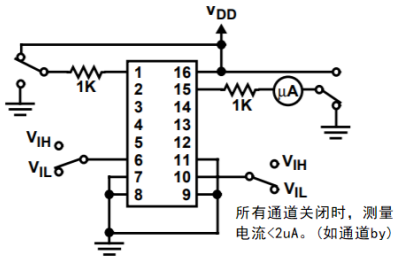


Fig.5 Input Logic Level Voltage

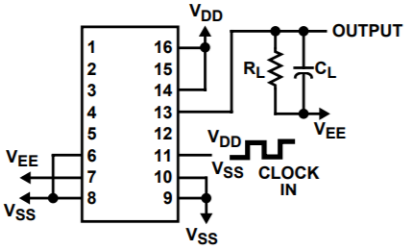


Fig.6 Propagation Delay - Channel Control Input to Switch Output

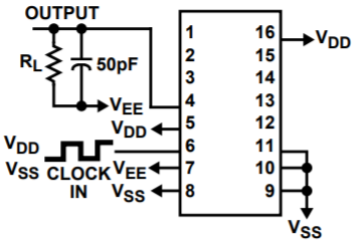


Fig.7 Propagation Delay - Enable Input to Switch Output

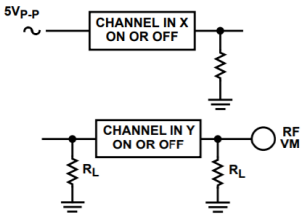


Fig.8 Signal crosstalk between adjacent channels

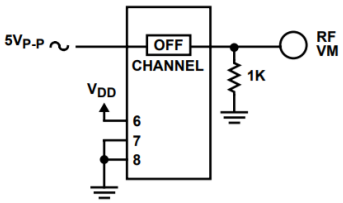


Fig.9 All channels are closed for signal crosstalk

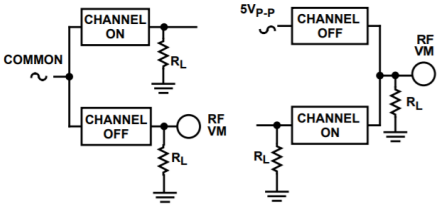
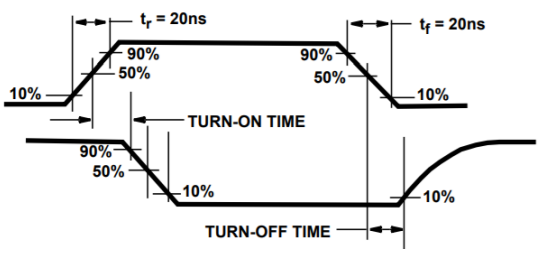
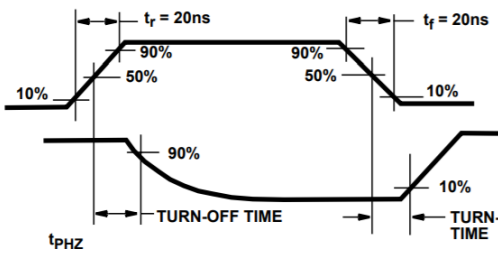


Fig.10 Interference of the same channel signal

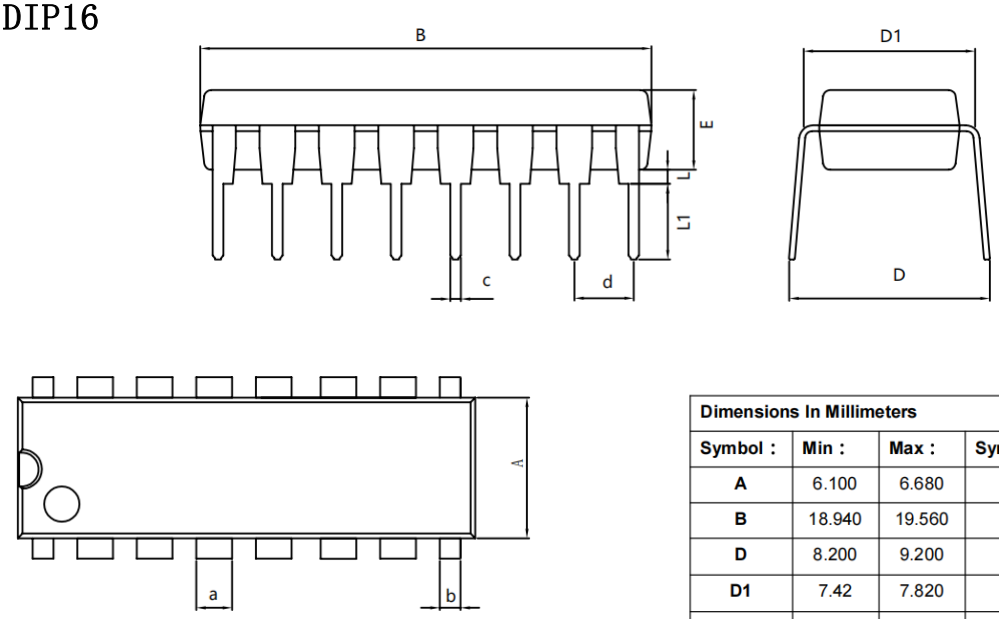
2、波形测量示意图





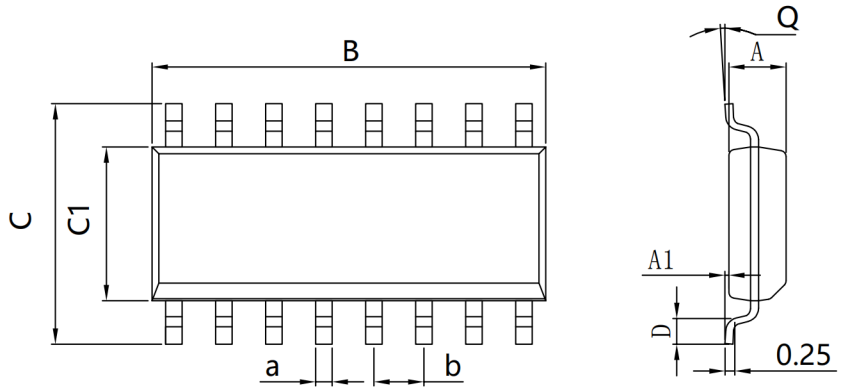
PACKAGE MECHANICAL DATA

DIP16



Dimensions In Millimeters					
Symbol :	Min :	Max :	Symbol :	Min :	Max :
A	6.100	6.680	L	0.500	0.800
B	18.940	19.560	a	1.524 TYP	
D	8.200	9.200	b	0.889 TYP	
D1	7.42	7.820	c	0.457 TYP	
E	3.100	3.550	d	2.540 TYP	
L	0.500	0.800			

SOP16



Dimensions In Millimeters					
Symbol :	Min :	Max :	Symbol :	Min :	Max :
A	1.225	1.570	D	0.400	0.950
A1	0.100	0.250	Q	0°	8°
B	9.800	10.00	a	0.420 TYP	
C	5.800	6.250	b	1.270 TYP	
C1	3.800	4.000			