Description：

CD4094 is a series in/parallel out high-speed converter with output latch and tri state control, which has the advantages of simple use, low power consumption, strong driving capability, and flexible control. The pin definition of CD4094 is shown in the figure. Among them, pin (1) is the latch terminal, pin (2) is the serial data input terminal, and pin (3) is the serial clock terminal. (1) When the pin is at a high level, the 8-bit parallel output ports Q1-Q8 vary with the serial input on the rising edge of the clock; (1) When the foot is at a low level, the output is locked. The use of latch terminals enables convenient chip selection and cascaded output control. (15) The pin is the parallel output state control terminal, and when pin (15) is at a low level, the parallel output terminal is in a high impedance state. When using CD4094 as a display output, it can make the display digits blink. (9) Pin QS and (10) pin Q'S are serial data output terminals used for cascading. The QS end starts outputting at the rising edge of the 9th serial clock, and the Q'S end starts outputting at the falling edge of the 9th serial clock. CD4094 provides DIP16 and SOP16 packaging forms.

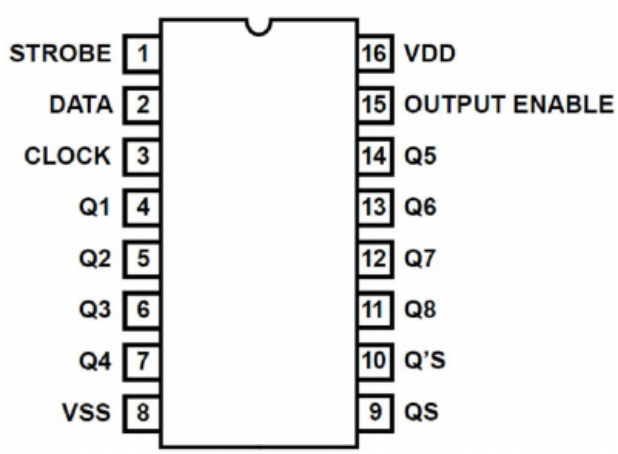
Features：

-Wide working power supply+3V~15V
-High anti-interference performance of 0.45 VDD (typ.)
-Low power consumption, TTL compatible,
Can drive two 74L or one 74LS channels
-Tri state output
-Full static operation (15V)

Application:

-Serial parallel data conversion
-Remote control holds register
-Dual level transfer, hold, and bus application

Pin Assignment：

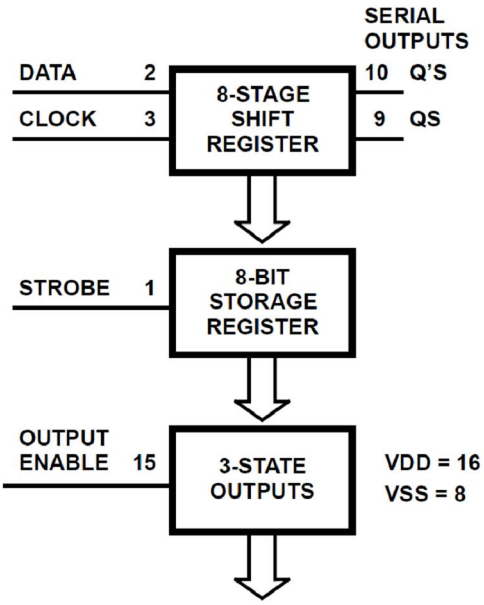


Absolute Maximum Ratings：

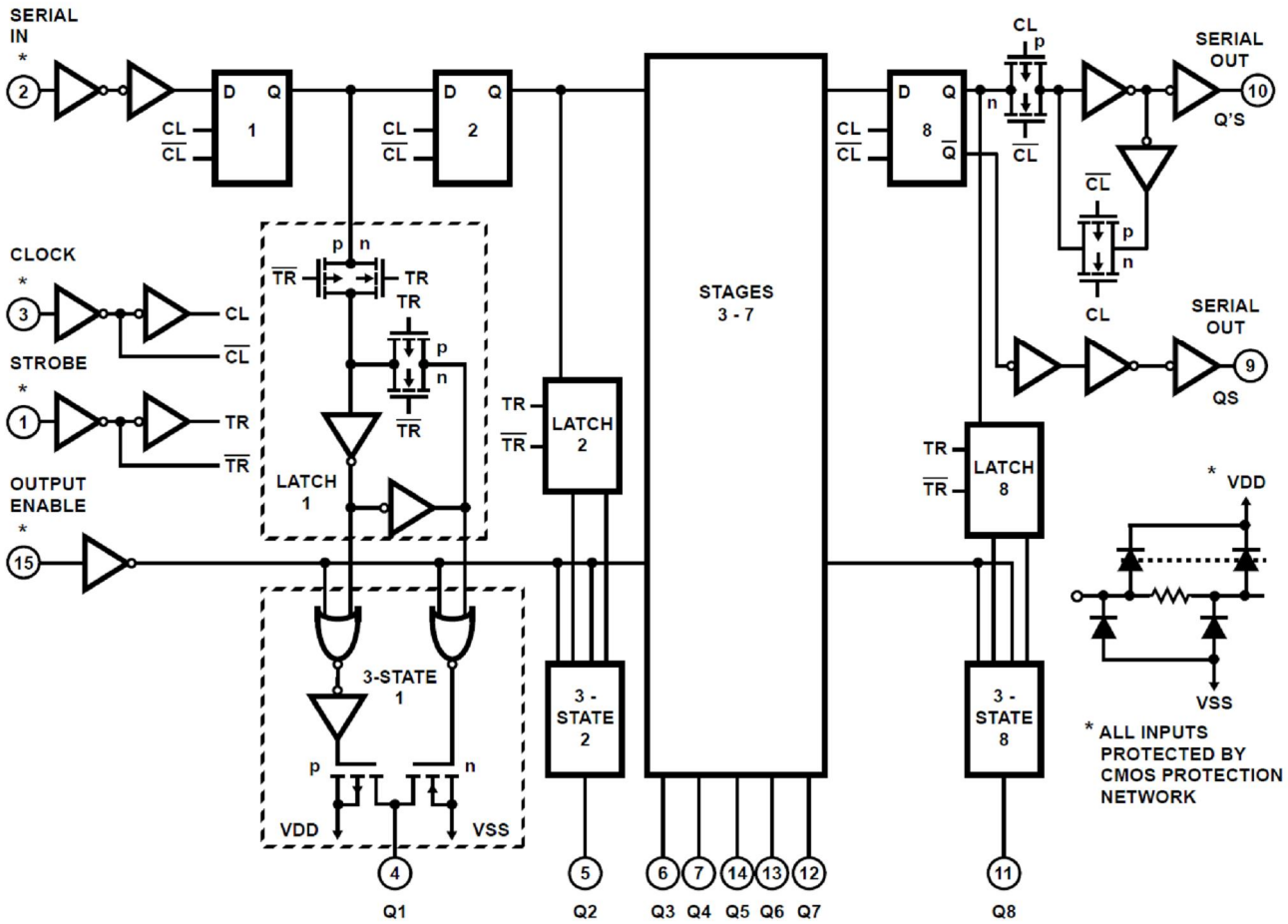
parameter	Symbol	Max	Unit
working voltage	V_{CC}	-0.5-18	V
Input/output voltage	V_{IN}、$V_{I/O}$	-0.5+VSS-VDD+0.5V	V
Input current	I_I	±10	mA
Dissipated power	P_D	500	mW
working temperature	T_A	0-70	℃
Storage temperature	T_S	-65-150	℃
Pin welding temperature	T_W	260,10s	℃

Note: Limit parameters refer to the limit values that cannot be exceeded under any conditions. If the limit value is exceeded, it may cause physical damage such as product degradation; At the same time, it cannot be guaranteed that the chip can function properly when approaching the limit parameters.

Functional Block Diagram



Logic diagram (overall)



Truth table

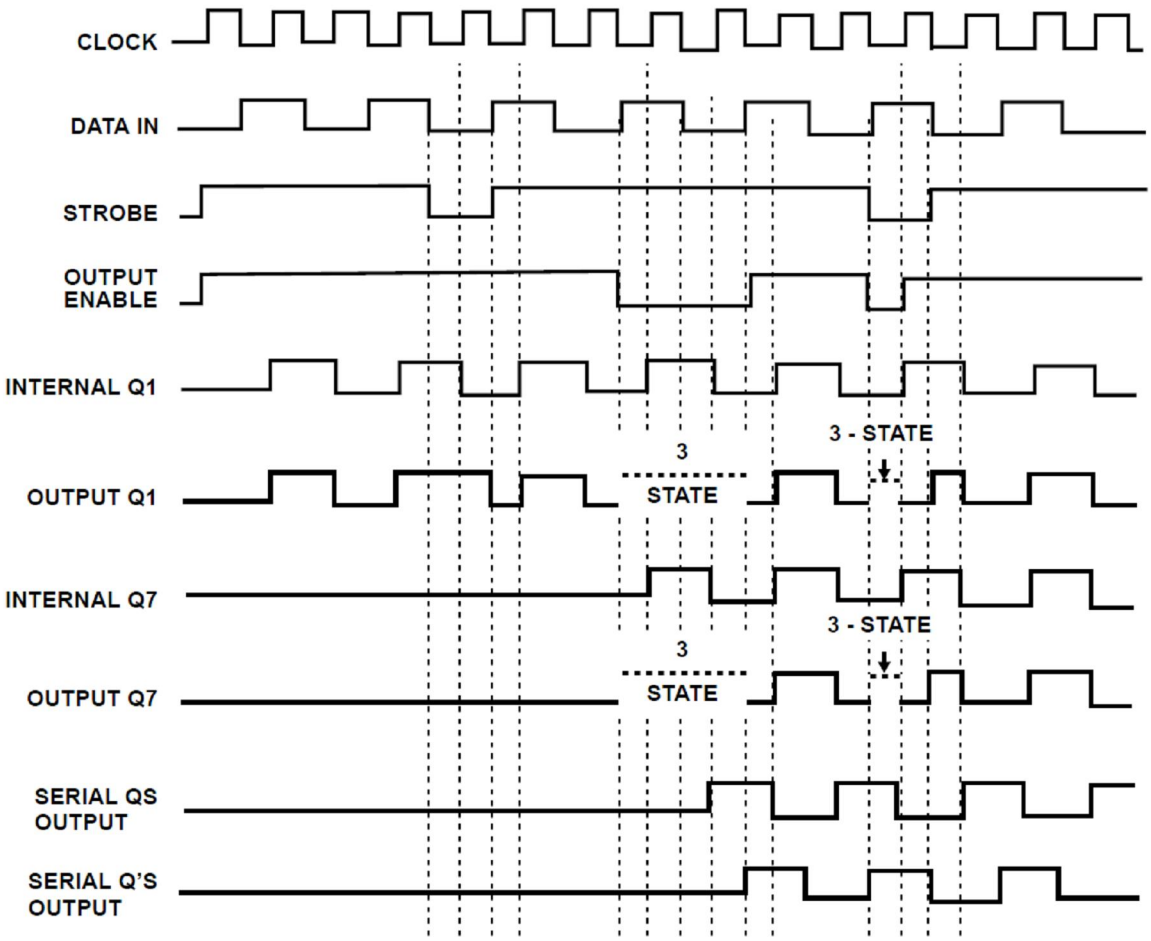
TRUTH TABLE

CL△	OUTPUT ENABLE	STROBE	DATA	PARALLEL OUTPUTS		SERIAL OUTPUTS	
				Q1	QN	QS*	Q'S
↑	0	X	X	OC	OC	Q7	NC
↓	0	X	X	OC	OC	NC	Q7
↑	1	0	X	NC	NC	Q7	NC
↑	1	1	0	0	QN-1	Q7	NC
↑	1	1	1	1	QN-1	Q7	NC
↓	1	1	1	NC	NC	NC	Q7

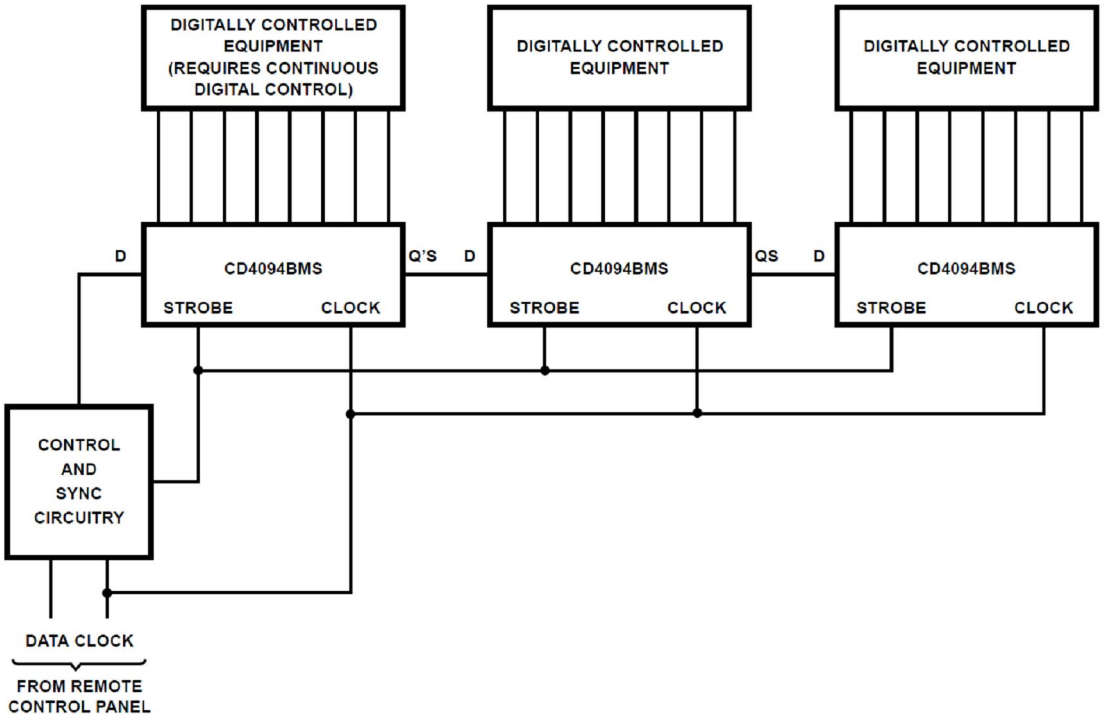
△ = Level Change
X = Don't Care
NC = No Change
OC = Open Circuit
Logic 1 = High
Logic 0 = Low

* At the positive clock edge information in the 7th shift register stage is transferred to the 8th register stage and the QS output

Timing diagram



Multi level control storage application



DC Electrical Characteristics (Note 2)

symbol	parameter	Test conditions	temperature	+25℃		unit
			Min	**Typ**	**Max**	
I_{DD}	Quiescent Device Current	V_{DD} = 5V V_{DD} =10V V_{DD} = 15V			5 10 20	υA
V_{OL}	LOW Level Output Voltage	|I_O| < 1.0 υA V_{DD} = 5V V_{DD} =10V V_{DD} = 15V 10V		0 0 0	0.05 0.05 0.05	V
V_{OH}	HIGH Level Output Voltage	|I_O| < 1.0 υA V_{DD} = 5V V_{DD} =10V V_{DD} = 15V V_{DD}	4.95 9.95 14.95	5 10 15		V
V_{IL}	LOW Level Input Voltage	|I_O| < 1.0 υA V_{DD} = 5V, V_O = 0.5V or 4.5V V_{DD} = 10V, V_O = 1.0V or 9.0V V_{DD} = 15V, V_O = 1.5V or 13.5V			1.5 3.0 4.0	V
V_{IH}	HIGH Level Input Voltage	|IO| < 1.0 υA V_{DD} = 5V, V_O = 0.5V or 4.5V V_{DD} = 10V, V_O = 1.0V or 9.0V V_{DD} = 15V, V_O = 1.5V or 13.5V	3.5 7.0 11.0			V
I_{OL}	LOW Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V V_{DD} = 10V, V_O = 0.5V V_{DD} = 15V, V_O = 1.5V	0.44 1.1 3			mA
I_{OH}	HIGH Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V V_{DD} = 10V, V_O = 9.5V V_{DD} = 15V, V_O = 13.5V			–0.44 –1.1 –3	mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V V_{DD} = 15V, V_{IN} = 15V			–0.3 0.3	υA
Ioz	3-STATE Output Leakage Current	VDD = 15V, VIN = 0V or 15V			1	υA

Note 3: I_{OL} and I_{OH} are tested one output at a time.

AC Electrical Characteristics (Note 5)

TA=25 C, CL =0 pF

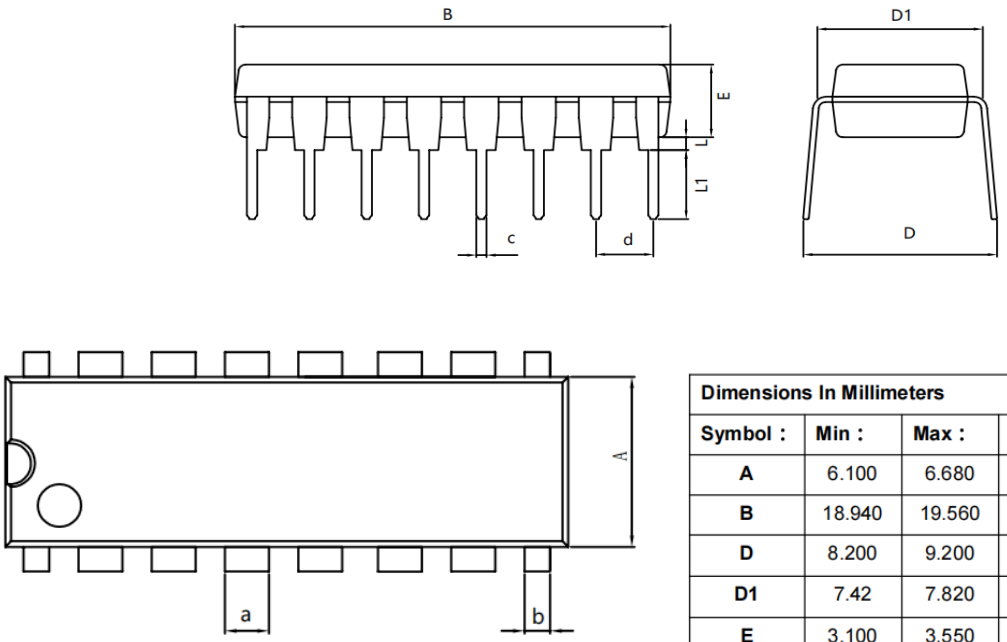
Symbol	Parameter	Conditions	Min	Typ	Max	Units
tPHL, tPLH	Propagation Delay Clock to QS	VDD=5.0V VDD=10V VDD=15V		300 125 95	600 250 190	ns
tPHL, tPLH	Propagation Delay Clock to Q	VDD=5.0V VDD=10V VDD=15V		230 110 75	460 220 150	ns
tPHL, tPLH	Propagation Delay Clock to Parallel Out	VDD=5.0V VDD=10V VDD=15V		420 195 135	840 390 270	ns
tPHL, tPLH	Propagation Delay Strobe to Parallel Out	VDD=5.0V VDD=10V VDD=15V		290 145 100	580 290 200	ns
tPHZ	Propagation Delay HIGH Level to HIGH Impedance	VDD=5.0V VDD=10V VDD=15V		140 75 55	280 150 110	ns
tPLZ	Propagation Delay LOW Level to HIGH Impedance	VDD=5.0V VDD=10V VDD=15V		140 75 55	280 150 110	ns
tPZH	Propagation Delay HIGH Impedance to HIGH Level	VDD=5.0V VDD=10V VDD=15V		140 75 55	280 150 110	ns
tPZL	Propagation Delay HIGH Impedance to LOW Level	VDD=5.0V VDD=10V VDD=15V		140 75 55	280 150 110	ns
tTHL, tTLH	Transition Time	VDD=5.0V VDD=10V VDD=15V		100 50 40	200 100 80	ns
tSU	Set-Up Time Data to Clock	VDD=5.0V VDD=10V VDD=15V	80 40 20	40 20 10		ns
tr, tf	Maximum Clock Rise and Fall Time	VDD=5.0V VDD=10V VDD=15V	1 1 1			ns
tPC	Minimum Clock Pulse Width	VDD=5.0V VDD=10V VDD=15V	200 100 83	100 50 40		ns
tPS	Minimum Strobe Pulse Width	VDD=5.0V VDD=10V VDD=15V	200 80 70	100 40 35		ns

fmax	Maximum Clock Frequency	VDD=5.0V VDD=10V VDD=15V	1.5 3.0 4.0	3.0 6.0 8.0		MHz MHz MHz
CIN	Input Capacitance	Any Input		5.0	7.5	pF

Note 5: AC Parameters are guaranteed by DC correlated testing.

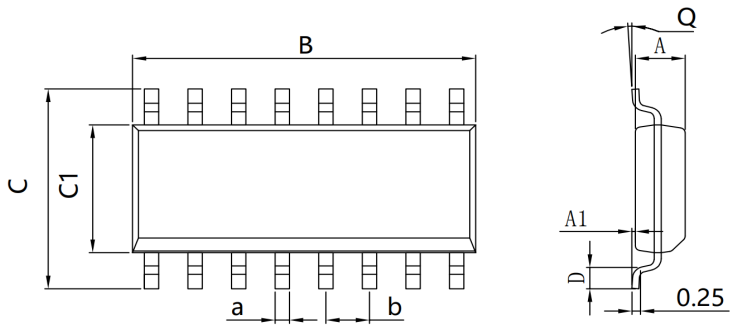
PACKAGE MECHANICAL DATA

DIP16



Dimensions In Millimeters					
Symbol :	**Min :**	**Max :**	**Symbol :**	**Min :**	**Max :**
A	6.100	6.680	**L**	0.500	0.800
B	18.940	19.560	**a**	1.524 TYP	
D	8.200	9.200	**b**	0.889 TYP	
D1	7.42	7.820	**c**	0.457 TYP	
E	3.100	3.550	**d**	2.540 TYP	
L	0.500	0.800			

SOP16



Dimensions In Millimeters					
Symbol :	**Min :**	**Max :**	**Symbol :**	**Min :**	**Max :**
A	1.225	1.570	**D**	0.400	0.950
A1	0.100	0.250	**Q**	0°	8°
B	9.800	10.00	**a**	0.420 TYP	
C	5.800	6.250	**b**	1.270 TYP	
C1	3.800	4.000			