三态输出-移位存储总线寄存器

简要说明

CD4094 是带输出锁存和三态控制的串入/并出高速转换器，具有使用简单、功耗低、驱动能力强和控制灵活等优点。

CD4094 的引脚定义如图。其中(1)脚为锁存端，(2)脚为串行数据输入端，(3)脚为串行时钟端。

(1)脚为高电平时，8 位并行输出口 Q1～Q8 在时钟的上升沿随串行输入而变化；(1)脚为低电平时，输出锁定。利用锁存端可方便地进行片选和级联输出控制。

(15)脚为并行输出状态控制端，(15)脚为低电平时，并行输出端处在高阻状态。

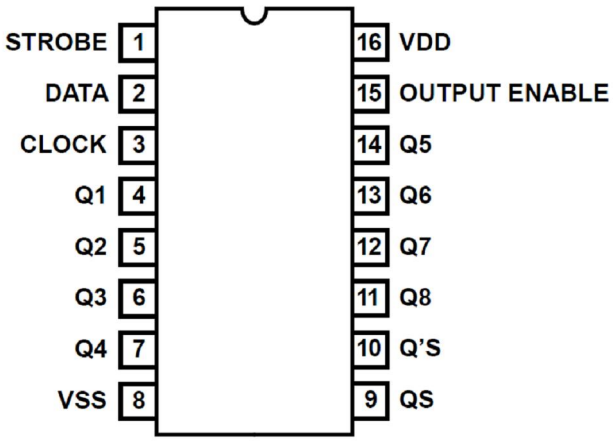
在用 CD4094 作显示输出时，可使显示数码闪烁。

(9)脚 QS、(10)脚 Q'S 是串行数据输出端，用于级联。QS 端在第 9 个串行时钟的上升沿开始输出，Q'S 端在第 9 个串行时钟的下降沿开始输出。

CD4094 提供了 DIP16 封装形式。

引脚图

TOP VIEW



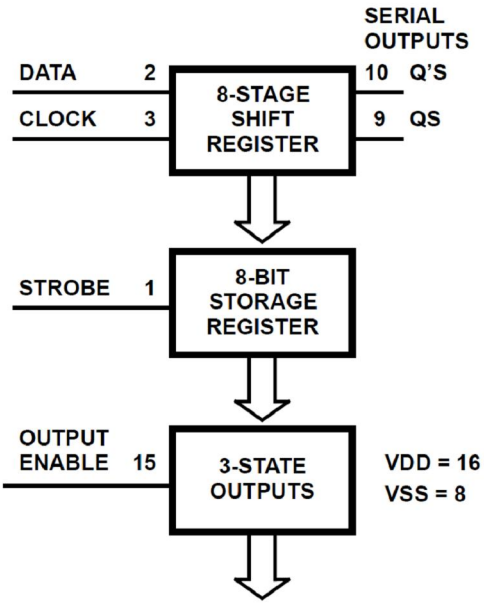
主要特点：

- 宽工作电源+3V~15V
- 抗干扰性能高 0.45 VDD (typ.)
- 低功耗，TTL兼容，
  可驱动两路74L或1路74LS
- 三态输出
- 全静态工作（15V）

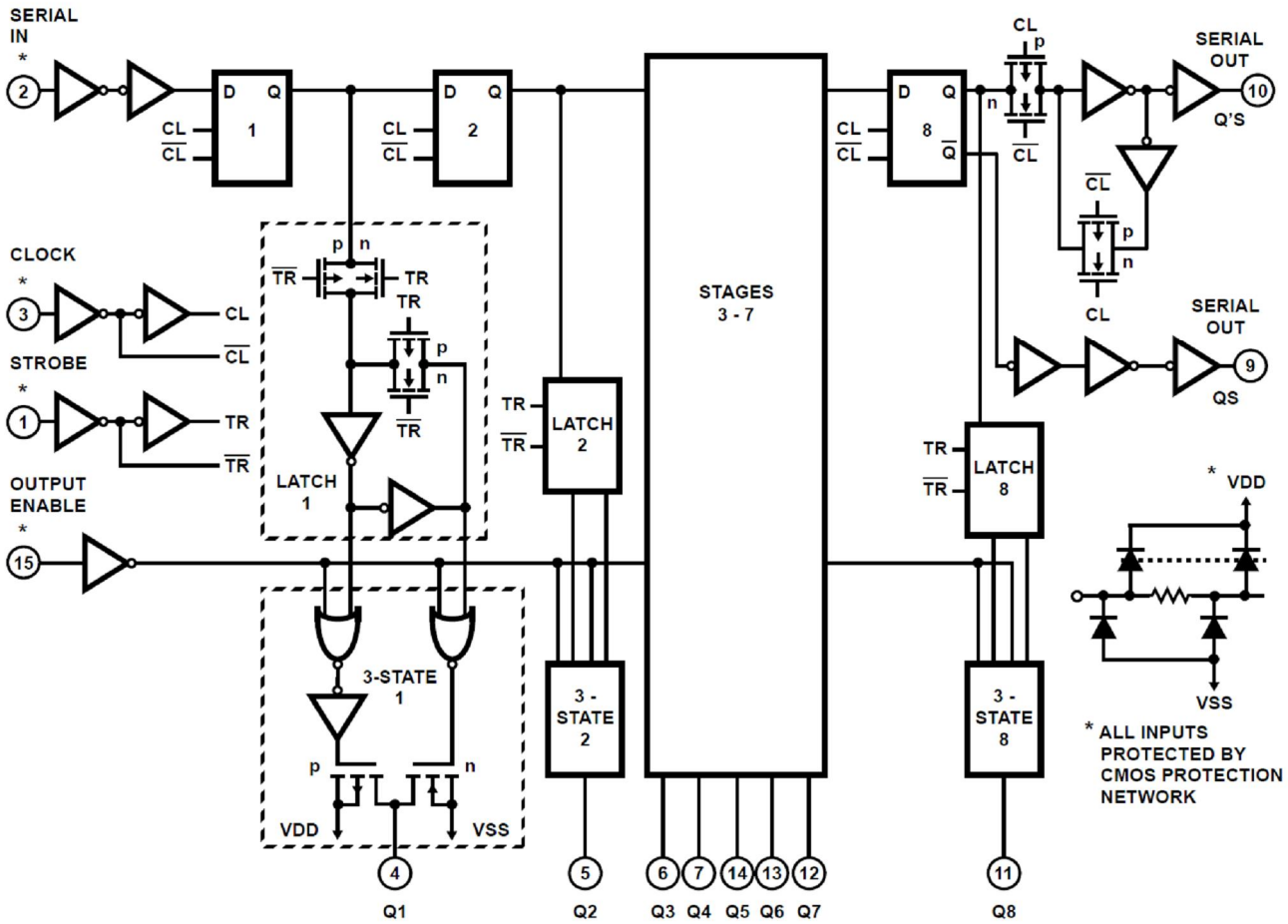
主要应用：

- 串并数据转换
- 遥控器保持寄存器
- 双级转移，保持，和总线应用

功能框图


SERIAL OUTPUTS
DATA 2
CLOCK 3
8-STAGE SHIFT REGISTER
10 Q'S
9 QS
STROBE 1
8-BIT STORAGE REGISTER
OUTPUT ENABLE 15
3-STATE OUTPUTS
VDD = 16
VSS = 8
PARALLEL OUTPUTS Q1 - Q8
(TERMINALS 4, 5, 6, 7, 14, 13, 12, 11, RESPECTIVELY)

逻辑框图（整体）


SERIAL IN
CLOCK
STROBE
OUTPUT ENABLE
LATCH 1
LATCH 2
STAGES 3 - 7
LATCH 8
3-STATE 1
3 - STATE 2
3 - STATE 8
SERIAL OUT
Q'S
SERIAL OUT
QS
VDD
VSS
* ALL INPUTS PROTECTED BY CMOS PROTECTION NETWORK
Q1
Q2
Q3 Q4 Q5 Q6 Q7
Q8

真值表

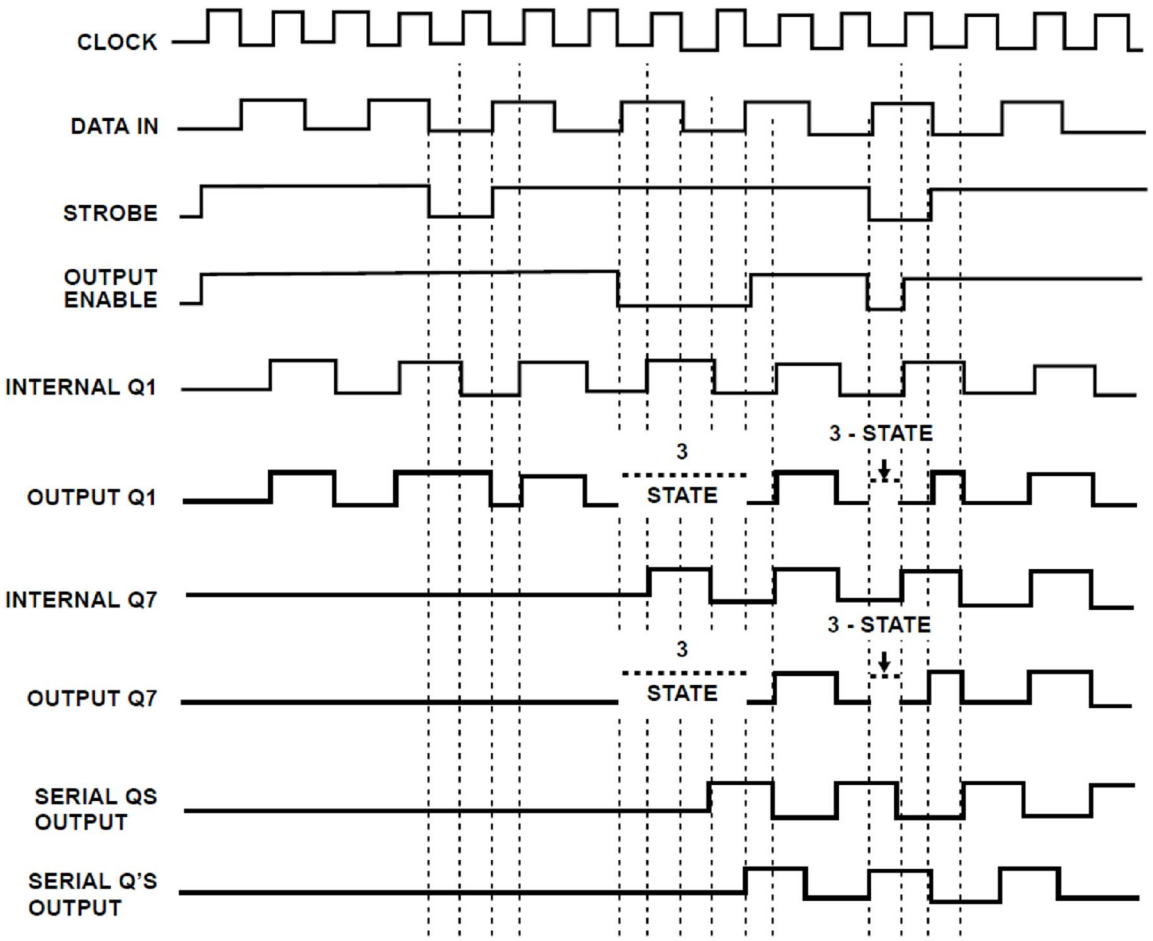
TRUTH TABLE

CL△	OUTPUT ENABLE	STROBE	DATA	PARALLEL OUTPUTS		SERIAL OUTPUTS	
				Q1	QN	QS*	Q'S
⌐‾	0	X	X	OC	OC	Q7	NC
‾⌐	0	X	X	OC	OC	NC	Q7
⌐‾	1	0	X	NC	NC	Q7	NC
⌐‾	1	1	0	0	QN-1	Q7	NC
⌐‾	1	1	1	1	QN-1	Q7	NC
‾⌐	1	1	1	NC	NC	NC	Q7

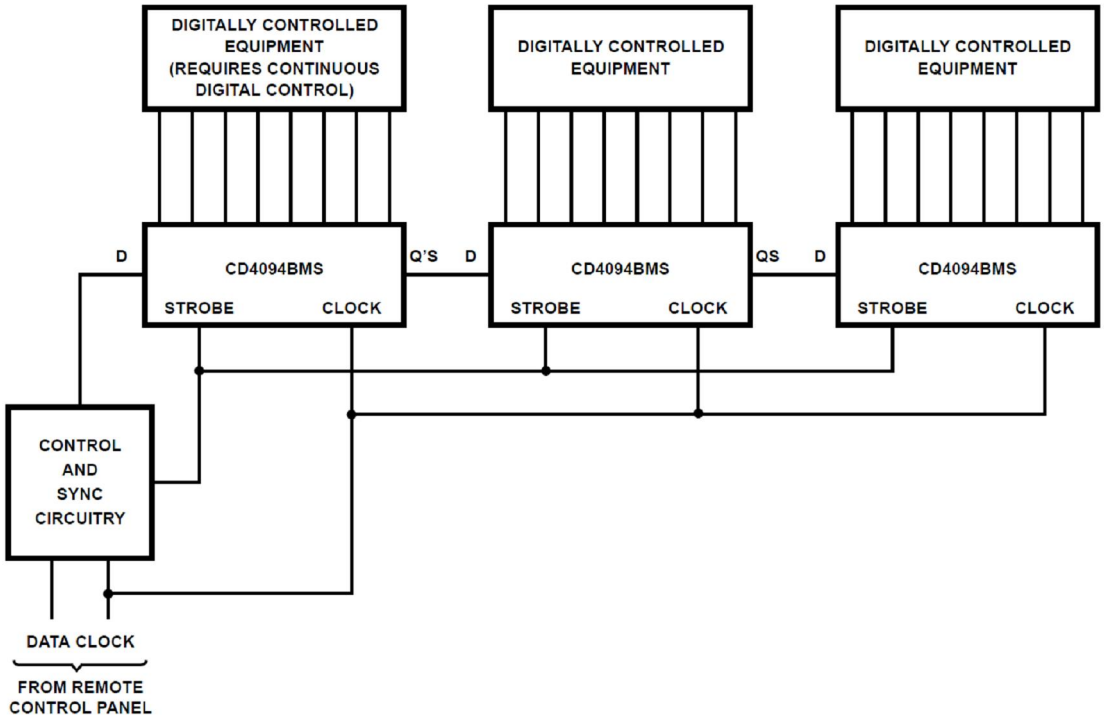
△ = Level Change
X = Don't Care
NC = No Change
OC = Open Circuit
Logic 1 = High
Logic 0 = Low

* At the positive clock edge information in the 7th shift register stage is transferred to the 8th register stage and the QS output

时序图



多级控制寄存应用



参数特性

Absolute Maximum Ratings(Note 1)

（极限参数）

(Note 2)

DC Supply Voltage (V_{DD})	-0.5 to +18 V_{DC}
	-0.5 to V_{DD} +0.5 V_{DC}
(T_S)	-55°C to +150°C
	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

（推荐工作条件）

DC Supply Voltage (V_{DD})	+3 V_{DC} to +15 V_{DC} Input Voltage (V_{IN})
Input Voltage (V_{IN})	0 to V_{DD} V_{DC} Storage Temperature
Operating Temperature Range (T_A)	0°C to +70°C Power Dissipation (P_D)

Note 1: “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of “Recommended Operating Conditions” and “Electrical Characteristics” provides conditions for actual device operation.

Note 2: VSS = 0V unless otherwise specified.

DC Electrical Characteristics (Note 2)

符号	参数	测试条件	温度	+25℃		单位
			Min	**Typ**	**Max**	

I_{DD}	Quiescent Device Current	V_{DD} = 5V V_{DD} =10V V_{DD} = 15V			5 10 20	υA
V_{OL}	LOW Level Output Voltage	|IO| < 1.0 υA V_{DD} = 5V V_{DD} =10V V_{DD} = 15V 10V		0 0 0	0.05 0.05 0.05	V
V_{OH}	HIGH Level Output Voltage	|IO| < 1.0 υA V_{DD} = 5V V_{DD} =10V V_{DD} = 15V V_{DD}	4.95 9.95 14.95	5 10 15		V
V_{IL}	LOW Level Input Voltage	|IO| < 1.0 υA V_{DD} = 5V, V_O = 0.5V or 4.5V V_{DD} = 10V, V_O = 1.0V or 9.0V V_{DD} = 15V, V_O = 1.5V or 13.5V			1.5 3.0 4.0	V
V_{IH}	HIGH Level Input Voltage	|IO| < 1.0 υA V_{DD} = 5V, V_O = 0.5V or 4.5V V_{DD} = 10V, V_O = 1.0V or 9.0V V_{DD} = 15V, V_O = 1.5V or 13.5V	3.5 7.0 11.0			V
I_{OL}	LOW Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V V_{DD} = 10V, V_O = 0.5V V_{DD} = 15V, V_O = 1.5V	0.44 1.1 3			mA
I_{OH}	HIGH Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V V_{DD} = 10V, V_O = 9.5V V_{DD} = 15V, V_O = 13.5V			–0.44 –1.1 –3	mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V V_{DD} = 15V, V_{IN} = 15V			–0.3 0.3	υA
Ioz	3-STATE Output Leakage Current	VDD = 15V, VIN = 0V or 15V			1	υA

Note 3: I_{OL} and I_{OH} are tested one output at a time.

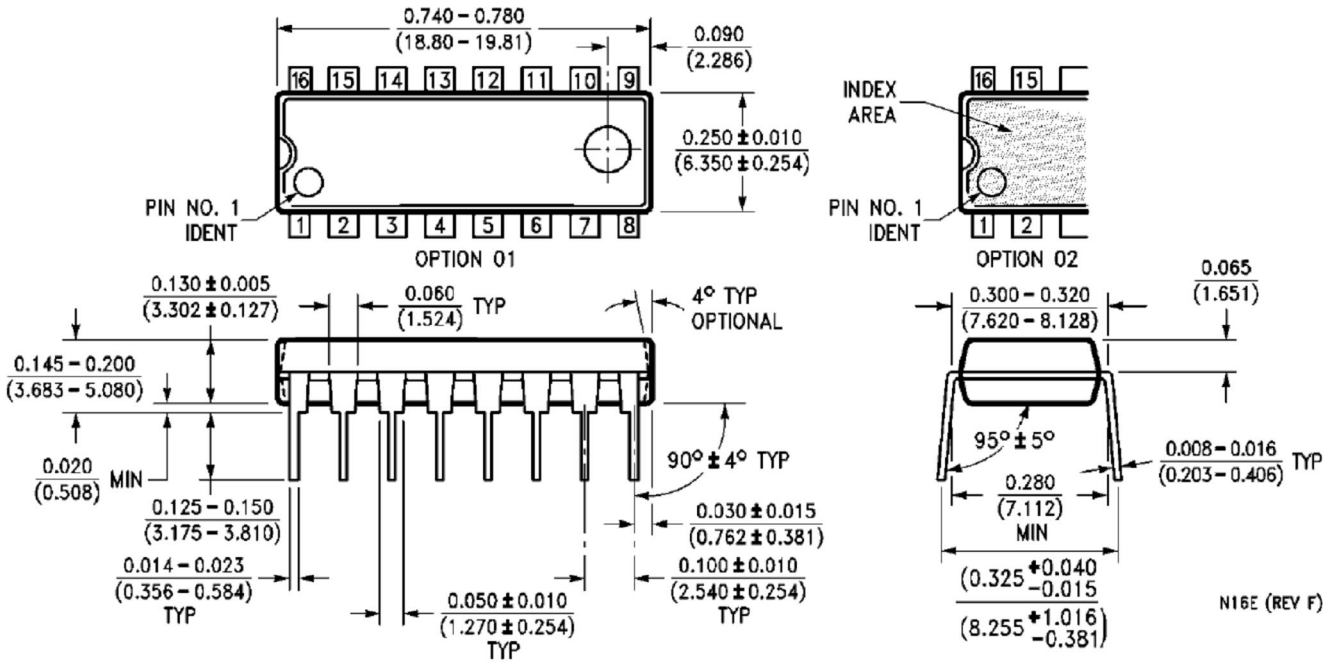
AC Electrical Characteristics (Note 5)

TA=25 C, CL =0 pF

Symbol	Parameter	Conditions	Min	Typ	Max	Units
tPHL, tPLH	Propagation Delay Clock to QS	VDD=5.0V VDD=10V VDD=15V		300 125 95	600 250 190	ns
tPHL, tPLH	Propagation Delay Clock to Q	VDD=5.0V VDD=10V VDD=15V		230 110 75	460 220 150	ns
tPHL, tPLH	Propagation Delay Clock to Parallel Out	VDD=5.0V VDD=10V VDD=15V		420 195 135	840 390 270	ns
tPHL, tPLH	Propagation Delay Strobe to Parallel Out	VDD=5.0V VDD=10V VDD=15V		290 145 100	580 290 200	ns
tPHZ	Propagation Delay HIGH Level to HIGH Impedance	VDD=5.0V VDD=10V VDD=15V		140 75 55	280 150 110	ns
tPLZ	Propagation Delay LOW Level to HIGH Impedance	VDD=5.0V VDD=10V VDD=15V		140 75 55	280 150 110	ns
tPZH	Propagation Delay HIGH Impedance to HIGH Level	VDD=5.0V VDD=10V VDD=15V		140 75 55	280 150 110	ns
tPZL	Propagation Delay HIGH Impedance to LOW Level	VDD=5.0V VDD=10V VDD=15V		140 75 55	280 150 110	ns
tTHL, tTLH	Transition Time	VDD=5.0V VDD=10V VDD=15V		100 50 40	200 100 80	ns
tSU	Set-Up Time Data to Clock	VDD=5.0V VDD=10V VDD=15V	80 40 20	40 20 10		ns
tr, tf	Maximum Clock Rise and Fall Time	VDD=5.0V VDD=10V VDD=15V	1 1 1			ns
tPC	Minimum Clock Pulse Width	VDD=5.0V VDD=10V VDD=15V	200 100 83	100 50 40		ns
tPS	Minimum Strobe Pulse Width	VDD=5.0V VDD=10V VDD=15V	200 80 70	100 40 35		ns

fmax	Maximum Clock Frequency	VDD=5.0V VDD=10V VDD=15V	1.5 3.0 4.0	3.0 6.0 8.0		MHz MHz MHz
CIN	Input Capacitance	Any Input		5.0	7.5	pF
Note 5: AC Parameters are guaranteed by DC correlated testing.						

相关封装信息



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E