Six CMOS Schmidt triggers

summary

CD 40106B Is a monolithic, complementary CMOS integrated circuit, which is a basic circuit composed of P channel and N channel enhanced field effect tube complementary. It ensures that the forward and reverse threshold voltages VT + and VT-are less affected by temperature and hysteresis. All inputs are equipped with protected diodes between VDD and VSS to eliminate electrostatic damage and interference to the chip.

1. Features

Make a wide power supply voltage range: 3V ~15V

High noise tolerance: 0.7 VDD (typical value)

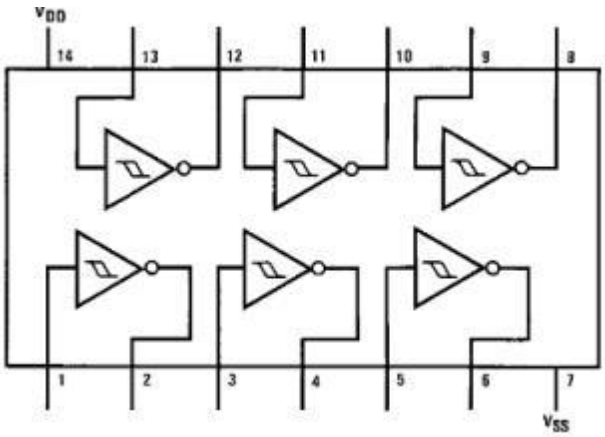
Make compatible with low-power TTL circuits

Order may drive two 74L circuits or one 74LS circuit respectively

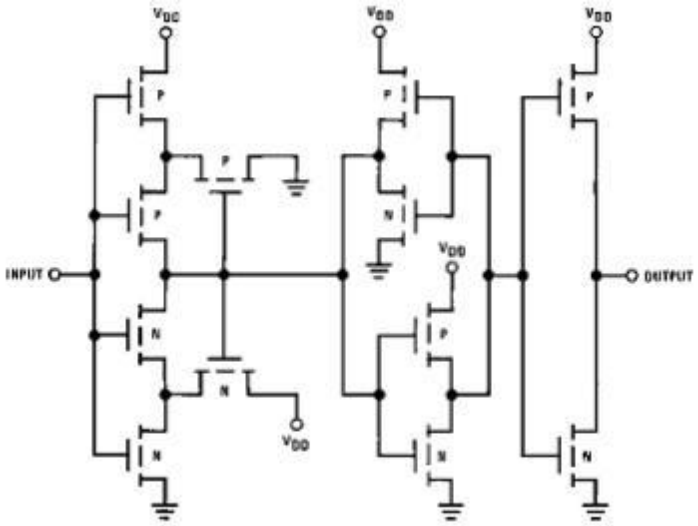
Stagnetic lag voltage: 0.4 VDD (typical value)

Order 0.2 VDD guaranteed value

2. Connection block diagram



3. A Schematic diagram



4. Limit parameters

(Note 1) (Note 2)

parameter	symbol	span
The DC power supply voltage	VDD	-0.5~+18VDC
input voltage	VIN	-0.5~VDD +0.5VDC
Storage temperature range	T S	-65℃~150℃
power dissipation DI P SOP	P D	 700mW 500mW
Welding temperature (10 seconds)	T L	260℃

5. Recommend the working conditions

(Note 2)

parameter	symbol	span
The DC power supply voltage	VDD	3~15VDC
input voltage	VIN	0~VDDVDC
operating temperature range	TA	- 10℃~70℃

Note 1: "Absolute maximum" means the adjacent state, which cannot guarantee the safe use of the circuit. The Operating Temperature Range and Electrical parameters tables provide the actual operating state of the circuit.

Note 2: VSS = 0 V unless otherwise specified

6. Direct current parameters

(Note 3)

symbol	parameter	condition	-40℃		+25℃			+85℃		unit
			minimum	maximum	minimum	typical case	maximum	minimum	maximum	
ID D	quiescent current	VDD =5V VDD =10V VDD =15V		4.0 8.0 16.0			4.0 8.0 16.0		30 60 120	μA
V OL	Low-level output voltage	|IO |＜1uA VDD =5V VDD =10V VDD =15V		 0.05 0.05 0.05			 0.05 0.05 0.05		 0.05 0.05 0.05	V
V OH	high level output voltage	|IO |＜1uA VDD =5V VDD =10V VDD =15V	 4.95 9.95 14.95		 4.95 9.95 14.95	 5 10 15		 4.95 9.95 14.95		V
VT -	Negative-direction threshold voltage	VDD =5V ,VO =4.5V VDD =10V ,VO =9V VDD =15V,VO=13.5V	0.7 1.4 2.1	2.0 4.0 6.0	0.7 1.4 2.1	1.4 3.2 5.0	2.0 4.0 6.0	0.7 1.4 2.1	2.0 4.0 6.0	V
VT +	Forward threshold voltage	VDD =5V ,VO =0.5V VDD =10V ,VO =9V VDD =15V,VO=1.5V	3.0 6.0 9.0	4.3 8.6 12.9	3.0 6.0 9.0	3.6 6.8 10.0	4.3 8.6 12.9	3.0 6.0 9.0	4.3 8.6 12.9	V
V H	Return differential voltage (VT +-VT -)	VDD =5V VDD =10V VDD =15V	1.0 2.0 3.0	3.6 7.2 10.8	1.0 2.0 3.0	2.2 3.6 5.0	3.6 7.2 10.8	1.0 2.0 3.0	3.6 7.2 10.8	V
I OL	Low-level output current (Note 3)	VDD =5V ,VO =0.4V VDD =10V,VO=0.5V VDD =15V,VO=1.5V	0.52 1.3 3.6		0.44 1.1 3.0	0.88 2.25 8.8		0.36 0.9 2.4		mA
IO H	High-level output current (Note 3)	VDD =5V ,VO =4.6V VDD =10V,VO=9.5V VDD =15V,VO=13.5V	-0.52 - 1.3 -3.6		-0.44 - 1.1 -3.0	-0.88 -2.25 -8.8		-0.36 -0.9 -2.4		mA

IIN	input currenton	VDD =15V ,VIN =0V VDD =15V,VIN=15V		-0.30 0.30		-10^{-5} 10^{-5}	-0.30 0.30		- 1.0 1.0	μA

Note 3: The IOH and IOL test values at the same output side.

7. AC current parameters

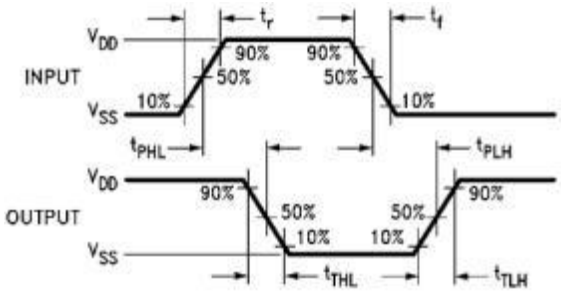
(Note 4)

When Ta =25℃, RL = 200 K Ω, CL = 50 Pf, Tr, Tf = 20 nS, unless otherwise specified

symbol	parameter	condition	least value	representative value	crest value	unit
Of either the tPHL or the tPLH	Transmission delay time from the input end to the output end	VDD=5V VDD=10V VDD=15V		220 80 70	400 200 160	n s
Of either tTHL or tTLH	duration of transmission	VDD=5V VDD=10V VDD=15V		100 50 40	200 100 80	n s
CIN	Average input capacitor	Any input		5	7.5	p F
C PD	Power equivalent capacitance	Any door circuit		14		p F

Note 4: The AC parameters are based on the DC-related tests.

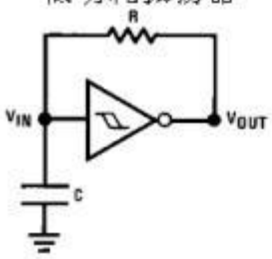
8. Exchange-time waveform map



tr=tf=20ns

9. Typical applications

低功耗振荡器

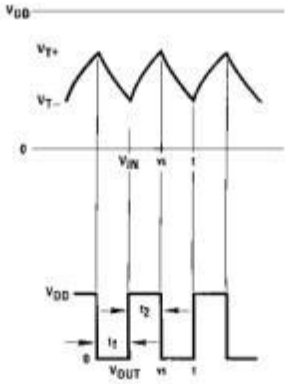


$$t_1 \approx RC \ln \frac{V_{T+}}{V_{T-}}$$

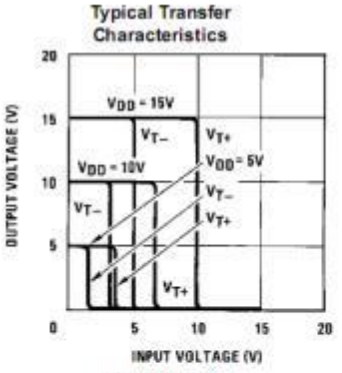
$$t_2 \approx RC \ln \frac{V_{DD} - V_{T-}}{V_{DD} - V_{T+}}$$

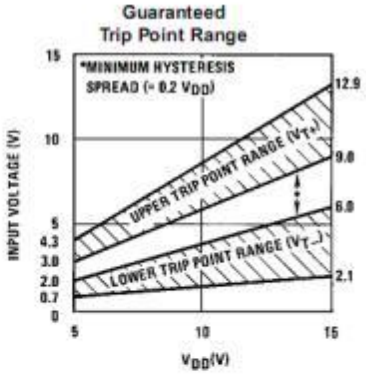
$$f \approx \frac{1}{RC \ln \frac{V_{T+}(V_{DD} - V_{T-})}{V_{T-}(V_{DD} - V_{T+})}}$$

注释：方程假设 $t_1 + t_2 >> t_{PHL} + t_{PLH}$

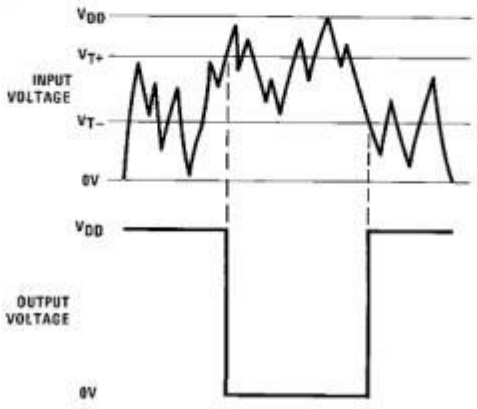


10., with its typical characteristics



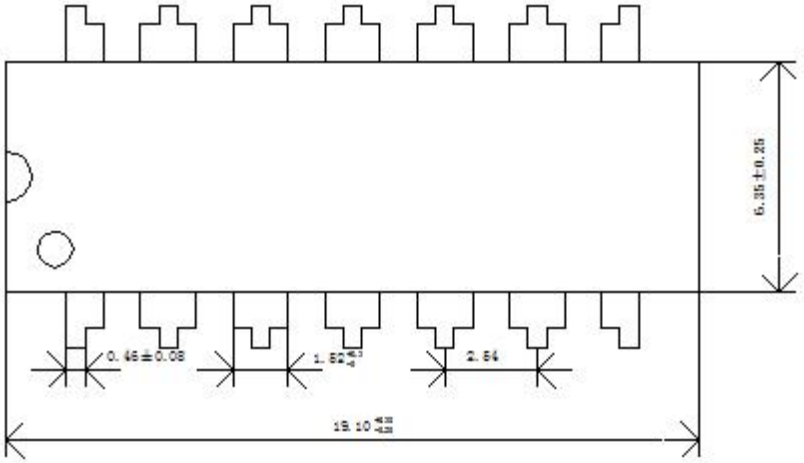


Guaranteed



11. Package size diagram

Make the DIP 14 package form



Make the SOP 14 package form