Description：

CD40106 is a low-power, wide operating voltage range Schmitt inverter designed using advanced CMOS technology. It integrates six independent Schmitt inverter circuits internally, with high anti-interf erence and driving capabilities.

Features：

-Low input current: IIN ≤ 1uA, @ VIN=VDD=15V, Ta=25 ℃
-Low static power consumption: IDD ≤ 4uA, @ VDD=15V, Ta=25 ℃
-Wide operating voltage range: 3V to 18V
-Encapsulation form: DIP14, SOP14

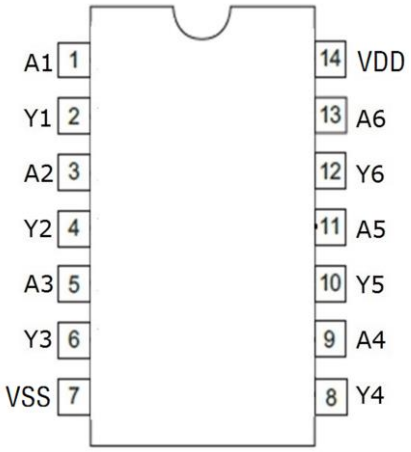
Application:

-Monostable multi harmonic oscillator
-High noise environment system
-Waveform and pulse shaper
-Other application areas

Pin Assignment：

PIN NO. DIP14/SOP14	Definition	PIN NO. DIP14/SOP14	Definition
1	A1	14	VDD
2	Y1	13	A6
3	A2	12	Y6
4	Y2	11	A5
5	A3	10	Y5
6	Y3	9	A4
7	VSS	8	Y4
Note: A is the input pin; Y is the output pin.			

DIP14/SOP14



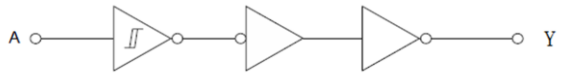
DIP:CD40106BD 1000/BOX
SOP:CD40106 2500/REEL

Absolute Maximum Ratings：

parameter	Symbol	Max	Unit
working voltage	V_{CC}	-0.5-20	V
Input/output voltage	V_{IN}、$V_{I/O}$	-0.5+VSS-VDD+0.5V	V
Input current	I_I	±10	mA
Dissipated power	P_D	500	mW
working temperature	T_A	0-70	℃
Storage temperature	T_S	-65-150	℃
Pin welding temperature	T_W	260,10s	℃

Note: Limit parameters refer to the limit values that cannot be exceeded under any conditions. If the limit value is excee ded, it may cause physical damage such as product degradation; At the same time, it cannot be guaranteed that the chi p can function properly when approaching the limit parameters.

logic diagram



$A=\overline{Y}$

Truth table

Input	Output
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

Recommended operating conditions

parameter	Symbol	Min	Typ	Max	Unit
working voltage	V_{DD}	3		18	V
Input and output voltage	V_{IN}、$V_{I/O}$	0		VDD	V
working temperature	T_A	0		60	℃

electrical characteristic

DC electrical characteristics:(Ta=25℃)

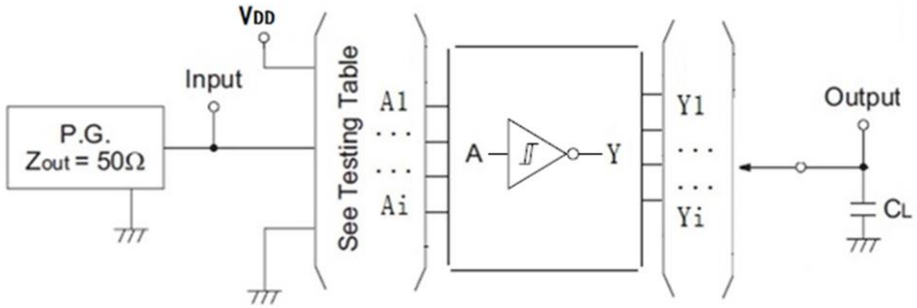
symbol	parameter	Test conditions	VDD（V）	min	typ	max	unit
V_{TP+}	High level Switching thresh old voltage	$\|I_O\|\leqslant 1uA$	5	-	2.5	-	V
			10	-	4.2	-	V
			15	-	5.8	-	V
V_{TN-}	Low level Switching threshol d voltage	$\|I_O\|\leqslant 1uA$	5	-	1.2	-	V
			10	-	2.0	-	V
			15	-	2.6	-	V
V_{TH}	Hysteresis vol tage （V_{TP+}-V_{TN-}）		5	-	1.3	-	V
			10	-	2.2	-	V
			15	-	3.2	-	V
V_{OH}	high level output voltage	$\|I_O\|<1uA$	5	4.95	-	-	V
			10	9.95	-	-	V
			15	14.95	-	-	V
V_{OL}	Low Level Output Voltage	$\|I_O\|<1uA$	5	-	-	0.05	V
			10	-	-	0.05	V
			15	-	-	0.05	V
I_{OH}	High Level Output Current	V_O= 4.6V	5	-	-3.0	-	mA
		V_O= 9.5V	10	-	-6.4	-	mA
		V_O= 13.5V	15	-	-22	-	mA
I_{OL}	Low Level Output Current	V_O= 0.4V	5	-	4.8	-	mA
		V_O= 0.5V	10	-	11.5	-	mA
		V_O= 1.5V	15	-	42	-	mA
I_{IN}	Input Current	V_{IN}=VDD or VSS	18	-	0.01	1	uA
I_{DD}	Working current	V_{IN}=VDD or VSS	5	-	0.01	1	uA
			10	-	0.01	2	uA
			15	-	0.01	4	uA
			18	-	0.01	20	uA

AC electrical characteristics: CL=51pF, Ta=25 ℃, see testing method.

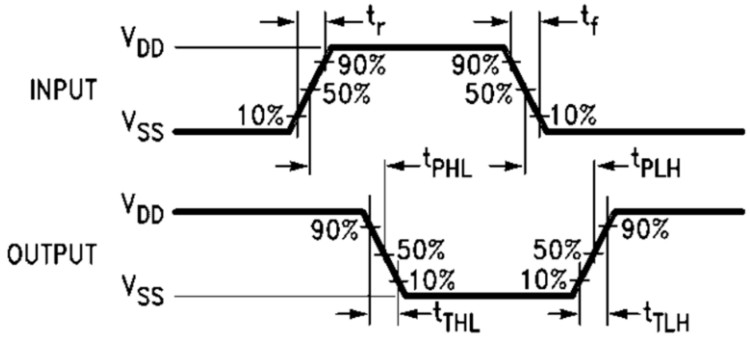
parameter	symbol	Test conditions	min	typ	max	unit
最大传输延迟时间 A to Y	t_{PHL}	VDD=5V	–	80	–	ns
	t_{PLH}		–	140	–	ns
	t_{PHL}	VDD=10V	–	45	–	ns
	t_{PLH}		–	75	–	ns
	t_{PHL}	VDD=15V	–	35	–	ns
	t_{PLH}		–	55	–	ns
输出上升/下降延迟时间	t_{THL}	VDD=5V	–	30	–	ns
	t_{TLH}		–	30	–	ns
	t_{THL}	VDD=10V	–	15	–	ns
	t_{TLH}		–	20	–	ns
	t_{THL}	VDD=15V	–	10	–	ns
	t_{TLH}		–	15	–	ns

test method

1. Test wiring diagram



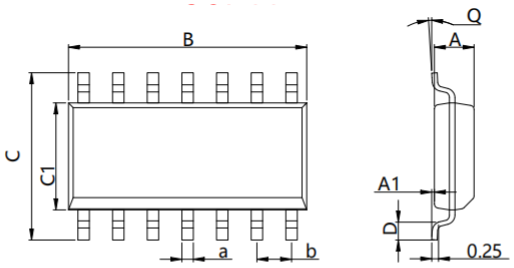
2. Schematic diagram of waveform measurement



Note:

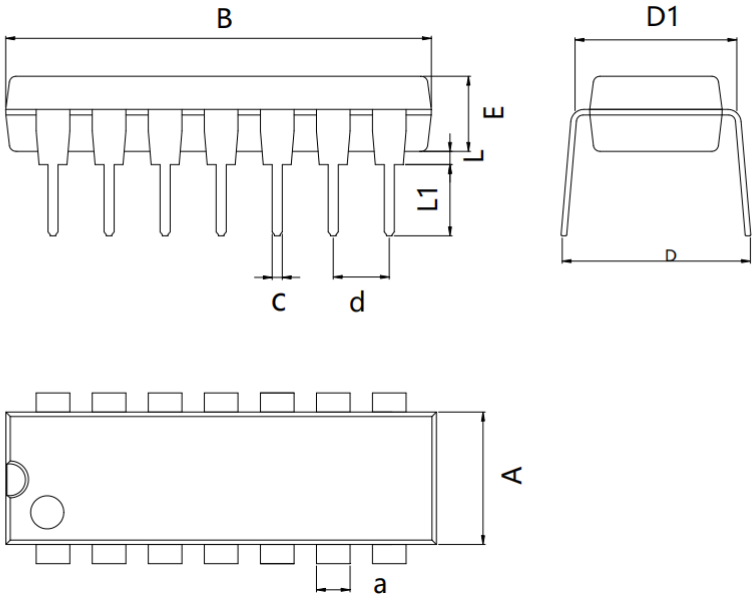
1. See Testing Table refers to the corresponding testing items in the AC electrical characteristics table;
2. The CL capacitor is an external patch capacitor (0603), connected near the output pin, and the capacitor ground is close to the chip VSS;
3. Input: Port input level, f=1MHz, D=50% square wave, tr=tf ≤ 20ns;
4. Output: Y-end output test.

SOP14



Dimensions In Millimeters(SOP14)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	8.55	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	8.75	6.20	4.00	0.80	8°	0.45	

DIP14



Dimensions In Millimeters(DIP14)										
Symbol:	A	B	D	D1	E	L	L1	a	C	d
Min:	6.10	18.94	8.40	7.42	3.10	0.50	3.00	1.50	0.40	2.54 BSC
Max:	6.68	19.56	9.00	7.82	3.55	0.70	3.60	1.55	0.50	