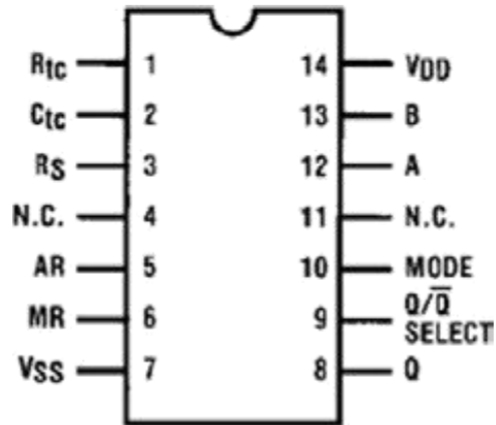# Programmable Timer

Description：

The CD4541 programmable timer consists of a 16 bit binary counter, a built-in oscillator (with external capacitors and two resistors), output control logic, and a special power on reset circuit. The particularity of the power reset circuit lies in: 1. No additional static current consumption; 2. Regardless of whether the power reset function is allowed or disabled, this function is effective throughout the entire voltage range (5-15V).

If the power on reset function is enabled, the internal timer and counter are initialized when the power is turned on. When the power supply is already turned on, external reset pulses can also initialize timers and counters. After the reset action is completed, the frequency of the built-in oscillator is determined by the external RC constant. A 16 bit counter divides the oscillator frequency by controlling the division ratio based on the value of any 4-bit binary number.

Features：

-Available division rates: 2_8, 2_{10}, 2_{13} or 2_{16}.

-Built in low-power RC oscillator (capable of maintaining ± 2% accuracy throughout the entire temperature range, ± 10% accuracy, and ± 3% process deviation accuracy across the entire operating power supply voltage range within a frequency range of less than 10kHz).

-Oscillator frequency range: DC~100kHz.

-When using an external clock, the internal oscillator can be bypassed.

-After the power is turned on, all counters are automatically reset and initialized.

-The external main reset is completely independent of the automatic reset operation.

-Can be used as a 2n frequency divider or a single timer.

-The output logic level can be flexibly changed by selecting Q/Q.

-Reset (automatic or master reset) can put the oscillator in a disabled state during the reset period, reducing dynamic power consumption during this period. The clock adjustment circuit allows for extremely slow clock up and down times to operate.

-Wide power supply voltage range: 5.0-15V.

-Three level parameters of 5V-10V-15V.

-High noise tolerance -0.45VDD (typ).

-Within the entire temperature range of 15V, the maximum input leakage current is 1 μ A.

Pin Assignment：

```
Rtc   — 1      14 —  VDD
Ctc   — 2      13 —  B
RS    — 3      12 —  A
N.C.  — 4      11 —  N.C.
AR    — 5      10 —  MODE
MR    — 6       9 —  Q/Q̄ SELECT
Vss   — 7       8 —  Q
```

Truth table

pin no.	state	
	0	1
5	Automatic reset operation	Prohibit automatic reset
6	Timer operation	Main reset
9	After resetting, the initial output value is low level	After resetting, the initial output value is high level
10	Single loop mode	Loop mode

Frequency divider

| A	B	Nth counter level of data	2N value
0	0	13	8192
0	1	10	1024
1	0	8	256
1	1	16	65536

Working characteristics

-When the automatic reset pin is set to "0", the counter circuit is initialized after the power is turned on. Alternatively, when the power supply is already connected and the main reset pin is set to "1", the counter circuit can also be initialized. Both of these reset methods can reset all counters Simultaneously reset, regardless of the original state of the counter.

-The frequency of an RC oscillator is determined by the external RC constant: $f=1/(2.3R_{tc}C_{tc})$ (frequency within the range of 1kHz $\leq f \leq$ 100kHz). The selected value for Rs is $R_s=2R_{tc}$ ($R_s \geq 10k \Omega$)

-The Q/Q pin is used to select the high or low output level. When the counter is in the reset state, if the Q/Q selection pin is set to "0", then the Q output is "0"; If the Q/Qselection pin is set to "1", then the Q output is "1".

--When the mode control pin (Pin10) is set to "1", the selected count value is continuously transmitted to the output. When the mode control pin is set to "0" and in the reset state, the RS trigger is reset (see logic diagram). At the beginning of the line counting, after counting to 2n-1, the RS trigger is set and causes a change in the output state. Therefore, after each count of 2n-1, the output state is changed once. Therefore, it is necessary to apply a main reset pulse or change the level of the mode control pin in order to reset the single cycle operation.

-The timing selection input terminals (A and B) provide a two bit address to select any of the four counting stages (2^8, 2^{10}, 2^{13}, or 2^{16}) for output. The 2n count in the frequency divider represents the Q-output of the Nth stage of the counter. When A is "1" and B is also "1", 2^{16} will be selected. When A is "1" and B is "0", the normal count will be interrupted, and the 9th level of the counter will skip the previous 8th level counter and directly receive the clock from the oscillator (effective count is 28 output).
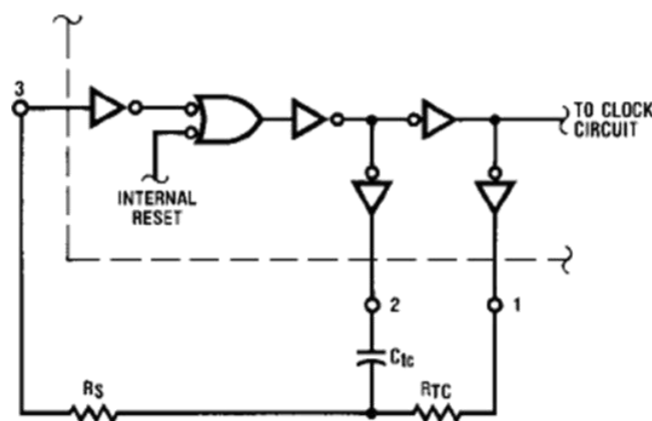
RC configuration diagram for oscillator circuit use

Logic Block Diagram
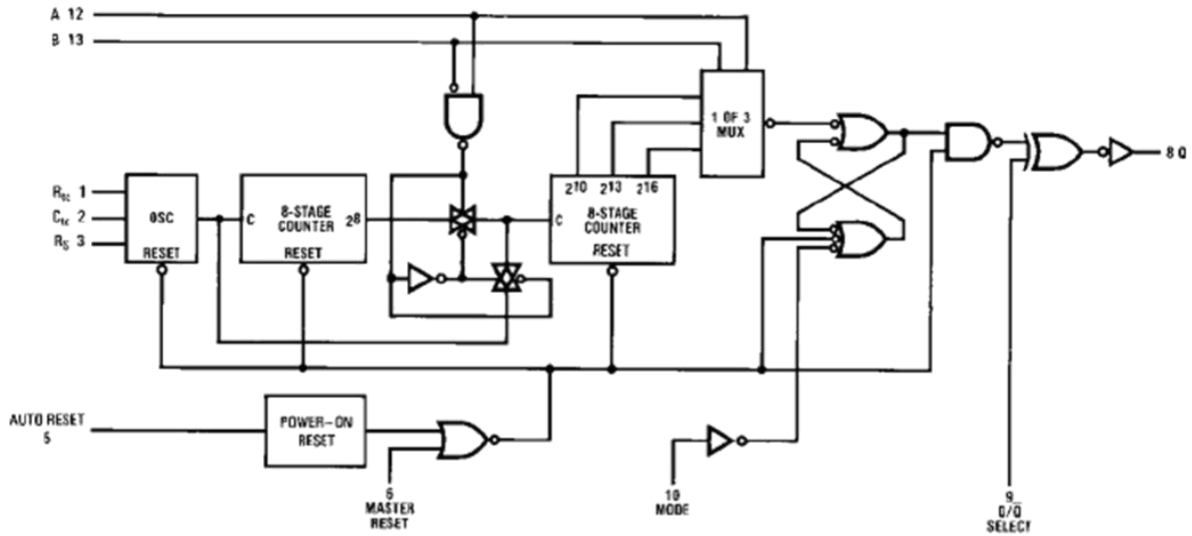
Absolute Maximum Ratings

symbol	parameter	condition	value	unit
V_{DD}	Power supply voltage range		-0.5～+18	V
V_{IN}	Input voltage range		-0.5～V_{DD}+0.5	V
T_{stg}	Working temperature range		-65～150	℃
P_D	maximum power dissipation	DIP	700	mW
		SOP	500	
T_L	Spot welding temperature		245	℃

Recommended working conditions

symbol	parameter	condition	value	unit
VDD	Power supply voltage range		5～15	V
VIN	Input voltage range		0～V_{DD}	V
TA	Working temperature range		-40～85	℃

note:
The working conditions of the limit parameters exceed the range that ensures the normal operation of the device. Under extreme parameter conditions, the safety of device operation cannot be guaranteed. It is recommended that users use the devices according to the recommended working conditions in the electrical parameter table.
Unless otherwise specified, VS=0V.

Electrical parameters

(Reference voltage: Vss)

parameter	symbol	condition	V$_{DD}$	-40℃		25℃			+85℃		unit
				min	max	min	typ	max	min	max	
Static current	IDD	VIN=V$_{DD}$ or VSS	5.0		20		0.005	20		150	μA
		VIN=V$_D$ or VSS	10		40		0.010	40		300	
		VIN=V$_{DD}$ or VSS	15		80		0.015	80		600	
Output low level	VOL	IO<1uA	5.0		0.05	0	0.05			0.05	V
			10		0.05	0	0.05			0.05	
			15		0.05	0	0.05			0.05	
Output high level	VOH	IO<1uA	5.0	4.95		4.95	5		4.95		V
			10	9.95		9.95	10		9.95		
			15	14.95		14.95	15		14.95		
Input low-level	VOL	VO=4.or 0.5V	5.0		1.5		2	1.5		1.5	V
		VO=9.or1.0V	10		3.0		4	3.0		3.0	
		VO=13 or 1.5V	15		4.0		6	4.0		4.0	
Input high level	VOH	VO=4.or0.5V	5.0	3.5		3.5	3		3.5		V
		VO=9.or1.0V	10	7.0		7.0	6		7.0		
		VO=13 or 1.5V	15	11		11	9		11		
Low level output power	IOL	VOL=0.4	5.0	1.70		1.30	2.0		1.10		mA
		VOL=0.5V	10	2.40		2.20	5.0		2.00		
		VOL=1.5V	15	9.70		8.50	15.0		6.50		
High level output current	IOH	VOH=2.5V	5.0	5.1		3.20	6.80		2.90		mA
		VOH=9.5V	10	3.80		3.50	5.80		2.85		
		VOH=13.5V	15	8.5		7.0	16.0		6.22		
Input current	IIN	VIN=0V	15		-0.3		-10^{-5}	-0.3		-1.0	μA
		VIN=15V	15		3.0		10^{-5}	0.3		1.0	

*：IOH and IOL are the results obtained by testing one output simultaneously.

Dynamic electrical parameters

（TA＝25℃ ）

| symbol	parameter	condition	VDD	min	typ	max	unit
tTLH	Output rise time		5V		50	200	ns
			10V		30	100	
			15V		25	80	
tTHL	Output drop time		5V		50	200	ns
			10V		30	100	
			15V		25	80	
tPLH tPHL	Transmission delay time	Power off and on transmission delay, from clockTo Q	5V		1.8	4.0	ns
			10V		0.6	1.5	
			15V		0.4	1.0	
tPHL tPLH	Transmission delay time	Transmission delay of power on/off, from clock To Q	5V		3.2	8.0	ns
			10V		1.5	3.0	
			15V		1.0	2.0	
tWH	Clock pulse width		5V	400	200		ns
			10V	200	100		
			15V	150	70		
tcl	Clock pulse frequency		5V		2.5	1.0	MHz
			10V		6.0	3.0	
			15V		8.5	4.0	
tWH	MR pulse width		5V	400	170		ns
			10V	200	75		
			15V	150	50		
CI	Average input capacitance	Any input			5.0	7.5	pF
CPD	Power consumption capacitance				100		pF

Remarks:

1. The accuracy of AC parameters is guaranteed by the relevant DC parameters. CPD represents the dynamic power consumption of each CMOS device when there is no load.

Test circuit and waveform diagram

Power consumption test circuit and waveform diagram

(R_{tc} and C_{tc} outputs are left open)
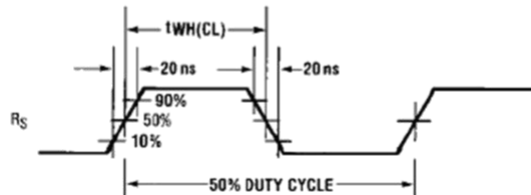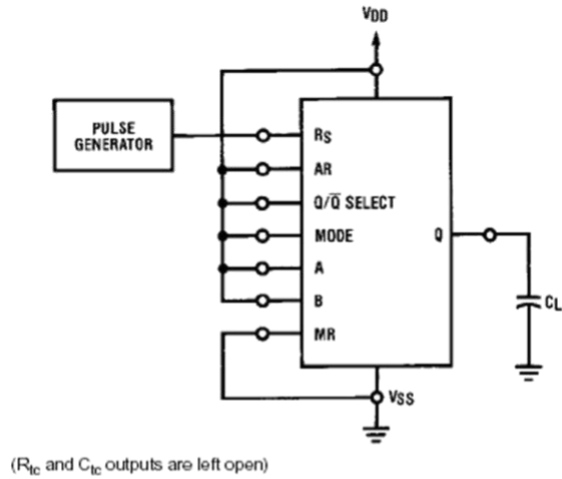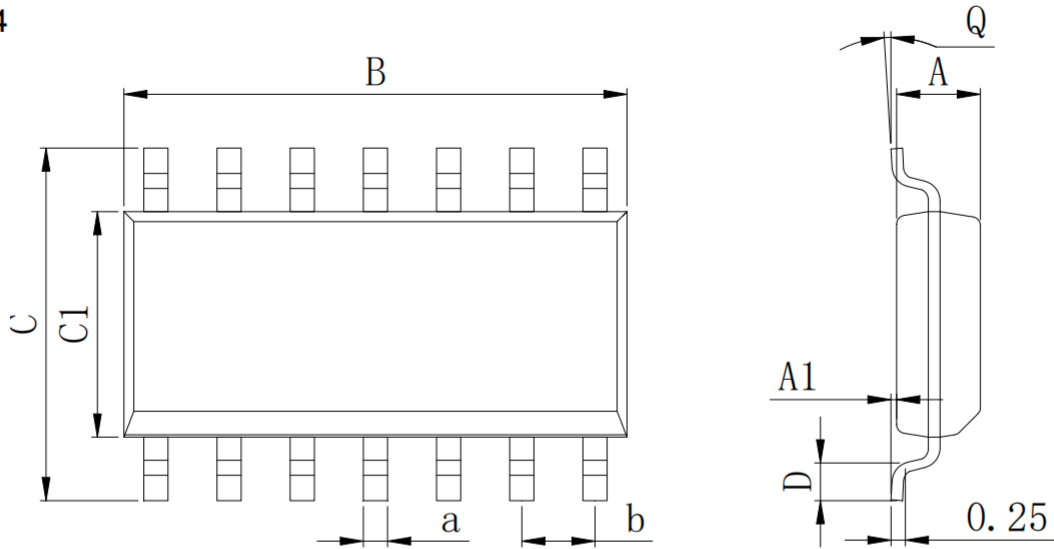

Switching time test circuit and waveform diagram
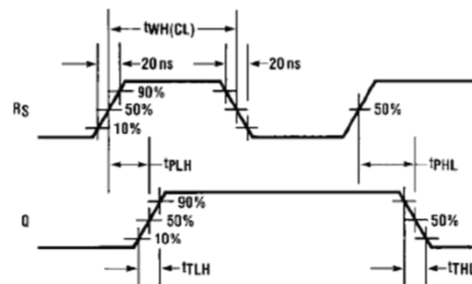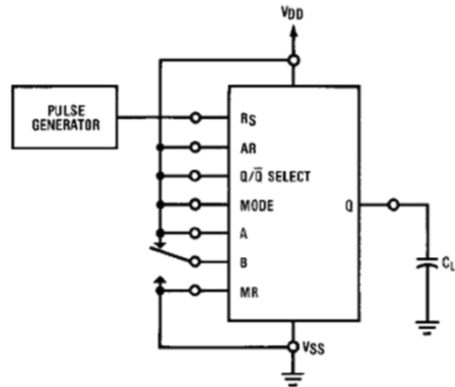
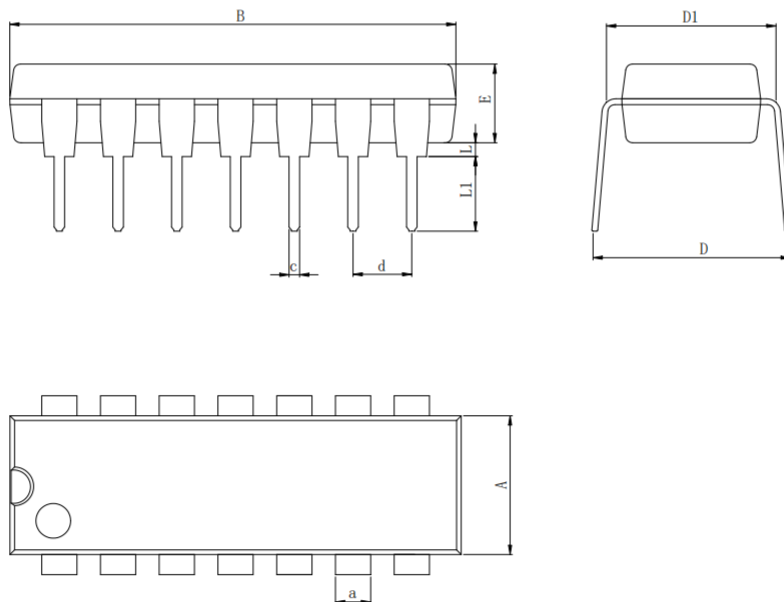## Packaging dimensions

SOP-14

Dimensions In Millimeters(SOP14)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	8.55	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	8.75	6.20	4.00	0.80	8°	0.45	

DIP-14

Dimensions In Millimeters(DIP14)									
Symbol:	A	B	D	D1	E	L	L1	a	c	d
Min:	6.10	18.94	8.10	7.42	3.10	0.50	3.00	1.50	0.40	2.54 BSC
Max:	6.68	19.56	10.9	7.82	3.55	0.70	3.60	1.55	0.50	