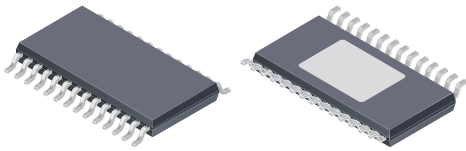


## Microstepping DMOS Driver with Translator

### FEATURES AND BENEFITS

- $\pm 2.8$  A, 40 V output rating
- Low  $R_{DS(on)}$  outputs, 0.22  $\Omega$  source, 0.15  $\Omega$  sink typical
- Automatic current decay mode detection/selection
- 3 to 5.5 V logic supply voltage range
- Mixed, fast, and slow current decay modes
- Home output
- Synchronous rectification for low power dissipation
- Internal UVLO and thermal shutdown circuitry
- Crossover-current protection
- Short-to-ground protection
- Short-to-VBB protection
- Shorted load protection

**Package: 28-lead TSSOP (suffix LP) with exposed thermal pad**



Not to scale

### DESCRIPTION

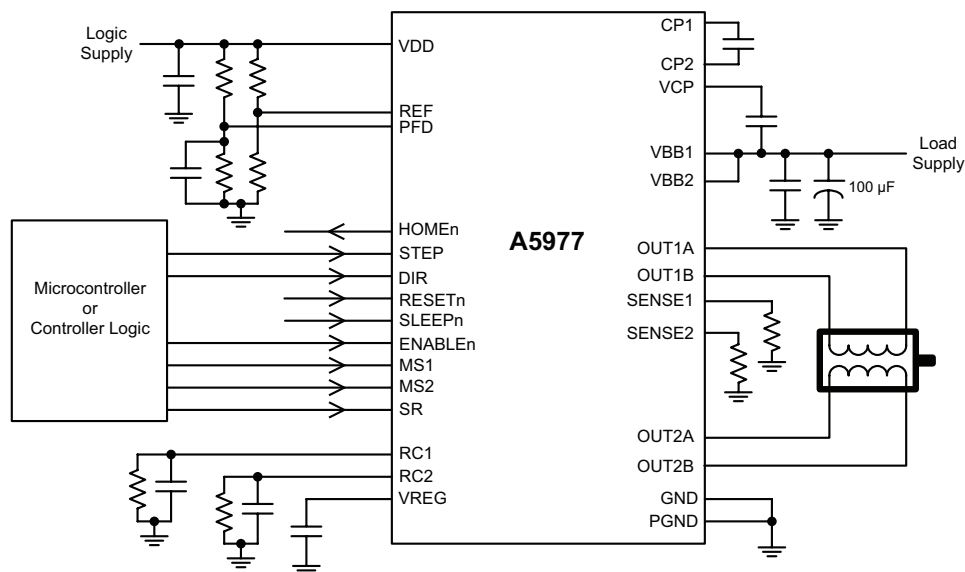
The A5977 is a complete microstepping motor driver with built-in translator. It is designed to operate bipolar stepper motors in full-, half-, quarter-, and eighth-step modes, with output drive capability of 40 V and  $\pm 2.8$  A. The A5977 includes a fixed off-time current regulator that has the ability to operate in slow-, fast-, or mixed-decay modes. This current-decay control scheme results in reduced audible motor noise, increased step accuracy, and reduced power dissipation.

The translator is the key to the easy implementation of the A5977. Simply inputting one pulse on the STEP input drives the motor one step (two logic inputs determine if it is a full-, half-, quarter-, or eighth-step). There are no phase sequence tables, high-frequency control lines, or complex interfaces to program. The A5977 interface is an ideal fit for applications where a complex microprocessor is unavailable or overburdened.

Internal synchronous rectification control circuitry is provided to improve power dissipation during PWM operation. Internal circuit protection includes thermal shutdown with hysteresis, undervoltage lockout (UVLO), and crossover-current protection. Special power-up sequencing is not required.

The A5977 is supplied in a thin (<1.2 mm) 28-pin TSSOP with an exposed thermal pad (suffix LP). The package is lead (Pb) free (suffix -T), with 100% matte-tin leadframe plating.

### Typical Application



## SELECTION GUIDE

Part Number	Package	Packing
A5977GLPTR-T	28-pin TSSOP	4000 pieces per reel



## SPECIFICATIONS

## ABSOLUTE MAXIMUM RATINGS

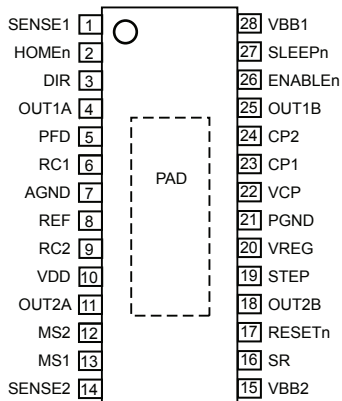
Load Supply Voltage	$V_{BB}$		40	V
Logic Supply Voltage	$V_{DD}$		7	V
Logic Input Voltage Range	$V_{IN}$	Pulsed, $t_W > 30$ ns	$-0.3$ to $V_{DD} + 0.3$	V
		Pulsed, $t_W < 30$ ns	$-1$ to $V_{DD} + 1$	V
SENSEx Voltage (DC)	$V_{SENSE}$		0.5	V
Reference Voltage	$V_{REF}$		$V_{DD}$	V
Output Current	$I_{OUT}$	Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C.	$\pm 2.8$	A
Operating Ambient Temperature	$T_A$	Range G	-40 to 105	°C
Junction Temperature	$T_J(\text{max})$		150	°C
Storage Temperature	$T_{stg}$		-55 to 150	°C

## THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package LP, on 4-layer PCB based on JEDEC standard	28	°C/W

\*Additional thermal information available on Allegro website.

## PINOUT DIAGRAM AND TERMINAL LIST TABLE



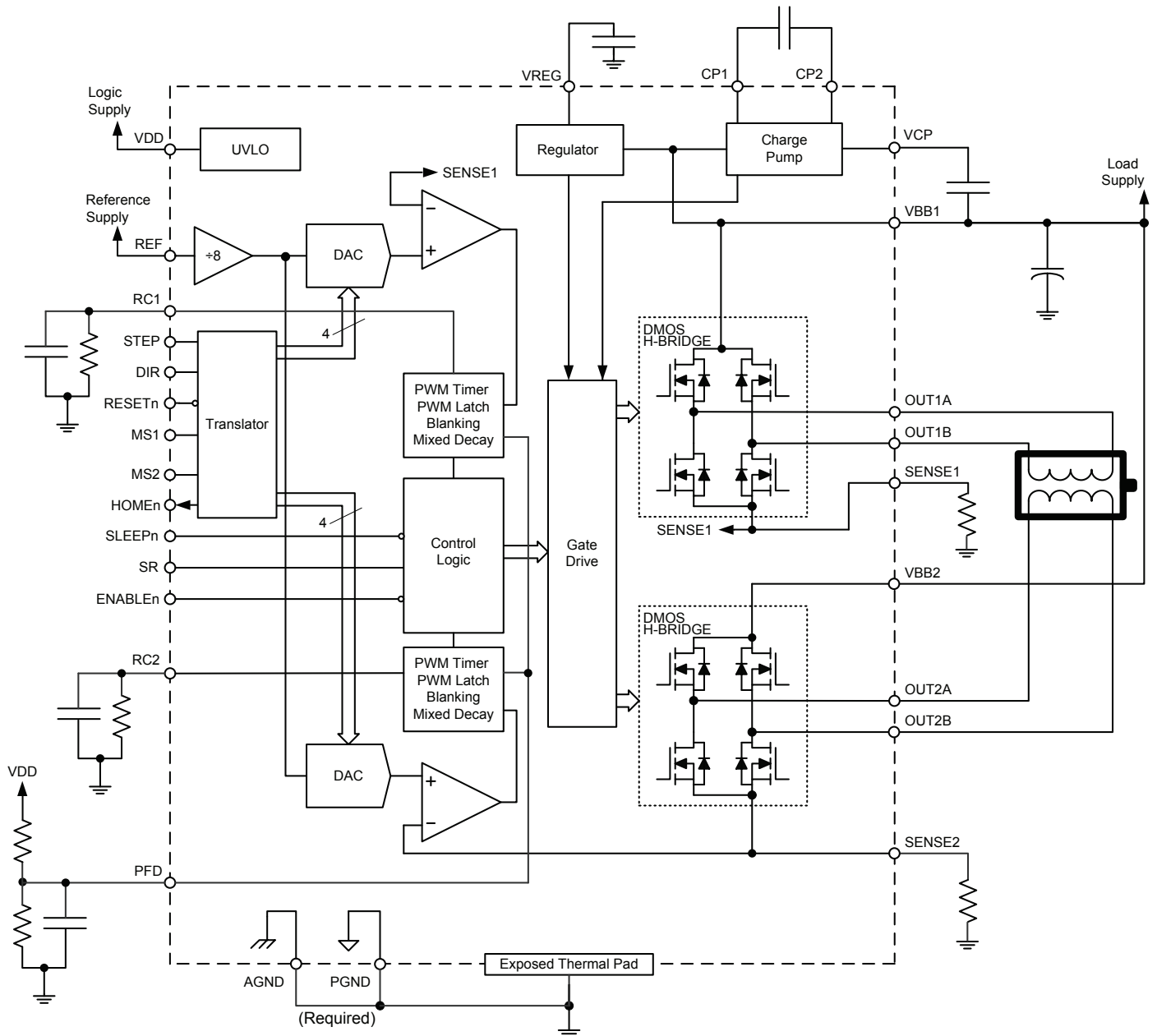
**Package LP,  
28-Pin TSSOP**

**Terminal List Table**

Number	Name	Description
1	SENSE1	Sense resistor for bridge 1
2	HOMEn	Logic output
3	DIR	Logic input
4	OUT1A	DMOS full-bridge 1, output A
5	PFD	Analog input for mixed-decay setting
6	RC1	Analog input for fixed off-time, bridge 1
7	AGND*	Analog ground
8	REF	Gm reference input
9	RC2	Analog input for fixed off-time, bridge 2
10	VDD	Logic supply voltage
11	OUT2A	DMOS full-bridge 2, output A
12	MS2	Logic input
13	MS1	Logic input
14	SENSE2	Sense resistor for bridge 2
15	VBB2	Load supply for bridge 2
16	SR	Logic input
17	RESETn	Logic input
18	OUT2B	DMOS full-bridge 2, output B
19	STEP	Logic input
20	VREG	Regulator decoupling
21	PGND*	Power ground
22	VCP	Reservoir capacitor
23	CP1	Charge pump capacitor
24	CP2	Charge pump capacitor
25	OUT1B	DMOS full-bridge 1, output B
26	ENABLEn	Logic input
27	SLEEPn	Logic input
28	VBB1	Load supply for bridge 1
–	PAD*	Thermal pad

\* GND, PGND, and thermal pad must be connected together externally under the device.

FUNCTIONAL BLOCK DIAGRAM



**ELECTRICAL CHARACTERISTICS<sup>1</sup>: Valid at  $T_A = 25^\circ\text{C}$ ,  $V_{BB} = 40\text{ V}$ , unless otherwise noted**

Characteristics	Symbol	Test Conditions	Min.	Typ. <sup>2</sup>	Max.	Units
Load Supply Voltage Range	$V_{BB}$	Operating	8	–	40	V
		During sleep mode	0	–	40	V
Output Leakage Current	$I_{DSS}$	$V_{OUT} = V_{BB}$	–	<1	20	$\mu\text{A}$
		$V_{OUT} = 0\text{ V}$	–	<1	–20	$\mu\text{A}$
Output On-Resistance	$R_{DS(On)}$	Source driver, $I_{OUT} = -2.5\text{ A}$ , $T_J = 25^\circ\text{C}$	–	0.22	0.30	$\Omega$
		Sink driver, $I_{OUT} = 2.5\text{ A}$ , $T_J = 25^\circ\text{C}$	–	0.15	0.24	$\Omega$
Body Diode Forward Voltage	$V_F$	Source diode, $I_F = -2.5\text{ A}$	–	1	1.4	V
		Source diode, $I_F = 2.5\text{ A}$	–	1	1.4	V
VBB Supply Current	$I_{BB}$	$f_{PWM} < 50\text{ kHz}$ , duty cycle = 50%	–	–	8	mA
		Operating, outputs disabled	–	–	6	mA
		Sleep mode	–	<1	20	$\mu\text{A}$
VDD Supply Current	$I_{DD}$	$f_{PWM} < 50\text{ kHz}$ , duty cycle = 50%	–	–	12	mA
		Operating, outputs disabled	–	–	10	mA
		Sleep mode	–	<1	20	$\mu\text{A}$
<b>Control Logic</b>						
Logic Supply Voltage Range	$V_{DD}$	Operating	3	–	5.5	V
Logic Input Voltage	$V_{IN(1)}$		$0.7 \times V_{DD}$	–	–	V
	$V_{IN(0)}$		–	–	$0.3 \times V_{DD}$	V
Logic Input Current	$I_{IN(1)}$	$V_{IN} = 0.7 \times V_{DD}$	–20	<1	20	$\mu\text{A}$
	$I_{IN(0)}$	$V_{IN} = 0.3 \times V_{DD}$	–20	<1	20	$\mu\text{A}$
Maximum Step Frequency <sup>3</sup>	$f_{STEP}$		500	–	–	kHz
HOMEn Output Voltage	$V_{OH}$	$I_{OH} = -200\ \mu\text{A}$	$0.7 \times V_{DD}$	–	–	V
	$V_{OL}$	$I_{OL} = 200\ \mu\text{A}$	–	–	$0.3 \times V_{DD}$	V
Blank Time	$t_{BLANK}$	$R_T = 56\text{ k}\Omega$ , $C_T = 680\text{ pF}$	700	950	1200	ns
Fixed Off-Time	$t_{OFF}$	$R_T = 56\text{ k}\Omega$ , $C_T = 680\text{ pF}$	30	38	46	$\mu\text{s}$
Reference Input Voltage Range	$V_{REFx}$	Operating	0	–	$V_{DD}$	V
Reference Input Current	$I_{REF}$		–	–	$\pm 3$	$\mu\text{A}$
Gain ( $G_m$ ) Error <sup>4</sup>	$E_G$	$V_{REF} = 2\text{ V}$ , phase current = 100.0%	–	–	$\pm 5$	%
		$V_{REF} = 2\text{ V}$ , phase current = 70.7%	–	–	$\pm 5$	%
		$V_{REF} = 2\text{ V}$ , phase current = 38.3%	–	–	$\pm 10$	%
Crossover Dead Time	$t_{DT}$		100	475	800	ns
Motor Output Slew Time	$t_{SR}$	10% to 90% rising; 90% to 10% falling	20	–	120	ns

Continued on the next page...

**ELECTRICAL CHARACTERISTICS<sup>1</sup> (continued): Valid at  $T_A = 25^\circ\text{C}$ ,  $V_{BB} = 40\text{ V}$ , unless otherwise noted**

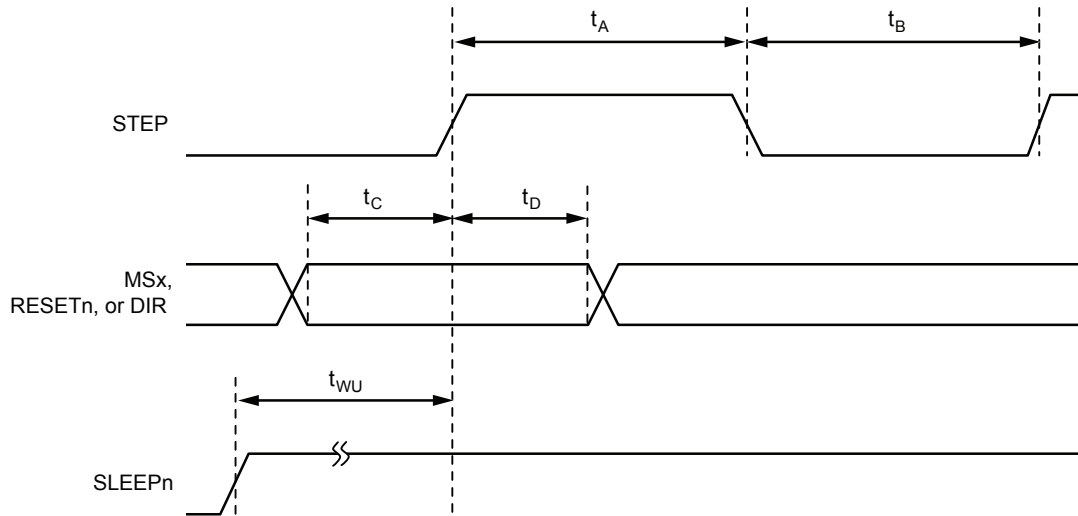
Characteristics	Symbol	Test Conditions	Min.	Typ. <sup>2</sup>	Max.	Units
<b>Protection Circuits</b>						
VDD UVLO Threshold	$V_{UV(VBB)}$	$V_{BB}$ rising	2.45	2.7	2.95	V
VDD UVLO Hysteresis	$V_{UV(VBB)HYS}$		50	100	–	mV
Overcurrent Protection Threshold	$I_{OCPST}$		3.5	–	–	A
Overcurrent Latch-Off Time	$t_{LATCHOFF(OC)}$		–	1.6	–	ms
Overcurrent Protection Blank Time	$t_{BLANK(OC)}$		–	1.5	–	$\mu\text{s}$
Thermal Shutdown Temperature	$T_{JSD}$		155	165	175	$^\circ\text{C}$
Thermal Shutdown Hysteresis	$T_{JSDHYS}$		–	15	–	$^\circ\text{C}$

<sup>1</sup> Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions. Performance may vary for individual units, within the specified maximum and minimum limits.

<sup>2</sup> Negative current is defined as coming out of (sourcing from) the specified device pin.

<sup>3</sup> Operation at a step frequency greater than the specified minimum value is possible but not warranted.

<sup>4</sup>  $E_G = ([V_{REF}/8] - V_{SENSE}) / (V_{REF}/8)$ .



Time Duration	Symbol	Typ.	Unit
STEP Minimum, high pulse width	$t_A$	1	$\mu\text{s}$
STEP Minimum, low pulse width	$t_B$	1	$\mu\text{s}$
Setup time, input change to STEP	$t_C$	200	ns
Hold time, input change to STEP	$t_D$	200	ns
Maximum wakeup time	$t_{WU}$	1	ms

Figure 1: Logic Interface Timing Diagram

Table 1: Microstep Resolution Truth Table

MS2	MS1	Microstep Resolution	Excitation Mode
L	L	Full Step	2 Phase
L	H	Half Step	1-2 Phase
H	L	Quarter Step	W1-2 Phase
H	H	Eighth Step	2W1-2 Phase

## FUNCTIONAL DESCRIPTION

## Device Operation

The A5977 is a complete microstepping motor driver with built-in translator for easy operation with minimal control lines. It is designed to operate bipolar stepper motors in full-, half-, quarter-, and eighth-step modes. The current in each of the two output full-bridges, all N-channel DMOS, is regulated with fixed off-time pulse-width modulated (PWM) control circuitry. The full-bridge current at each step is set by the value of an external current-sense resistor ( $R_S$ ), a reference voltage ( $V_{REF}$ ), and the output voltage of its DAC (which in turn is controlled by the output of the translator).

At power-up, or reset, the translator sets the DACs and phase current polarity to the initial home state (see figures for home-state conditions), and sets the current regulator for both phases to mixed-decay mode. When a step command signal occurs on the STEP input, the translator automatically sequences the DACs to the next level (see Table 2 for the current level sequence and current polarity). The microstep resolution is set by inputs MS1 and MS2 as shown in Table 1. If the new DAC output level is lower than the previous level, the decay mode for that full-bridge will be set by the PFD input (fast, slow, or mixed decay). If the new DAC level is higher or equal to the previous level, then the decay mode for that full-bridge will be slow decay. This automatic current-decay selection will improve microstepping performance by reducing the distortion of the current waveform due to the motor BEMF.

When stepping, if the new output levels of the DACs are higher than or equal to their previous levels, then the decay mode for that full-bridge is set to slow. If the new output levels of the DACs are lower than their previous output levels, then the decay mode for that full-bridge is set by the state of the PFD input (see PFD input description). This automatic current decay selection improves microstepping performance by reducing the distortion of the current waveform that results from the back-EMF of the motor. See Figure 6 on page 14 for decay mode detail.

## Internal PWM Current Control

Each full-bridge is controlled by a fixed off-time PWM current-control circuit that limits the load current to an appropriate level ( $I_{TRIP}$ ). Initially, a diagonal pair of source and sink DMOS outputs are enabled, and current flows through the motor wind-

ing and the current-sense resistor,  $R_S$ . When the voltage across  $R_S$  rises to the DAC output voltage, the current-sense comparator resets the PWM latch, which turns off the source driver (in slow-decay mode) or the sink and source drivers (in fast- or mixed-decay mode).

The maximum level of current limiting is set by the selection of  $R_S$  and the voltage at the VREF input with a transconductance function approximated by:

$$I_{TRIPmax} = V_{REF} / (8 \times R_S)$$

The DAC output reduces the VREF output to the current-sense comparator in precise steps (see Table 2 for %  $I_{TRIPmax}$  at each step).

$$I_{TRIP} = (\% I_{TRIPmax} / 100) \times I_{TRIPmax}$$

It is critical to ensure that the maximum rating on the SENSE terminal is not exceeded (0.5 V). For full-step mode,  $V_{REF}$  can be applied up to the maximum rating of  $V_{DD}$ , because the peak sense value is  $0.707 \times V_{REF} / 8$ . In all other modes,  $V_{REF}$  should not exceed 4 V.

## Fixed Off-Time

The internal PWM current-control circuitry uses a one-shot to control the time that the drivers remain off. The one-shot off-time,  $t_{OFF}$ , is determined by the selection of an external resistor ( $R_T$ ) and capacitor ( $C_T$ ) connected between the RC timing terminal and ground. The off-time, over a range of values of  $C_T = 470$  pF to 1500 pF and  $R_T = 12$  k $\Omega$  to 100 k $\Omega$  is approximated by:

$$t_{OFF} = R_T \times C_T$$

## RC Blanking

In addition to the fixed off-time of the PWM control circuit, the  $C_T$  component sets the comparator blanking time. This function blanks the output of the current-sense comparator when the outputs are switched by the internal current-control circuitry. The comparator output is blanked to prevent false overcurrent detection due to reverse-recovery currents of the clamp diodes, and/or switching transients related to the capacitance of the load. The blank time,  $t_{BLANK}$ , can be approximated by:

$$t_{BLANK} = 1400 \times C_T$$



**Step Input (STEP)**

A low-to-high transition on the STEP input sequences the translator and advances the motor one increment. The translator controls the input to the DACs and the direction of current flow in each winding. The size of the increment is determined by the state of inputs MS1 and MS2 (see Table 1).

**Microstep Select (MS1 and MS2)**

Input terminals MS1 and MS2 select the microstepping format per Table 1. Changes to these inputs do not take effect until the STEP command.

**Direction Input (DIR)**

The state of the DIR input will determine the direction of rotation of the motor.

**Percent Fast-Decay Input (PFD)**

When a STEP input command results in a lower output current than the previous step, it switches the output current decay for that bridge to either slow-, fast-, or mixed-decay, depending on the voltage level at the PFD input. If the voltage at the PFD input is greater than  $0.6 \times V_{DD}$ , then slow-decay is selected. If the voltage on the PFD input is less than  $0.21 \times V_{DD}$ , then fast-decay is selected. Mixed-decay is selected when the voltage on the PFD input is between these two levels. This terminal should be decoupled with a 0.1  $\mu$ F capacitor.

**Mixed-Decay Operation**

If the voltage on the PFD input is between  $0.6 \times V_{DD}$  and  $0.21 \times V_{DD}$ , the bridge will operate in mixed-decay mode when a STEP input command results in a lower output current than the previous step. As the trip point is reached, the bridge will go into fast-decay mode until the voltage on the RC terminal decays to the voltage applied to the PFD terminal. The time the bridge remains in fast-decay is approximated by:

$$t_{FD} = R_T \times C_T \times I_n (0.6 \times V_{DD} / V_{PFD})$$

After this fast-decay portion,  $t_{FD}$ , the bridge will switch to slow-decay mode for the remainder of the fixed off-time period.

**Reset Input (RESETn)**

The RESETn input (active low) sets the translator to a predefined home state (see figures for home state conditions) and turns off all of the DMOS outputs. The HOMEn output goes low and all STEP inputs are ignored until the RESETn input goes high.

**Home Output (HOMEn)**

The HOMEn output is a logic output indicator of the initial state of the translator. At power-up, the translator is reset to the home state (see figures for home state conditions), and the HOMEn output will be low. When the translator is not in the home state, this output is high.

**Synchronous Rectification**

When a PWM off-cycle is triggered by an internal current control, load current will recirculate according to the decay mode selected by the control logic. The A5977 synchronous rectification feature will turn on the appropriate MOSFETs during the current decay and effectively short out the body diodes with the low  $R_{DS(ON)}$  driver. This will reduce power dissipation significantly and eliminate the need for external Schottky diodes for most applications.

The synchronous rectification can be set in either active mode or disabled mode using the SR pin.

**Synchronous Rectification Mode (SR)**

When the SR input is logic-low, active mode is enabled and synchronous rectification will occur. Reversal of the current in the motor winding is prevented when using this mode by turning off synchronous rectification if the current in the winding decays to zero. When the SR input is logic-high, synchronous rectification is disabled. Synchronous rectification is typically disabled only when external diodes are required to transfer power dissipation from the A5977 package to the external diodes.

**Enable Input (ENABLEn)**

This active-low input enables all of the DMOS outputs. When logic-high, the outputs are disabled. Inputs to the translator (STEP, DIR, MS1, MS2) are all active independent of the ENABLEn input state.

**Sleep Mode (SLEEPn)**

This active-low input is used to minimize power consumption when the device is not in use. Sleep mode disables much of the internal circuitry, including the output DMOS, regulator, and charge pump. A logic-high allows normal operation and a rising edge on this input resets the translator to the home position. When coming out of sleep mode, 1 ms is required before issuing a STEP command, to allow the charge pump to stabilize.

**Charge Pump (CP1 and CP2)**

The charge pump is used to generate a gate supply greater than  $V_{BB}$  to drive the source-side DMOS gates. A 0.22  $\mu\text{F}$  ceramic capacitor is required between CP1 and CP2, and a 0.22  $\mu\text{F}$  ceramic capacitor is required between VCP and VBB. VCP is internally monitored, and in the case of a fault condition, the outputs of the device are disabled.

**VREG**

This internally generated voltage is used to operate the sink-side DMOS gates. The VREG terminal should be decoupled with a 0.22  $\mu\text{F}$  capacitor to ground. VREG is internally monitored, and in the case of a fault condition, the outputs of the device are disabled.

**Shutdown**

In the event of a fault (excessive junction temperature, or low voltage on VCP or VREG), the outputs of the device are disabled until the fault condition is removed. At power-up, and in the event of low  $V_{DD}$ , the undervoltage lockout (UVLO) circuit disables the drivers and resets the translator to the home position.

**Overcurrent Protection (OCP)**

If any FET's current exceeds  $I_{OCP}$  for longer than the blank time, all FETs are disabled for 1.6 ms.  $R_{SENSE}$  is not required for low-side OCP to function and the OCP threshold is independent of the  $R_{SENSE}$  value.

PHASE CURRENT DIAGRAMS

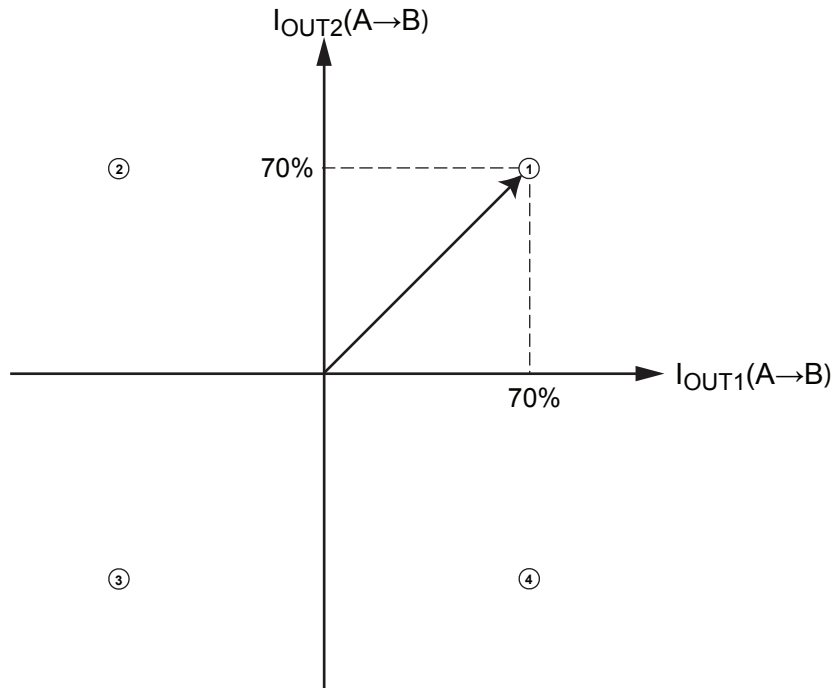


Figure 2: Full Step  
 MS2 = L, MS1 = L, DIR = H. See Table 2 for step number detail.

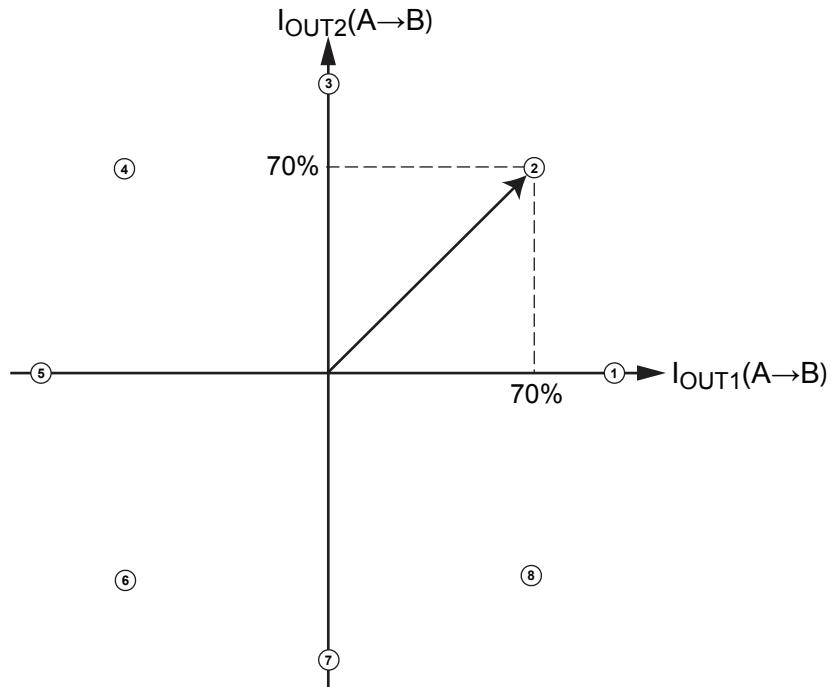
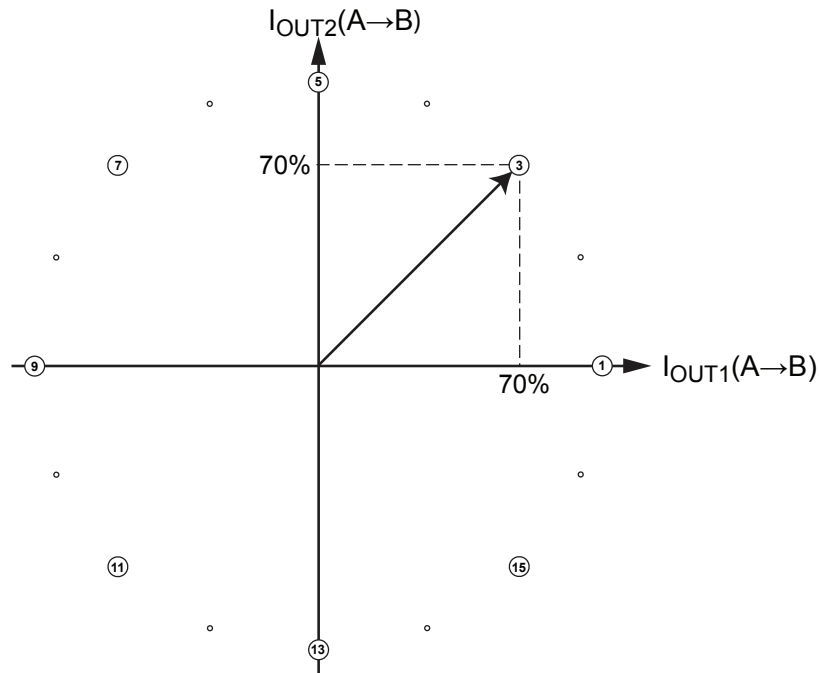
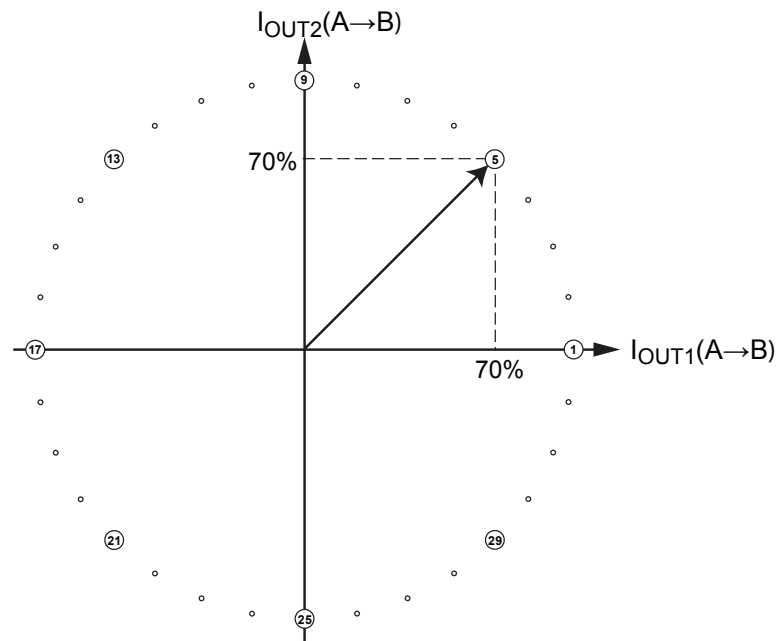


Figure 3: Half Step  
 MS2 = L, MS1 = H, DIR = H. See Table 2 for step number detail.



**Figure 4: Quarter Step**  
 MS2 = H, MS1 = L, DIR = H. See Table 2 for step number detail.



**Figure 5: Eighth Step**  
 MS2 = H, MS1 = H, DIR = H. See Table 2 for step number detail.

**Table 2: Step Sequencing Settings**

DIR = H; 360° = 4 full steps; home microstep position at step angle 45°

Full Step #	Half Step #	1/4 Step #	1/8 Step #	Phase 1 Current [% I <sub>tripMax</sub> ] (%)	Phase 2 Current [% I <sub>tripMax</sub> ] (%)	Step Angle (°)
	1	1	1	100.0	0.0	0.0
			2	98.1	19.5	11.3
		2	3	92.4	38.3	22.5
			4	83.1	55.6	33.8
<b>1*</b>	<b>2*</b>	<b>3*</b>	<b>5*</b>	<b>70.7*</b>	<b>70.7*</b>	<b>45.0*</b>
			6	55.6	83.1	56.3
		4	7	38.3	92.4	67.5
			8	19.5	98.1	78.8
	3	5	9	0.0	100.0	90.0
			10	-19.5	98.1	101.3
		6	11	-38.3	92.4	112.5
			12	-55.6	83.1	123.8
2	4	7	13	-70.7	70.7	135.0
			14	-83.1	55.6	146.3
		8	15	-92.4	38.3	157.5
			16	-98.1	19.5	168.8
	5	9	17	-100.0	0.0	180.0
			18	-98.1	-19.5	191.3
		10	19	-92.4	-38.3	202.5
			20	-83.1	-55.6	213.8
3	6	11	21	-70.7	-70.7	225.0
			22	-55.6	-83.1	236.3
		12	23	-38.3	-92.4	247.5
			24	-19.5	-98.1	258.8
	7	13	25	0.0	-100.0	270.0
			26	19.5	-98.1	281.3
		14	27	38.3	-92.4	292.5
			28	55.6	-83.1	303.8
4	8	15	29	70.7	-70.7	315.0
			30	83.1	-55.6	326.3
		16	31	92.4	-38.3	337.5
			32	98.1	-19.5	348.8

\* Home state; HOMEn output low.

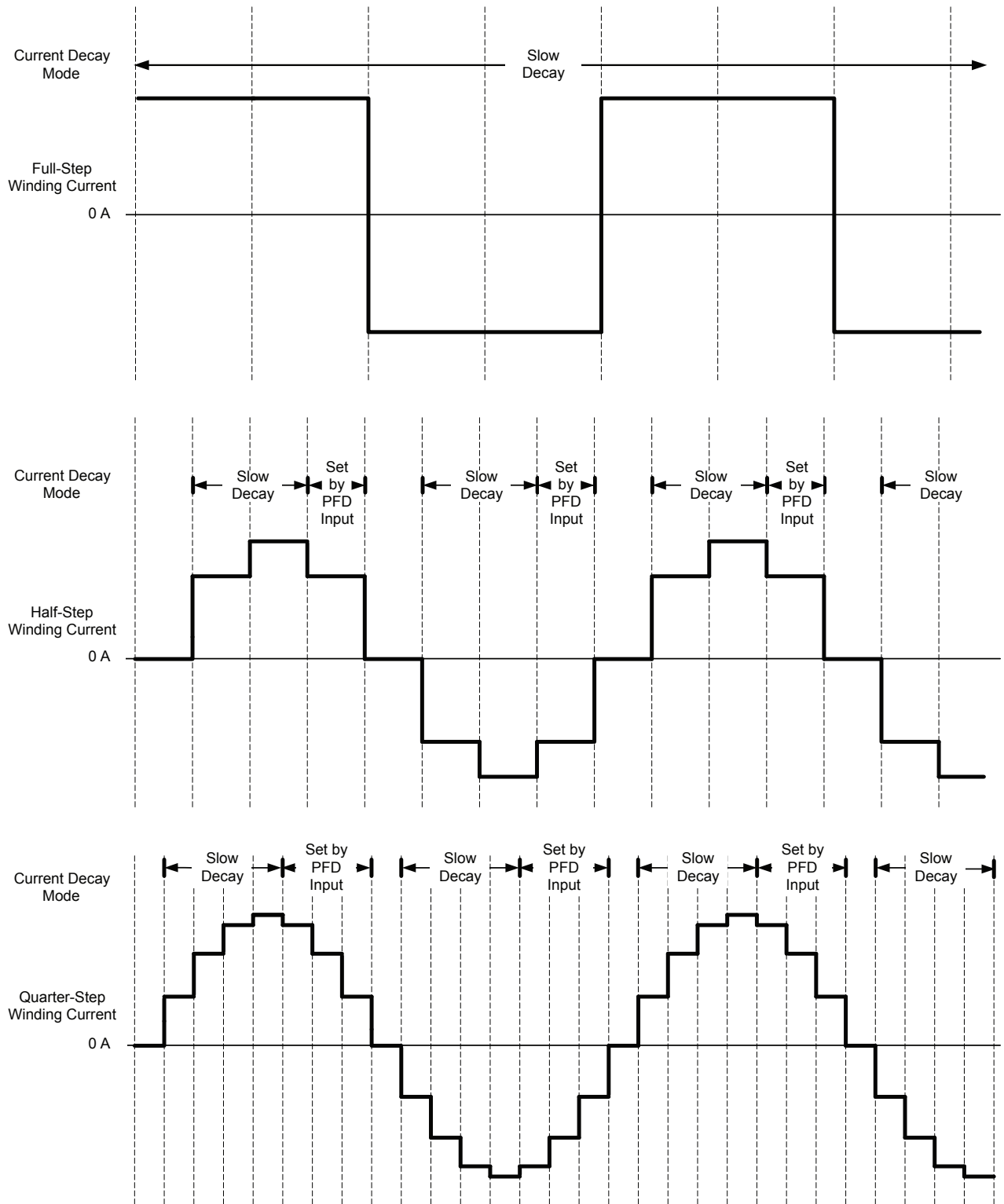
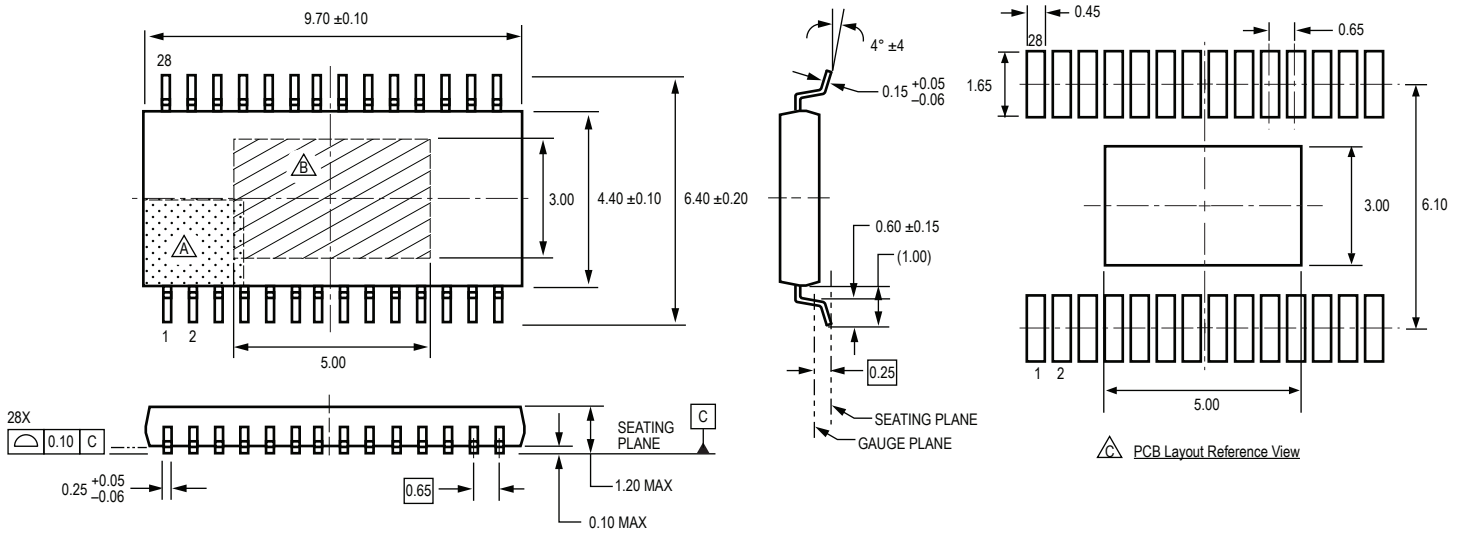


Figure 6: Automatic Decay Mode

PACKAGE OUTLINE DRAWING



For reference only  
 (reference JEDEC MO-153 AET)  
 Dimensions in millimeters  
 Dimensions exclusive of mold flash, gate burrs, and dambar protrusions  
 Exact case and lead configuration at supplier discretion within limits shown

- △ Terminal #1 mark area
- △ Exposed thermal pad (bottom surface)
- △ Reference land pattern layout (reference IPC7351 SOP65P640X120-29CM); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Figure 7: LP Package, 28-Pin TSSOP with Exposed Thermal Pad

**Revision History**

Revision	Current Revision Date	Description of Revision
–	December 21, 2015	Initial release
1	January 21, 2016	Corrected formula on page 8
2	May 31, 2016	Corrected setup and hold time units on page 7

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