EZ-PD™ PMG1-S3 Power Delivery MCU Gen1

EZ-PD™ PMG1 family general description

EZ-PD™ PMG1 (Power delivery MCU Gen1) is a family of high-voltage USB-C power delivery (PD) microcontrollers (MCU). These chips include an Arm® Cortex®-M0/M0+ CPU and USB-C PD controller along with analog and digital peripherals. EZ-PD™ PMG1 is targeted for any embedded system that provides/consumes power to/from a high-voltage USB-C PD port and leverages the microcontroller to provide additional control capability. **Figure 1** shows the EZ-PD™ PMG1 family segmentation.

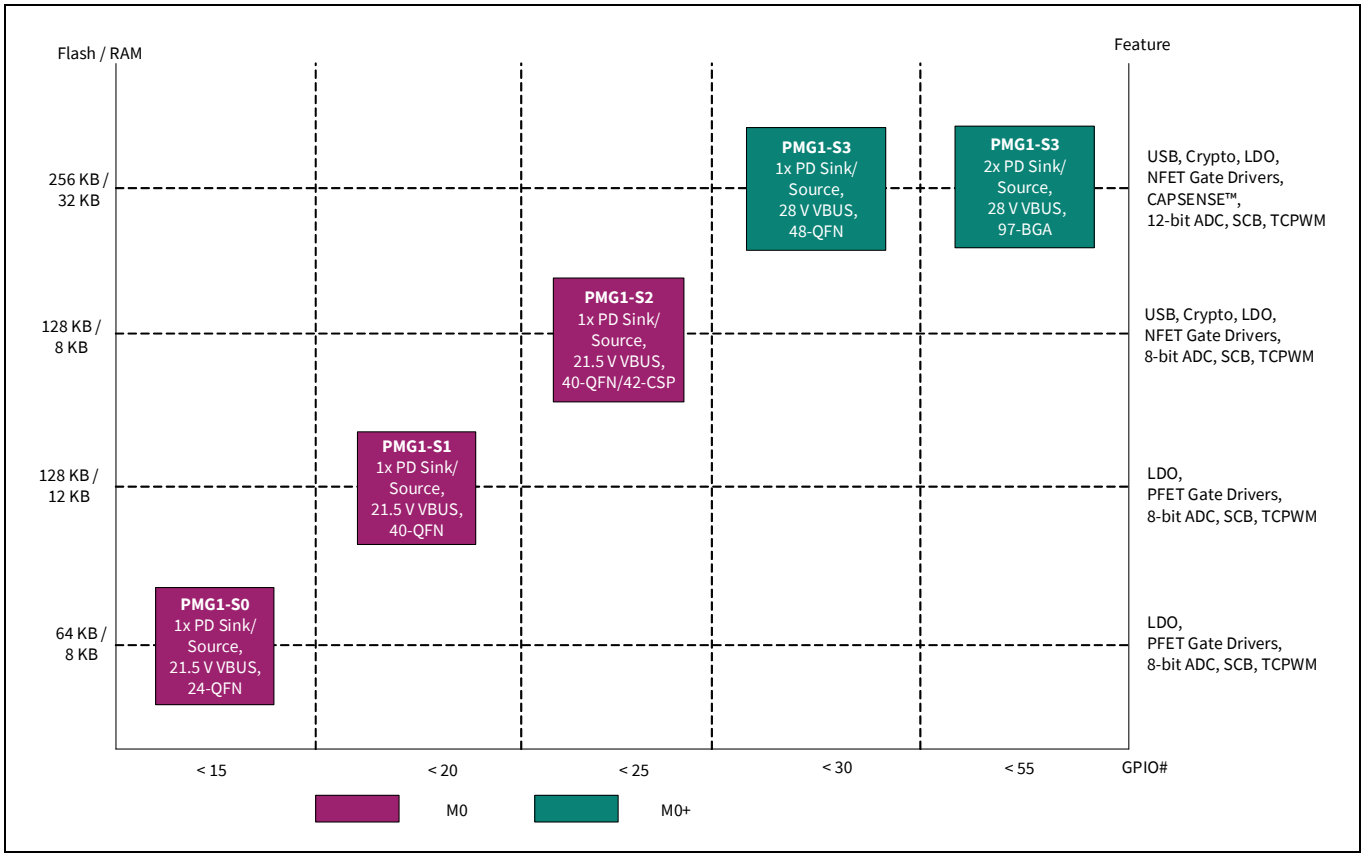


Figure 1 PMG1 family segmentation

Table 1 shows the comparison of features of different MCUs of the EZ-PD™ PMG1 family.

Table 1 Comparison of features of different EZ-PD™ PMG1 family MCUs

Subsystem or range	Item	PMG1-S0	PMG1-S1	PMG1-S2	PMG1-S3
CPU and memory subsystem	Core	Arm® Cortex®-M0	Arm® Cortex®-M0	Arm® Cortex®-M0	Arm® Cortex®-M0+
	Max. freq (MHz)	48	48	48	48
	Flash (KB)	64	128	128	256
	SRAM (KB)	8	12	8	32
Power delivery	Power delivery ports	1	1	1	1 port for 48-QFN 2 ports for 97-BGA
	Role	DRP	DRP	DRP	DRP
	MOSFET gate drivers	2x PFET	2x PFET	2x NFET	Flexible 2x NFET
	Fault protections	VBUS OVP, UVP, and OCP. SCP (for source configuration only)	VBUS OVP, UVP, and OCP. SCP and RCP (for source configuration only)	VBUS OVP, UVP, and OCP	VBUS OVP, UVP, and OCP. SCP and RCP (for source configuration only)
USB	Integrated full speed USB 2.0 device with Billboard class support	No	No	Yes	Yes
Voltage range	Supply (V)	VDDD (2.7–5.5) VBUS (4–21.5)	VSYS (2.75–5.5) VBUS (4–21.5)	VSYS (2.7–5.5) VBUS (4–21.5)	VSYS (2.8–5.5) VBUS (4–28)
	IO (V)	1.71–5.5	1.71–5.5	1.71–5.5	1.71–5.5
Digital	SCB (configurable as I2C/UART/SPI)	2	4	4	7 for 48-QFN (out of which only 5 can be configured as SPI and UART) 8 for 97-BGA
	TCPWM block (configurable as timer, counter or pulse width modulator)	4	2	4	7 for 48-QFN 8 for 97-BGA
	Hardware authentication block (Crypto)	No	No	Yes (AES-128/192/256, SHA1, SHA2-224, SHA2-256, PRNG, CRC)	Yes (AES-128, SHA2-256, TRNG, vector unit)
Analog	ADC	2x 8-bit SAR	1x 8-bit SAR	2x 8-bit SAR	2x 8-bit SAR 1x 12-bit SAR
	On-chip temperature sensor	Yes	Yes	Yes	Yes
Direct memory access (DMA)	DMA	No	No	No	Yes
GPIO	Max # of I/Os	12 (10+2 Fail-Safe)	17 (15+2 Fail-Safe)	20 (18+2 Fail-Safe)	26 (24+2 Fail-Safe) for 48-QFN 50 (48+2 Fail-Safe) for 97-BGA
Charging standard	Charging source	BC 1.2, AC, AFC and QC 3.0	BC 1.2, AC	BC 1.2, AC	BC 1.2, AC, AFC and QC 3.0
	Charging sink	BC 1.2, AC and QC 2.0	BC 1.2, AC	BC 1.2, AC	BC 1.2, AC and QC 2.0

Table 1 Comparison of features of different EZ-PD™ PMG1 family MCUs *(continued)*

Subsystem or range	Item	PMG1-S0	PMG1-S1	PMG1-S2	PMG1-S3
ESD protection	ESD protection	Yes (Human body model and charged device model)	Yes (Human body model and charged device model)	Yes (Human body model and charged device model)	Yes (Human body model and charged device model)
Packages	Package options	24-QFN (4 × 4 mm, 0.5 mm pitch)	40-QFN (6 × 6 mm, 0.5 mm pitch)	40-QFN (6 × 6 mm, 0.5 mm pitch) / 42-CSP (2.63 × 3.18 mm, 0.4 mm pitch)	48-QFN (6 × 6 mm, 0.5 mm pitch) / 97-BGA (6 × 6 mm, 0.5 mm and 0.65 mm pitch)

The rest of this document discusses EZ-PD™ PMG1-S3 device in detail.

EZ-PD™ PMG1-S3 general description

EZ-PD™ PMG1-S3 expands the PMG1 family with 256 KB flash, 32 KB SRAM, 50 GPIOs, Full-speed USB device controller, a Crypto engine for authentication, analog resources (ADC, opamps, comparators, CAPSENSE™), and dual Type-C PD ports. It is targeted for device, dock, and accessory applications and is available in QFN and BGA packages.

Features

- **32-bit MCU subsystem**
- **48-MHz Arm® Cortex®-M0+ CPU with DMA**
- **Memory**
  - 256 KB flash
  - 32 KB SRAM
  - 96 KB ROM with PD code
- **Type-C/PD blocks**
  - Up to two Type-C/PD blocks each with a baseband transceiver
  - Two pairs of integrated VBUS NFET gate drivers
  - Slew rate control to limit the inrush current on the gate drivers configured to be used in VBUS provider or consumer path
  - Integrated USB power-delivery (USB-PD) 3.1 support
  - Supports 28 V extended power range (EPR)
  - High-voltage (28 V) regulator and VBUS discharge
  - Configurable VBUS overvoltage protection (OVP), overcurrent protection (OCP), short-circuit protection (SCP) and reverse-current (RCP) protection
  - VCONN FETs with OCP
  - Two integrated 3:1 SBU analog muxes for alternate modes (Display Port and Thunderbolt) on the 97-BGA part
- **Interfaces**
  - Up to eight run-time reconfigurable serial communication blocks (SCBs) configurable as I^2C, SPI or UART
  - Up to eight timer/counter pulse-width modulators (TCPWMs)
- **Programmable GPIO pins**
  - Up to 50 GPIO pins
  - Any GPIO pin can be CAPSENSE™, analog, or digital
  - Programmable drive modes, strengths, and slew rates
- **Integrated analog blocks**
  - Two 8-bit SAR ADCs
  - One 12-bit SAR ADC
  - Two opamps
  - Two LP comparators
- **Capacitive sensing**
  - CAPSENSE™ sigma-delta (CSD) provides best-in-class signal-to-noise ratio (SNR) (>5:1) and water tolerance
  - Infineon™-supplied software component makes capacitive sensing design easy
  - Automatic hardware tuning (SmartSense)
- **Hardware crypto engine for secure FW boot and signed FW update**
- **USB full-speed device**
- **Charger detect block**

- **Power**
  - VSYS (2.8 V to 5.5 V)
  - VBUS (4 V to 28 V)
  - Independent supply voltage pin for GPIO that allows 1.71 V to 5.5 V signaling on the I/Os
- **Packages**
  - 48-QFN
  - 97-BGA
- **Software tool**
  - ModusToolbox™

Block diagram

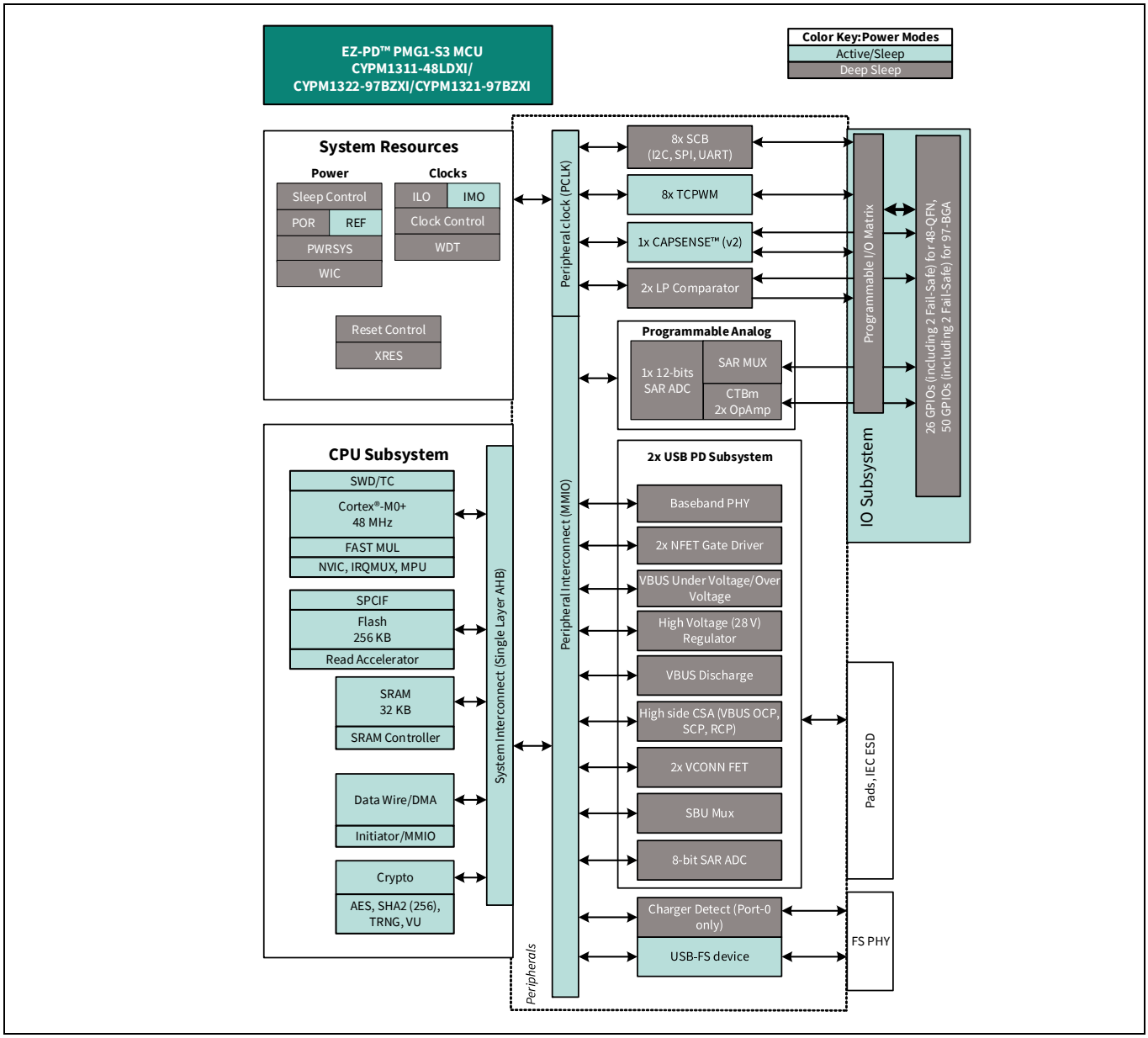


Table of contents

1 Development support

The EZ-PD™ PMG1 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit **www.infineon.com/products/ez-pd-pmg1** to find out more.

1.1 Documentation

A suite of documentation supports the EZ-PD™ PMG1 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software user guide: A step-by-step guide for using ModusToolbox™ (MTB). The software user guide shows you how MTB build process works in detail, how to use source control with MTB, and much more.

Component datasheets: The flexibility of EZ-PD™ PMG1 allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all the information needed to select and use a particular component, including functional description, API documentation, example codes, and AC/DC specifications.

Application notes: This includes the Getting Started application note and the hardware design guidelines.

Technical reference manual: The technical reference manual (TRM) contains all the technical detail you need to use a EZ-PD™ PMG1 device, including a complete description of all EZ-PD™ PMG1 registers. The TRM is available in the Documentation section at **www.infineon.com/products/ez-pd-pmg1**.

1.2 Online

In addition to print documentation, the **EZ-PD™ PMG1 forums** connect you with fellow users and experts in PMG1 from around the world, 24 hours a day, 7 days a week.

1.3 Tools

Withthe industry standard cores, programming, and debugging interfaces, the EZ-PD™ PMG1 family is part of a development tool ecosystem.

Visit us at **https://www.infineon.com/products/modustoolbox-software-environment** for the latest information on the revolutionary, easy to use ModusToolbox™ IDE, supported third party compilers, programmers, debuggers, and development kits.

1.4 ModusToolbox™ IDE and the EZ-PD™ PMG1 SDK

ModusToolbox™ is an Eclipse-based development environment on Windows, macOS, and Linux platforms that includes the ModusToolbox™ IDE and the EZ-PD™ PMG1 SDK. The ModusToolbox™ IDE brings together several device resources, middleware, and firmware to build an application. Using ModusToolbox™, you can enable and configure device resources and middleware libraries, write C/C++/assembly source code, and program and debug the device.

The PMG1 SDK is the software development kit for the EZ-PD™ PMG1 MCU. The SDK makes it easier to develop firmware for supported devices without the need to understand the intricacies of the device resources.

For additional details on using the ModusToolbox™, refer to the **Getting started with EZ-PD™ PMG1 MCU on Modus Toolbox™** application note and the documentation and help integrated into ModusToolbox™. As **Figure 2** shows, with the ModusToolbox™ IDE, you can:

1. Create a new application based on a list of template applications, filtered by kit or device, or browse the collection of code examples online.
2. Configure device resources in Device Configurator to build your hardware system design in the workspace.
3. Add software components or middleware.
4. Develop your application firmware.

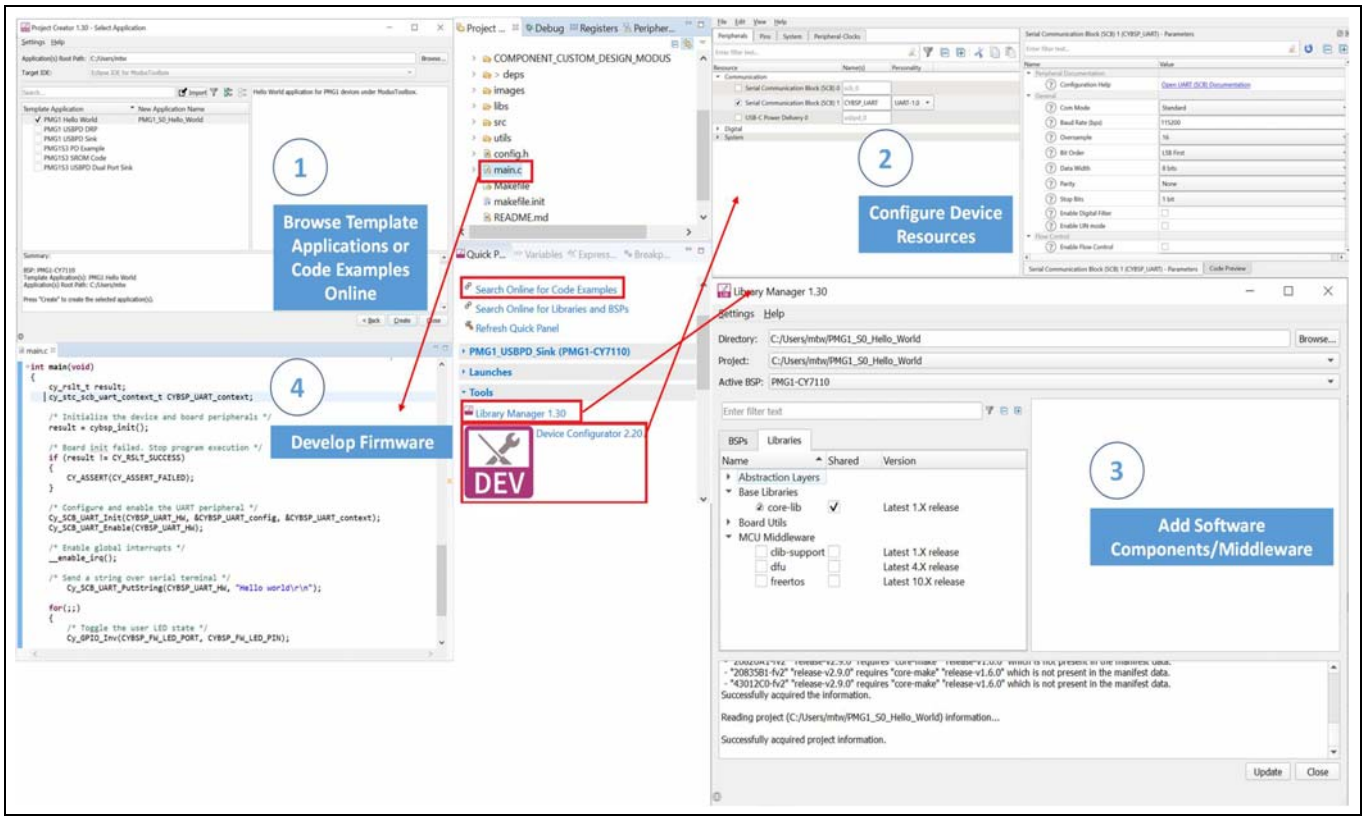


Figure 2 ModusToolbox™ IDE resources and middleware

2 Functional overview

2.1 CPU and memory sub-system

2.1.1 CPU

The Cortex®-M0+ in the PMG1-S3 is a 32-bit MCU which is optimized for low power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. The infineon implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a wakeup interrupt controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode.

The CPU sub-system also includes a 16-channel DMA/Datawire block and a serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for PMG1-S3 has four break-point (address) comparators and two watchpoint (data) comparators.

2.1.2 Flash

The PMG1-S3 has a 256-KB (2x 128 KB) Flash module.

2.1.3 SRAM

32-KB of SRAM which is retained during Deep Sleep is provided.

2.1.4 ROM

96-KB of supervisory ROM that contains boot and configuration routines is provided. In addition to the flash erase and program routines provided for PMG1-S3, the SROM also contains flash checksum routines.

2.1.5 Cryptographic accelerator

The Crypto accelerator block supports below requirements:

- Vector unit (VU) to support asymmetric key cryptography.
- SHA2 (256-bit)
- Vector unit for asymmetric cryptography capable of performing RSA-4096, 3072, ECC-256
- AES (128-bit) supports forward block cipher
- True random number generator (AIS-31-compliant)
- Performance @ 48 MHz
  - RSA-3072 verify performance: 25 ms
  - SHA-2 256-bit over 64 KB: 10 ms
  - Secure boot transfer control to user program in 50 ms
- Public-Key storage
  - Flash: 2KB RSA-3072 key-structure stored in flash. The key-structure includes modulus, exponent and three coefficients

2.2 System resources

2.2.1 Power system

Power system is described in detail in **"Power systems overview"** on page 17. It provides assurance that voltage levels are as required for each respective mode and will either delay mode entry (on power-on reset (POR) for instance) until voltage levels are as required for proper function or will generate resets (brown-out detection (BOD)) if operation under unsafe power supply levels is imminent. PMG1-S3 can operate with a single external supply over the range of 2.8 V to 5.5 V (VSYS) or 4 V to 28 V (VBUS) and has three different power modes (Active, Sleep, Deep Sleep), transitions between which are managed by the power system.

The PMG1-S3 power system is designed for 60 mA capability based on internal peripherals. When operating on a 28 V regulator, depending on the package and VBUS supply value, ensure that you limit the current consumption (by turning OFF peripherals) and ensure that the die T_{JA} does not exceed 125°C.

2.2.2 Clock system

The clock system for PMG1-S3 is a strict subset of the M0S8 platform. PMG1-S3 has a fully integrated clock and hence does not require an external crystal. The clock system is responsible for providing clocks to all sub-systems that require clocks (SCB, TCPWM, programmable analog sub-system (PASS) and PD) and for switching between different clock sources without glitches. In addition, it must ensure that no metastable conditions occur.

Figure 3 illustrates the PMG1-S3 clock system which consists of the internal main oscillator (IMO) and the internal low-power oscillator (ILO). PERXYZ_CLK represents the clocks for different peripherals.

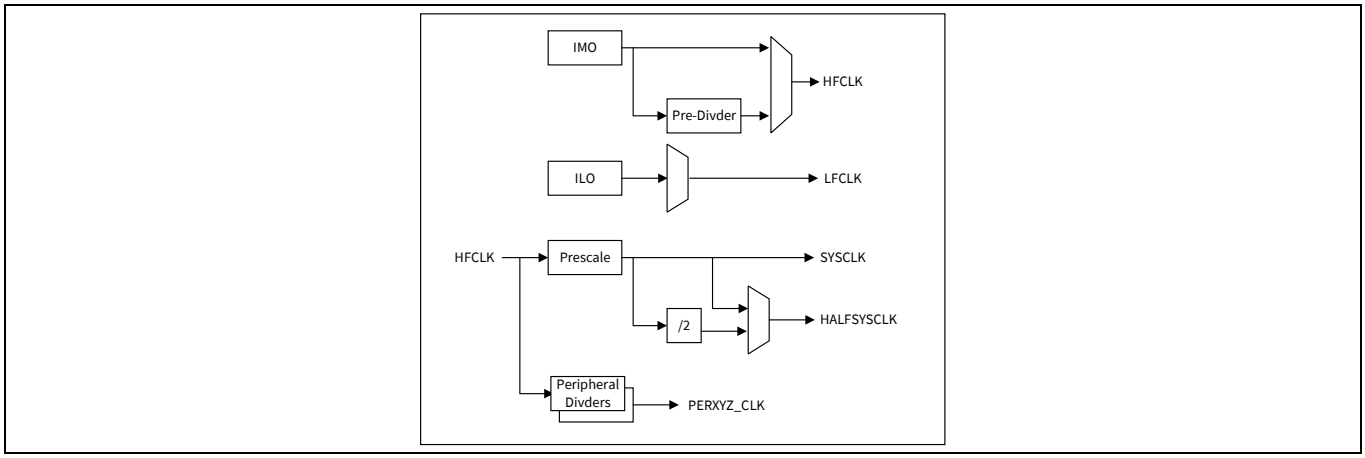


Figure 3 Clocking architecture of PMG1-S3

The HFCLK signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are 21 clock dividers for PMG1-S3 (5 with fractional divide and 16 with integer divide capability). The analog clock leads the digital clocks to allow analog events to occur before digital clock-related noise is generated. The digital clock dividers generate enabled clocks (i.e., 1 in N clocking where 'N' is the divisor). The analog clock divider needs to provide a true 50% duty to maintain analog performance at all allowed frequencies.

IMO clock source

The IMO is the primary source of internal clocking in PMG1-S3. It is trimmed during production to achieve the desired accuracy of ±2%. Trim values are stored in supervisory rows in the flash memory. Additional trim settings from flash can be used to compensate for changes. The IMO default frequency is 48 MHz ±2%. IMO RMS jitter allows 12-bit SAR accuracy.

ILO clock source

The ILO is a very low power, relatively inaccurate, oscillator, which is primarily used to generate clocks for peripheral operation in USB Suspend (Deep Sleep) mode. It is a 40 kHz oscillator with untrimmed accuracy of –50 to +100% and it is capable of being trimmed within ±55%.

2.2.3 Watchdog timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the timeout occurs. The timer can be used to generate interrupts if required in addition to generating resets.

2.2.4 Reset

The PMG1-S3 can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register which is sticky through reset and allows software to determine the cause of the reset. A pin (XRES) is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration.

2.2.5 Voltage reference

The PMG1-S3 reference system generates all internally required references. To allow better signal to noise ratios (SNR) and better absolute accuracy, it is possible to bypass the internal reference using a GPIO pin or to use an external reference for the 12-bit SAR ADC. The internal reference at the pin may be buffered by using one of the on-chip opamps and used as an external reference.

2.3 Analog blocks

2.3.1 12-bit SAR ADC

The 12-bit 1 MS/second SAR ADC operates at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion. The ADC clock input is derived by dividing the CPU clock rate by an integer value. This means that at 48 MHz CPU clock rate, the highest allowable clock rate for the ADC is 16 MHz. The 16 MHz clock rate allows 10-bit conversions to be performed at 1 MS/second (a 10-bit conversion takes a minimum of 16 clocks). Using integer dividers also means that 12-bit ADC performance is 890 samples/s at 48 MHz and its peak of 1 MS/s is at 18 or 36 MHz. The ADC requires an approximately 50% duty cycle clock and this is provided for all integer divider values.

The block functionality is augmented for the user by adding a reference buffer to it and by providing the choice of three internal voltage references: VDDA, VDDA/2, and internal bandgap reference (nominally 1.2 V) as well as an external reference through a GPIO pin. The sample-and-hold (S/H) aperture is programmable allowing the Gain-bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed allowing less expensive external opamps to be used. System performance is 68 dB for true 12-bit precision provided appropriate references are used. In particular, it is possible to provide an external bypass (via P3.0: sar_ext_vref pin) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through selected channels autonomously (sequencer scan) and does so with zero switching overhead (i.e. aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. In order to accommodate signals with varying source impedance and frequency it is possible to have different sample times programmable on a per-channel basis. Also, signal range specification via a pair of range registers (LOW and HIGH range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR includes multiple sample averaging capability in order to save CPU bandwidth. It digitizes the output of the on-board temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep mode as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 5.5 V. When the supply voltage VDDA is less than 4 V, boost-pump must be enabled to maintain the performance.

2.3.2 Continuous time block mini (CTBm)

PMG1-S3 has one CTBm block which consists of two opamps. The inputs and outputs of the opamps are connected to fixed pins and they have three power modes (low, medium, high) and three operational modes (comparator, follower, opamp). The outputs can be used as buffers for the SAR inputs. The CTBm block, when accessed from the IO pins on port 3, provides full features. It can also be connected to other user-preferred pins via the analog multiplexer buses. The block can also be turned OFF (power-switched) to save power when not being used. It can also be operated in Deep Sleep mode in order to allow fast analog system start-up after Deep Sleep. The opamps are trimmable to achieve better than 1 mV offset voltage.

2.3.3 Temperature sensor

PMG1-S3 has an on-chip temperature sensor which consists of a diode biased by a current source that can be disabled to save power. The diode is calibrated during production to achieve ±5% maximum deviation from accuracy (typical ±1%). Since the measured temperature is the on-chip temperature of the diode, the diode is placed in close proximity to the SAR ADC to allow more accurate measurement.

2.3.4 Low-power comparators

PMG1-S3 has a pair of low-power comparators which can operate in the Deep Sleep mode. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels duringLow-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode (Deep Sleep) where the system wake-up circuit is activated by a comparator switch event. It is possible to route the comparator outputs to pins in order to be able to use the comparator outputs without synchronization or gating for the purposes of implementing control loops (such as hysteretic control).

2.3.5 Analog multiplexed buses

PMG1-S3 has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources (SAR ADCs, comparator, CSD, and Op-Amps) to connect to any pin on the I/O Ports. The two amux can also be split in 3 to isolate CSD, ADC and GPIO connectivity.

2.4 USB-PD sub-system

This sub-system provides the interface to the Type-C USB port.

2.4.1 USB-PD physical layer

The USB-PD sub-system contains the USB-PD physical layer block and supporting circuits. The physical layer consists of a transmitter and receiver that communicate BMC encoded data over the CC as per the PD 3.1 standard All communication is half-duplex. The physical layer or PHY practices collision avoidance to minimize communication errors on the channel.

2.4.2 VCONN FET

PMG1-S3 has two integrated VCONN FETs to power either CC1 or CC2 pins. There is a power supply input VCONN_Source pin for providing power to EMCA cables through these VCONN FETs. The FETs can provide 1.5W power per port over the valid VCONN range of 4.85 V to 5.5 V on the CC1/2 pins for EMCA cables. At any given time, only one of the VCONN FETs is ON.

2.4.3 8-bit SAR ADC

The 8-bit SAR ADC is a low-footprint ADC available for general purpose A-D conversion applications in the chip. The ADC can be accessed from all the GPIOs through the on-chip analog mux by closing appropriate firmware-controlled splitters. In PMG1-S3, one ADC is instantiated per PD port.

2.4.4 SBU mux

The 97-BGA package of PMG1-S3 contains a set of analog switches to connect SBU1 and SBU2 pins of the Type-C connector to AUX pins of DisplayPort or LSX pins of Thunderbolt. The SBU pins and LSTX/RX pins, SBU pins and UART debug (DBG), LSTX/RX pins and UART debug pins are multiplexed digitally as shown in **Figure 4**. Two sets of comparators connected to the SBU lines provide the SBU signal detection based on the specified reference voltage.

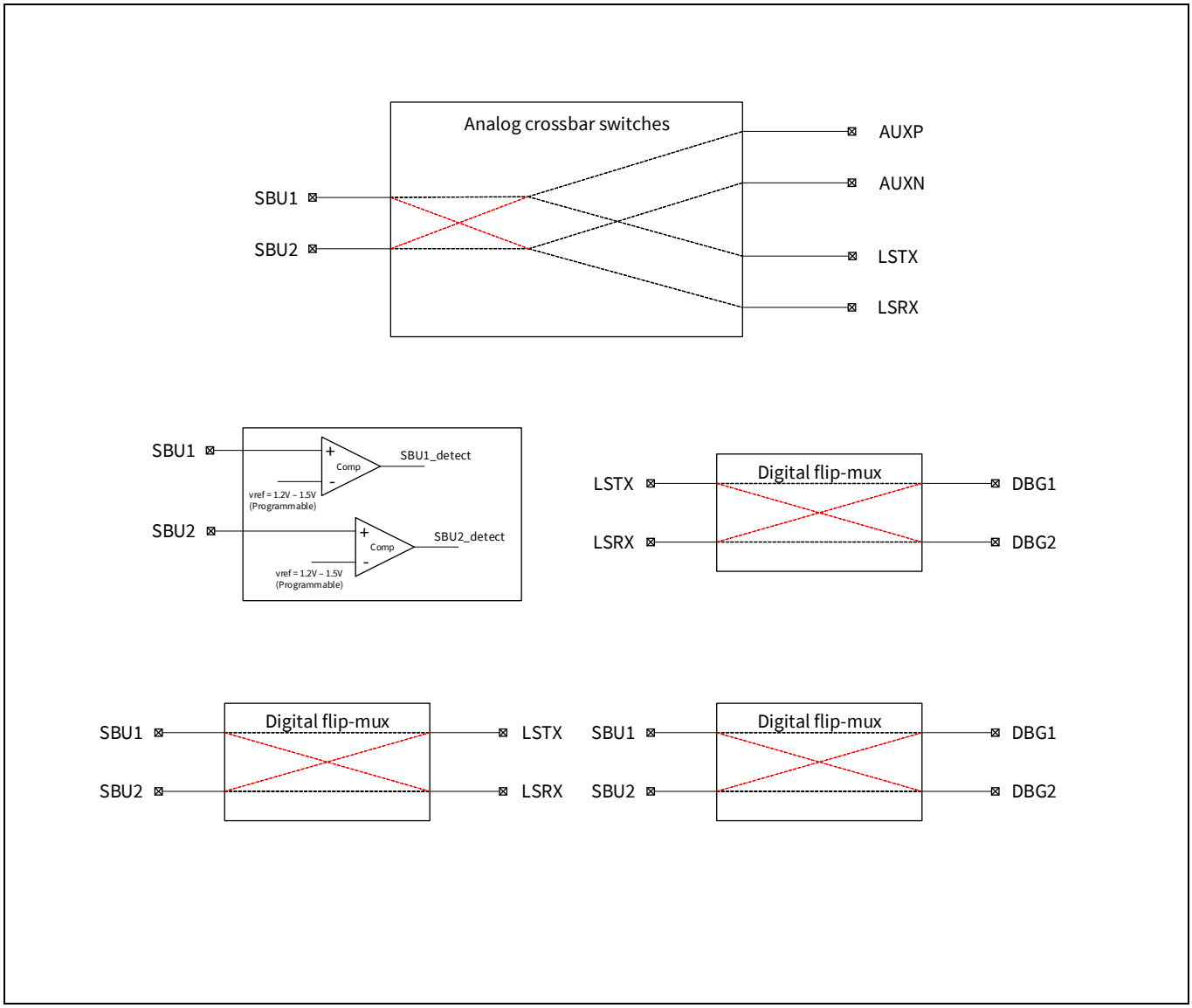


Figure 4 SBU mux

2.4.5 Load switch controller

PMG1-S3 has an integrated load switch controller with the following functions.

Overvoltage and undervoltage protection on VBUS

The chip implements an under-voltage/over-voltage (UVOV) detection circuit for the VBUS supply. The thresholds for both UV and OV are programmable.

Over current, short-circuit current and reverse current fault detection comparators for VBUS

The chip supports the detection of over current, short-circuit current and reverse current faults in the VBUS provider path. External resistor (5 mΩ) placed in connector VBUS path connects to the chip, the drop across this resistor is monitored to detect these faults. PMG1-S3 restricts reverse current to 400mA on VBUS provider path when Type-C VBUS is greater than VIN (provider voltage before the VBUS NFET). PMG1-S3 reacts quickly and turns off the VBUS provider NFET. This feature is not supported on consumer path and there will be reverse current whenever the consumer side voltage is higher than connector side voltage on the consumer path.

VBUS discharge

PMG1-S3 has an integrated high-voltage (28 V) VBUS discharge circuitry. After cable removal detection, the chip will discharge the residual charge and bring the floating VBUS back to vSafe0V.

VBUS regulator

The chip has up to three input power supplies – VSYS and VBUS_C (Port0 and Port1). A regulator operating on these power supplies will derive the chip operating supply. The VSYS always takes priority over VBUS. In absence of VSYS, the regulator powers the chip from VBUS (Port0 or Port1 whichever is present). VBUS regulators do not provide any inrush current protection, and can supply a maximum of 60 mA of current.

Flexible gate drivers for VBUS NFETs

PMG1-S3 has two pairs of integrated gate drivers to drive external NFETs. These are flexible gate drivers i.e., they are independent of provider or consumers paths and can be configured as needed on either port. Once these are configured either as provider/consumer, for a given board/application, the functionality cannot be changed without a board-re-spin. These gate-drivers support only external NFET and these NFETs must be capable of supporting max VGS of ±VBUS_NGDO_MAX. These gfate-drivers do not support FRS feature.

2.5 USB2.0 full speed device and charger detection

PMG1-S3 has one USB 2.0 FS device to support billboard class, and HID class applications for firmware download. The charger detection block connected to the DP/DM pins allows PMG1-S3 to detect conventional battery chargers conforming to BC 1.2, Apple Charger, QC3.0 and AFC specifications. The AFC protocol is supported for source mode only.

2.6 Fixed-function digital

2.6.1 Timer/counter/PWM block

The timer/counter/PWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register which is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead-band programmable complementary PWM outputs. It also has a kill input to force outputs to a pre-determined state; this is used in motor drive systems for instance when an over-current state is indicated and the PWMs driving the FETs need to be shut-off immediately with no time for software intervention.

PMG1-S3 has up to eight TCPWMs. They can be used as internal timers by firmware or for providing PWM based functions on the GPIOs.

2.6.2 SCB

PMG1-S3 has eight SCB blocks that can be configured for I2C, SPI, or UART. These blocks implement full multi-master and slave I2C interfaces capable of multi-master arbitration. I2C is compatible with the standard Philips I2C specification v3.0. These blocks operate at speeds of up to 1 Mbps and have flexible buffering options to reduce interrupt overhead and latency for the CPU.

The SCB blocks support 8-deep FIFOs for Receive (RX) and Transmit (TX), which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time. The FIFO mode is very useful in the absence of DMA. Data throughput is not a critical consideration for I2C. Only the I2C port of SCB0 is fail-safe. I2C ports for SCB1–7 are not fail-safe because, a high logic level on these GPIOs can back-power the MCU.

UART mode: This is a full-feature UART operating at up to 1 Mbps. In addition, it supports the 9-bit multi-processor mode which allows address of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported.

SPI mode: The SPI mode supports full Motorola SPI as well as TI SSP (essentially adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI) variants. The SPI block can also utilize the FIFO.

2.6.3 GPIO interface

The PMG1-S3 has up to 50 GPIOs including the SCB and SWD pins which can also be used as GPIOs.

The GPIO block implements the following:

- Eight drive strength modes including strong push-pull, resistive pull-up and pull-down, weak (resistive) pull-up and pull-down, open drain and open source, input only, and disabled.
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output disables.
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode).
- Selectable slew rates for dV/dt related noise control.

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity. Data output registers and pin state registers store, respectively, the values to be driven on the pins and the states of the pins. The configuration of the pins can be done by programming of registers through software for each digital I/O Port.

Every I/O pin can generate an edge-triggered interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it.

The I/O ports can retain their state during Deep Sleep mode or remain ON. If operation is restored using reset, then the pins go the High-Z state. If operation is restored by an interrupt event, then the pin drivers retain their state until firmware chooses to change it. The I/Os (on data bus) do not draw current on power down.

GPIO power domain

All the GPIOs reside in a separate I/O power domain called VDDIO (with exception of SBU GPIO). The separate I/O power domain provides flexible system-level interfacing. GPIOs connected to SBU (connector side) are on the VDDD domain and not on the VDDIO domain.

Table 50 lists the number of GPIOs on VDDIO and VDDD domains in 48-QFN and 97-BGA. In 97-BGA, out of the 38 GPIOs on VDDIO, a total of 26 GPIOs (Port-1(only LP-Comp Inputs), Ports 2, 3 and 5) are used by special analog peripheral blocks such as CTBm, 12-bit SAR ADC, CAPSENSE™ inputs and LPCOMP. For these GPIOs, ensure the following:

1. Voltage applied externally or routed internally to the I/O must not exceed the VDDIO supply (as VDDIO ≤ VDDA)
2. At start-up, an external voltage can be applied on these I/Os only after all supplies (VDDIO, VDDD, and VDDA) are up.

For all 50 GPIOs in 97-BGA, the voltages on AMUXBUSA and AMUXBUSB lines cannot be more than VDDA supply.

2.6.3.1 Fail-Safe GPIOs

EZ-PD™ PMG1-S3 has two pins which are fail-safe GPIOs. These are P4.0 and P4.1, which are the I2C pins for SCB0. The fail-safe feature ensures that, in the absence of VBUS/VSYS power, a logic high level on these pins due to I2C line activity will not back-power the MCU.

2.7 Special function peripherals

2.7.1 CAPSENSE™

CAPSENSE™ is supported on 16 pins in PMG1-S3 via a CAPSENSE™ sigma-delta (CSD) block that can be connected to any pin via the analog mux buses that any GPIO pin can be connected to. CAPSENSE™ function can thus be provided on any pin or group of pins in a system under software control.

The CAPSENSE™ block has two IDACs, which may be used for general purposes if CAPSENSE™ is not being used. Having two AMUX buses allows CAPSENSE™ to use one of the IDACs (without waterproofing) while the other one is available for general-purpose use.

Shield drive for water tolerance is provided using the second IDAC to drive the shield in order to keep the parasitic capacitance at the same charge level during sensing. The CAPSENSE™ blocks provide both self as well as mutual capacitance sensing.

3 Power systems overview

Figure 5 illustrates the general requirements for power pins on PMG1-S3. PMG1-S3 power scheme allows different VDDD and VDDA connections. There are no sequencing requirements. **Figure 5** is intended to show that VDDD and VDDA are separate nets which are not ohmically connected on chip. Depending on different package requirements, these may be connected together in the bonding arrangement or required to be connected off chip.

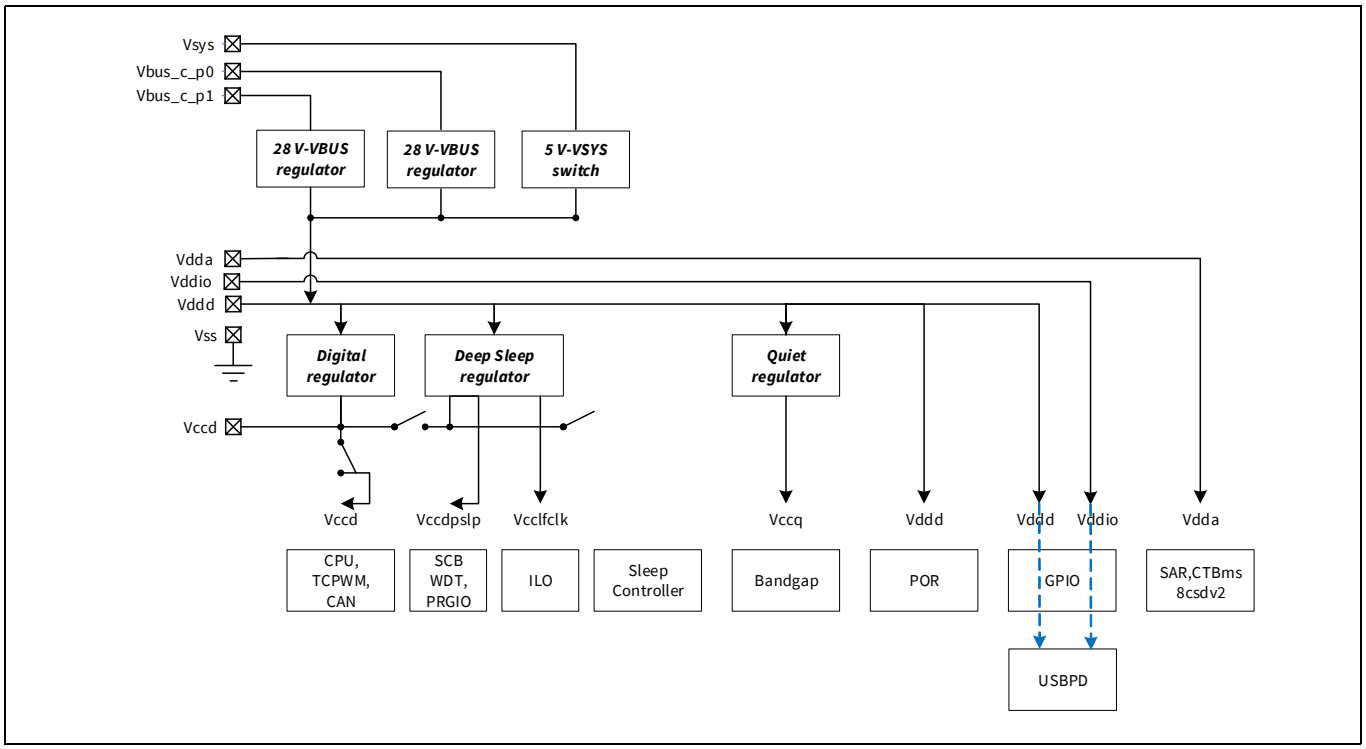


Figure 5 PMG1-S3 power system block diagram

4 Pinouts

Table 2 Pin list for PMG1-S3 CYPM132x-97BZXI and CYPM1311-48LDXI

Group	97-BGA	48-QFN	Pin name	Alternate functions (HSIOM_PORT_SEL)								Pin description
				Analog	ACT#0	ACT#1	ACT#2	ACT#3	DS#0	DS#2	DS#3	
GPIO	H2		P1.0	–	–	–	–	–	–	–	–	GPIO, CSD
	P3	12	P1.1	lpcomp1_inp	–	–	scb3_uart_rx	–	swd_clk	scb3_spi_clk	scb3_i2c_scl	GPIO, COMP1, SCB3, CSD, serial wire debug clock
	R3	13	P1.2	lpcomp1_inn	–	–	scb3_uart_tx	–	swd_data	scb3_spi_miso	scb3_i2c_sda	GPIO, COMP1, SCB3, CSD, serial wire debug data
	K4	14	P1.3	–	tcpwm4_line	tcpwm4_compare_match	scb3_uart_cts	tcpwm4_tr_in	–	scb3_spi_mosi	–	GPIO, SCB3, TCPWM4, CSD, thunderbolt interrupt PD port-0
	M10	20	P1.4	–	tcpwm5_line	tcpwm5_compare_match	scb3_uart_rts	tcpwm5_tr_in	–	scb3_spi_select	–	GPIO, SCB3, TCPWM5, CSD, hot plug detect PD port-0
	M12	21	P1.5	lpcomp0_inn	–	–	scb1_uart_tx[1]	–	–	scb1_spi_miso	scb1_i2c_sda	GPIO, COMP0, SCB1, CSD
	K12	22	P1.6	lpcomp0_inp	ext_clk0	–	–	–	–	scb1_spi_clk	scb1_i2c_scl	GPIO, COMP0, SCB1, CSD, external clock input
	A2		P2.0	sarmux_0	–	–	scb5_uart_rts	–	–	scb5_spi_select	–	GPIO, SAR input, SCB5, CSD
	B2	48	P2.1	sarmux_1	tcpwm2_line	tcpwm2_compare_match	scb0_uart_rts	tcpwm2_tr_in	–	scb0_spi_select	–	GPIO, SAR input, TCPWM2, SCB0, CSD
GPIO	A3	47	P2.2	sarmux_2	–	–	scb5_uart_tx[1]	–	–	scb5_spi_miso	scb5_i2c_sda	GPIO, SAR input, SCB5, CSD
	B5	46	P2.3	sarmux_3	–	–	scb5_uart_rx[1]	–	–	scb5_spi_clk	scb5_i2c_scl	GPIO, SAR input, SCB5, CSD
	A7	45	P2.4	sarmux_4	tcpwm3_line	tcpwm3_compare_match	scb0_uart_cts	tcpwm3_tr_in	–	scb0_spi_miso	–	GPIO, SAR input, TCPWM3, SCB0, CSD
	A5		P2.5	sarmux_5	–	–	scb5_uart_cts	–	–	scb5_spi_mosi	–	GPIO, SAR input, SCB5, CSD
	B7		P2.6	sarmux_6	–	–	scb1_uart_rts	–	–	scb1_spi_mosi	–	GPIO, SAR input, SCB1, CSD
	A8		P2.7	sarmux_7	–	–	scb1_uart_cts		–	scb1_spi_select	–	GPIO, SAR input, SCB1, CSD
	A1	1	P3.0	sar_ext_vref ctb0_oa1+	tcpwm6_line	tcpwm6_compare_match	scb4_uart_cts	tcpwm6_tr_in	–	scb4_spi_mosi	–	GPIO, CTBm, TCPWM6, SCB4, CSD
	B3		P3.1	ctb0_oa0+	–	–	–	–	–	–	–	GPIO, CTBm, CSD
	C2		P3.2	ctb0_oa1+	–	–	–	–	–	–	–	GPIO, CTBm, CSD

Notes
1. Not available in 48-QFN package.
2. I/O logic is connected to VDDD instead of VDDIO.

Table 2 Pin list for PMG1-S3 CYPM132x-97BZXI and CYPM1311-48LDXI *(continued)*

Group	97-BGA	48-QFN	Pin name	Alternate functions (HSIOM_PORT_SEL)								Pin description
				Analog	ACT#0	ACT#1	ACT#2	ACT#3	DS#0	DS#2	DS#3	
GPIO	B1	2	P3.3	ctb0_oa1-	tcpwm7_line	tcpwm7_compare_match	scb4_uart_rts	tcpwm7_tr_in	-	scb4_spi_select	–	GPIO, CTBm, TCPWM7, SCB4, CSD
	D4		P3.4	ctb0_oa1_out_10x	–	–	–	–	–	–	–	CTBm, GPIO, CSD
	F4	3	P3.5	ctb0_oa0_out_10x	–	–	scb4_uart_rx	–	–	scb4_spi_clk	scb4_i2c_scl	GPIO, CTBm, SCB4, CSD
	E2	4	P3.6	ctb0_oa0-	–	–	scb4_uart_tx	–	–	scb4_spi_miso	scb4_i2c_sda	GPIO, CTBm, SCB4, CSD
	C1		P3.7	ctb0_oa0+	–	–	-	–	–	–	–	GPIO, CTBm, CSD
	E15	34	P4.0	–	–	–	scb0_uart_rx	–	swd_clk(alt)	scb0_spi_clk	scb0_i2c_scl	GPIO, SCB0, CSD
	D12	35	P4.1	–	–	–	scb0_uart_tx	–	swd_data(alt)	scb0_spi_mosi	scb0_i2c_sda	GPIO, SCB0, CSD
	G2	7	P5.0	csd_csh_tank	–	–	scb2_uart_rx	–	–	scb2_spi_clk	scb2_i2c_scl	GPIO, SCB2, CSD
	E1	8	P5.1	csd_c_mod	–	–	scb2_uart_tx	–	–	scb2_spi_mosi	scb2_i2c_sda	GPIO, SCB2, CSD
	H6	9	P5.2	csd_c_shield	–	–	scb2_uart_cts	–	–	scb2_spi_miso	lpcomp1_comp	GPIO, CSD
	H1	10	P5.3	csd_vref_ext	–	–	scb2_uart_rts	–	–	scb2_spi_select	lpcomp0_comp	GPIO, SCB2, CSD
	G1		P5.4	–	–	–	–	–	–	–	–	GPIO, CSD
	H4	11	P5.5	–	–	–	–	–	–	–	–	GPIO, CSD, embedded controller interrupt
	G15		P7.0	–	–	–	scb1_uart_rx	–	–	–	–	GPIO, SCB1, thunderbolt interrupt PD port-1, CSD
	G14		P7.1	–	–	–	–	–	–	–	–	CSD, hot plug detect PD port-1
	A14		P7.2	–	–	–	–	–	–	–	–	GPIO, CSD
	B13		P7.3	–	–	–	scb7_uart_tx	–	–	scb7_spi_miso	scb7_i2c_sda	GPIO, SCB7, CSD
	B11		P7.4	–	–	–	scb7_uart_rx	–	–	scb7_spi_clk	scb7_i2c_scl	GPIO, SCB7, CSD
	A9		P7.5	–	–	–	scb7_uart_cts	–	–	scb7_spi_mosi	–	GPIO, SCB7, CSD
	B9		P7.6	–	–	–	scb7_uart_rts	–	–	scb7_spi_select	–	GPIO, SCB7, CSD

Notes
1. Not available in 48-QFN package.
2. I/O logic is connected to VDDD instead of VDDIO.

Table 2 Pin list for PMG1-S3 CYPM132x-97BZXI and CYPM1311-48LDXI *(continued)*

Group	97-BGA	48-QFN	Pin name	Alternate functions (HSIOM_PORT_SEL)								Pin description
				Analog	ACT#0	ACT#1	ACT#2	ACT#3	DS#0	DS#2	DS#3	
Muxes/ Switches	R8	17	P0.0/ LSRX_P1[2]	–	–	–	–	–	usbpd1_sbu_lsrx[1]	–	–	CSD, GPIO, LSRX port-1
	R7		P0.1/ LSTX_P1[2]	–	–	–	–	–	usbpd1_sbu_lstx	–	–	CSD, GPIO, LSTX port-1
	P7		P0.2/ DBG1_P1[2]	–	–	–	–	–	usbpd1_sbu_dbg1	–	–	CSD, GPIO, SBU-LSTX debug1 pin port-1
	K6		P0.3/ DBG2_P1[2]	–	–	–	–	–	usbpd1_sbu_dbg2	–	–	CSD, GPIO, SBU-LSTX debug2 pin port-1
	P8		P0.4/ DBG2_P0[2]	–	tcpwm1_line	tcpwm1_compare_match	–	tcpwm1_tr_in	usbpd0_sbu_dbg2	–	–	CSD, GPIO, TCPWM1, SBU-LSTX debug2 pin port-0
	M8		P0.5/ DBG1_P0[2]	–	–	–	–	–	usbpd0_sbu_dbg1	–	–	CSD, GPIO, SBU-LSTX debug1 pin port-0
	R9		P0.6/ LSTX_P0[2]	–	–	–	–	–	usbpd0_sbu_lstx	–	–	CSD, GPIO, LSTX port-0
	R11		P0.7/ LSRX_P0[2]	–	–	–	–	–	usbpd0_sbu_lsrx	–	–	CSD, GPIO, LSRX port-0
	R5	15	P6.0/ SBU1_P1[2]	–	ext_clk1	–	scb6_uart_tx	–	usbpd1_sbu_io1	scb6_spi_miso	scb6_i2c_sda	CSD, GPIO, Type-C auxiliary signal for DisplayPort – Connector side: Port-1, SCB6, external clock input
	P5	16	P6.1/ SBU2_P1[2]	–	–	–	scb6_uart_rx	–	usbpd1_sbu_io2	scb6_spi_clk	scb6_i2c_scl	CSD, GPIO, Type-C auxiliary signal for DisplayPort – Connector side: Port-1, SCB6
	P13	18	P6.2/ SBU2_P0[2]	–	tcpwm0_line	tcpwm0_compare_match	scb6_uart_rts	tcpwm0_tr_in	usbpd0_sbu_io2	scb6_spi_select	–	CSD, GPIO, Type-C auxiliary signal for DisplayPort – Connector side: Port-0, SCB6
	R13	19	P6.3/ SBU1_P0[2]	–	–	–	scb6_uart_cts	–	usbpd0_sbu_io1	scb6_spi_mosi	–	CSD, GPIO, Type-C auxiliary signal for DisplayPort – Connector side: Port-0, SCB6
	M4		AUX_P_P1	–	–	–	–	–	–	–	–	Type-C auxiliary signal for DisplayPort – System side: Port-1
Muxes/ Switches	M6		AUX_N_P1	–	–	–	–	–	–	–	–	Type-C auxiliary signal for DisplayPort – System side: Port-1
	P11		AUX_P_P0	–	–	–	–	–	–	–	–	Type-C auxiliary signal for DisplayPort – System side: Port-0
	P9		AUX_N_P0	–	–	–	–	–	–	–	–	Type-C auxiliary signal for DisplayPort – System side: Port-0

Notes
1. Not available in 48-QFN package.
2. I/O logic is connected to VDDD instead of VDDIO.

Table 2 Pin list for PMG1-S3 CYPM132x-97BZXI and CYPM1311-48LDXI *(continued)*

Group	97-BGA	48-QFN	Pin name	Alternate functions (HSIOM_PORT_SEL)								Pin description
				Analog	ACT#0	ACT#1	ACT#2	ACT#3	DS#0	DS#2	DS#3	
USB FS	A11	40	USBDM	–	–	–	–	–	–	–	–	USB 2.0 (FS-PHY) DM
	A13	39	USBDP	–	–	–	–	–	–	–	–	USB 2.0 (FS-PHY) DP
VBUS OCP/ SCP/RCP	A15	37	CSN_P0	–	–	–	–	–	–	–	–	Current sense negative input for VBUS side external Rsense: Port-0
	B15	38	CSP_P0	–	–	–	–	–	–	–	–	Current sense positive input for VBUS side external Rsense: Port-0
	C14		CSN_P1	–	–	–	–	–	–	–	–	Current sense negative input for VBUS side external Rsense: Port-1
	C15		CSP_P1	–	–	–	–	–	–	–	–	Current sense positive input for VBUS side external Rsense Port-1
USB PD Type-C	N14	28	CC1_P0	–	–	–	–	–	–	–	–	USB PD port-0 connector detect/configuration channel 1
	N15											
	N1		CC1_P1	–	–	–	–	–	–	–	–	USB PD port-1 connector detect/configuration channel 1
	N2											
	J14	30	CC2_P0	–	–	–	–	–	–	–	–	USB PD port-0 connector detect/configuration channel 2
	J15											
	J1		CC2_P1	–	–	–	–	–	–	–	–	USB PD port-1 connector detect/configuration channel 2
	J2											

Notes
1. Not available in 48-QFN package.
2. I/O logic is connected to VDDD instead of VDDIO.

Table 2 Pin list for PMG1-S3 CYPM132x-97BZXI and CYPM1311-48LDXI *(continued)*

Group	97-BGA	48-QFN	Pin name	Alternate functions (HSIOM_PORT_SEL)								Pin description
				Analog	ACT#0	ACT#1	ACT#2	ACT#3	DS#0	DS#2	DS#3	
VBUS_NGDO	R14	24	VBUS_IN_NGDO_P0	–	–	–	–	–	–	–	–	VBUS input for the NGDO - Path-0 (4 V to 30 V)
	R2		VBUS_IN_NGDO_P1	–	–	–	–	–	–	–	–	VBUS input for the NGDO - Path-1 (4 V to 30 V)
	R15	25	VBUS_OUT_NGDO_P0	–	–	–	–	–	–	–	–	VBUS output for the NGDO - Path-0 (4 V to 30 V)
	R1		VBUS_OUT_NGDO_P1	–	–	–	–	–	–	–	–	VBUS output for the NGDO - Path-1 (4 V to 30 V)
	P14	27	VBUS_IN_CTRL_P0	–	–	–	–	–	–	–	–	Full rail control I/O for enabling/disabling NFET (Input-Side) of USB Type-C Port-0
	P2		VBUS_IN_CTRL_P1	–	–	–	–	–	–	–	–	Full rail control I/O for enabling/disabling NFET (Input-Side) of USB Type-C Port-1
	P15	26	VBUS_OUT_CTRL_P0	–	–	–	–	–	–	–	–	Full rail control I/O for enabling/disabling NFET (Output Side) of USB Type-C Port-0
VBUS_NGDO	P1		VBUS_OUT_CTRL_P1	–	–	–	–	–	–	–	–	Full rail control I/O for enabling/disabling NFET (Output Side) of USB Type-C Port-1
Reset	E14	33	XRES	–	–	–	–	–	–	–	–	RESET INPUT

Notes
1. Not available in 48-QFN package.
2. I/O logic is connected to VDDD instead of VDDIO.

Table 2 Pin list for PMG1-S3 CYPM132x-97BZXI and CYPM1311-48LDXI *(continued)*

Group	97-BGA	48-QFN	Pin name	Alternate functions (HSIOM_PORT_SEL)								Pin description
				Analog	ACT#0	ACT#1	ACT#2	ACT#3	DS#0	DS#2	DS#3	
Power	B14	36	VSYS	–	–	–	–	–	–	–	–	2.8-V to 5.5-V supply for the system
	D8	43	VDDD	–	–	–	–	–	–	–	–	VDDD supply output 1. VSYS powered - (Min: VSYS-100 mV) 2.7 Vto 5.5 V 2. VBUS powered - 2.7 V to 3.6V
	D6	5	VDDA	–	–	–	–	–	–	–	–	Programmable analog supply (2.7V - 5.5V) shorted to VDDD at board level
	F6			–	–	–	–	–	–	–	–	
	B8	23	VDDIO	–	–	–	–	–	–	–	–	GPIO supply (1.71 V - 5.5 V)
	H12	42		–	–	–	–	–	–	–	–	
	D10	41	VCCD	–	–	–	–	–	–	–	–	1.8-V regulator output for filter capacitor. This pin cannot drive external load.
	H15	31	VBUS_C_P0	–	–	–	–	–	–	–	–	VBUS input for the NGDO - Port-0 (4 V to 30V)
	H14		VBUS_C_P1	–	–	–	–	–	–	–	–	VBUS input for the NGDO - Port-1 (4 V to 30 V)
	L14	29	VCONN_-Source_P0	–	–	–	–	–	–	–	–	4.85 V to 5.5 V supply for VCONN FET of Type-C: Port-0
	L15			–	–	–	–	–	–	–	–	
	L1		VCONN_-Source_P1	–	–	–	–	–	–	–	–	4.85 V to 5.5 V supply for VCONN FET of Type-C: Port-1
	L2			–	–	–	–	–	–	–	–	
Ground	F10	6	VSS	–	–	–	–	–	–	–	–	Ground
	F12	32	VSS	–	–	–	–	–	–	–	–	
	F8	44	VSS	–	–	–	–	–	–	–	–	
	H10		VSS	–	–	–	–	–	–	–	–	
	H8		VSS	–	–	–	–	–	–	–	–	
	K10		VSS	–	–	–	–	–	–	–	–	
	K8		VSS	–	–	–	–	–	–	–	–	

Notes
1. Not available in 48-QFN package.
2. I/O logic is connected to VDDD instead of VDDIO.

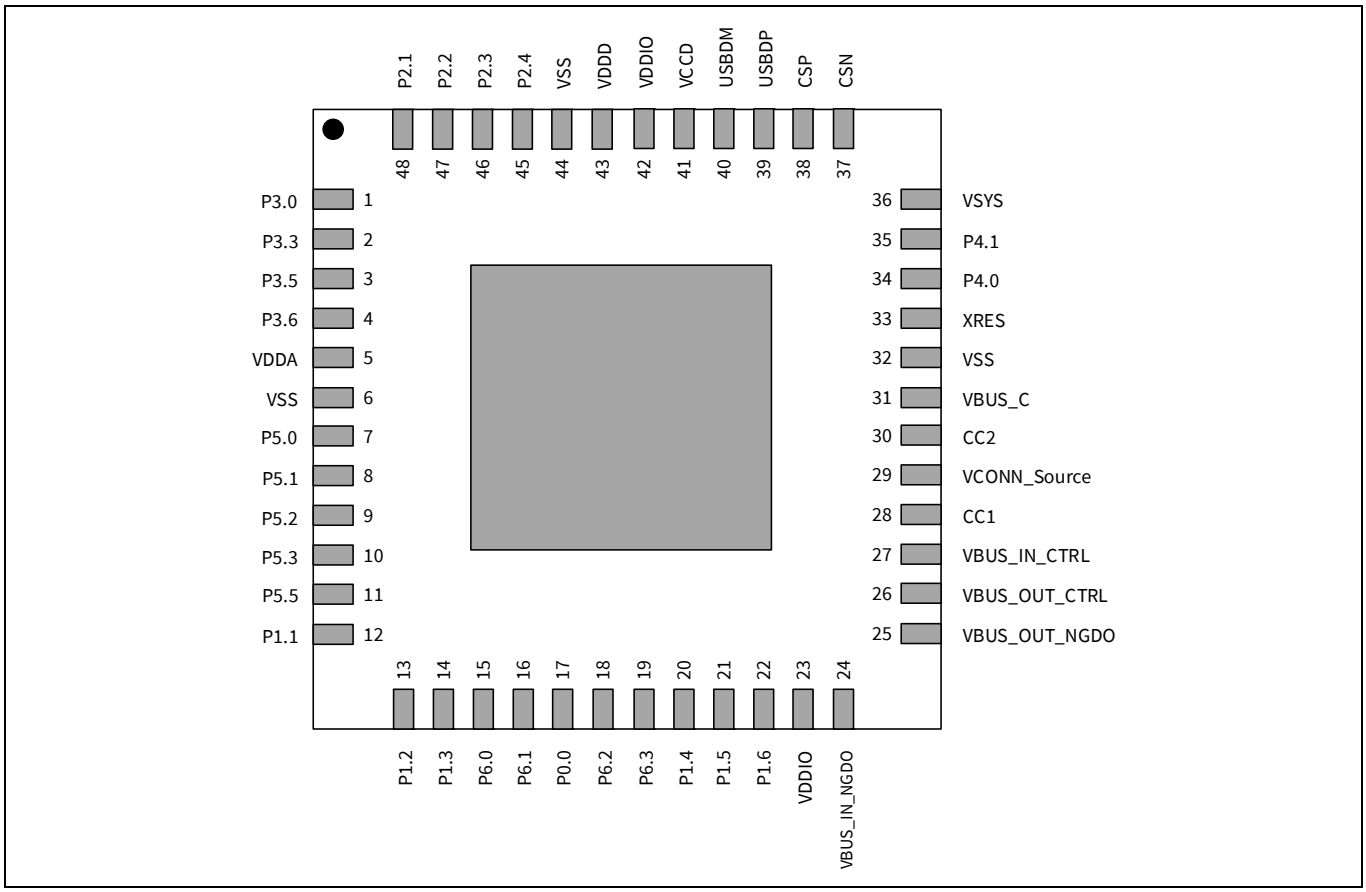


Figure 6 CYPM1311-48LDXI: single-port 48-pin QFN

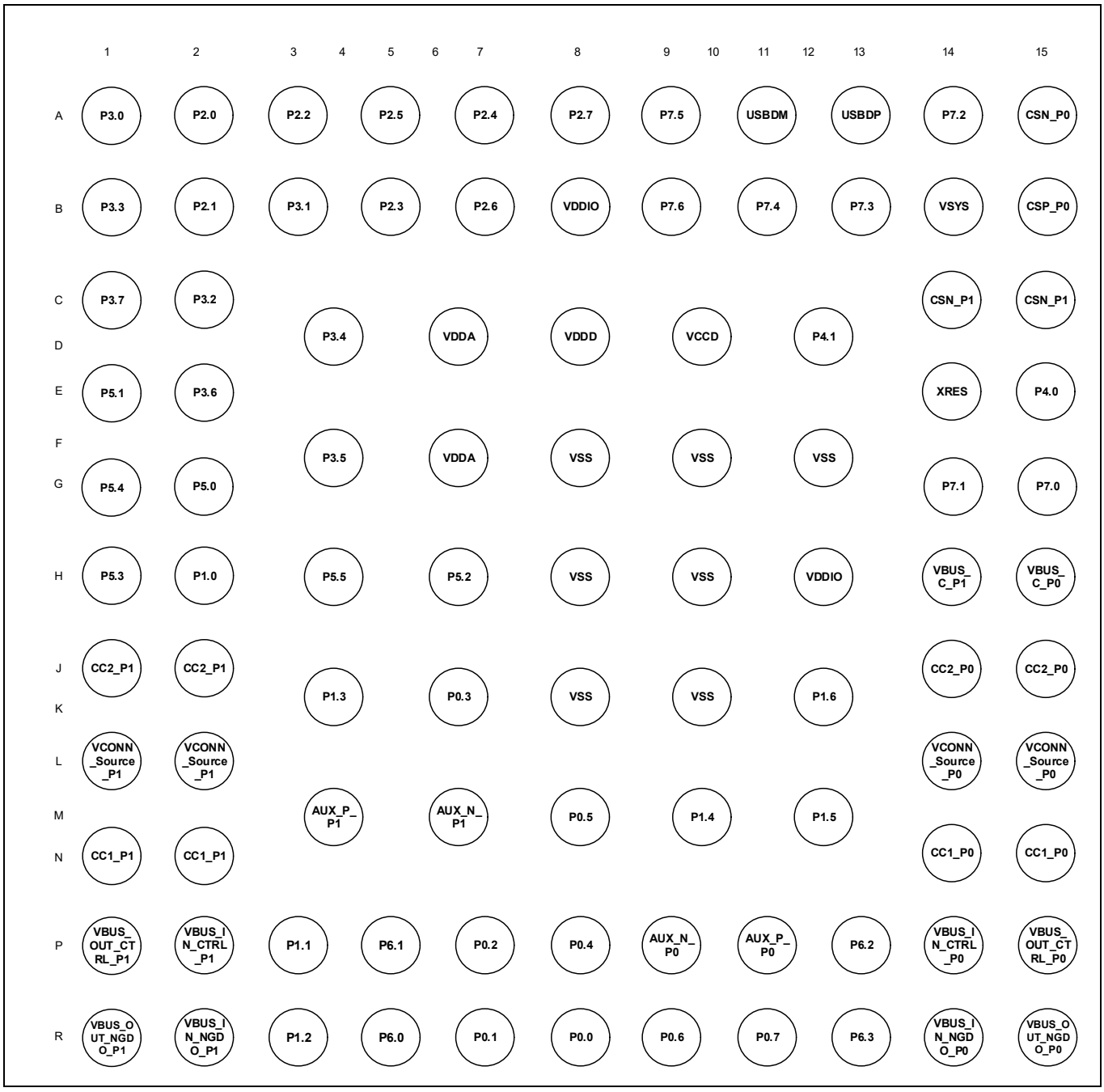


Figure 7 CYPM132x-97BZXI: dual-port 97-ball BGA

5 Application diagrams

Figure 8 illustrates PMG1-S3 in a single port power consumer role which will negotiate PD contract with the connected charger to get higher voltage and act as an MCU in the system. As only one Type-C port is needed, PMG1-S3 48-pin QFN can be used for this device application.

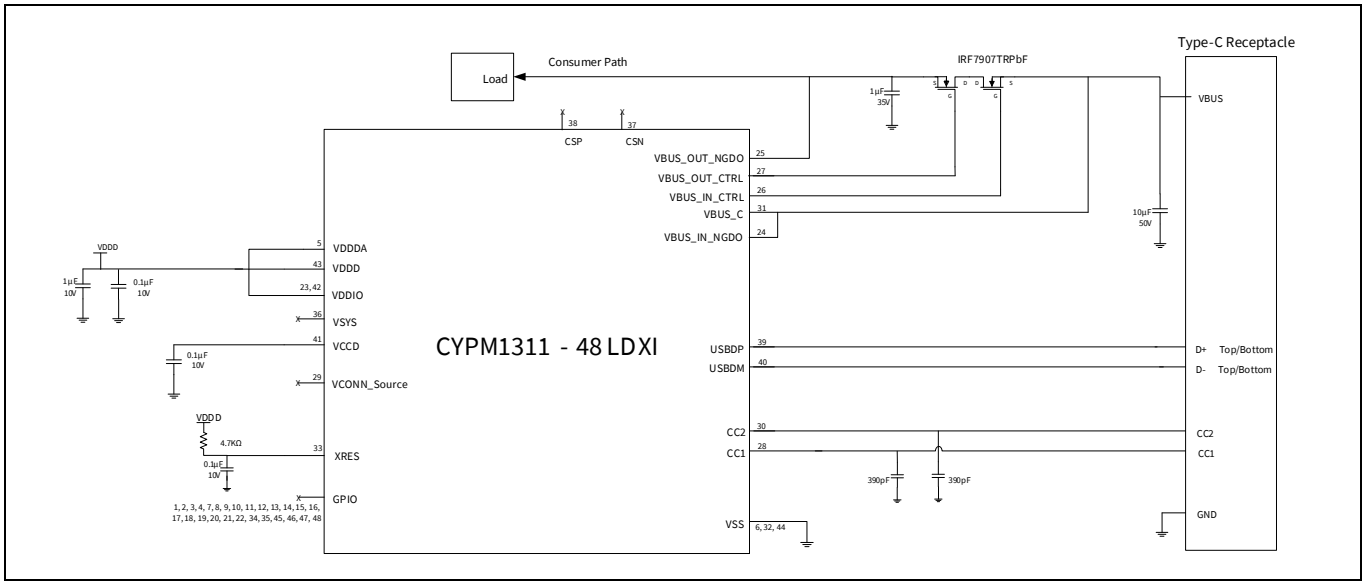


Figure 8 Power sink application using 48-pin QFN PMG1-S3

Figure 9 illustrates an application using 97-ball BGA PMG1-S3 where it acts as a power consumer on both Type-C ports.

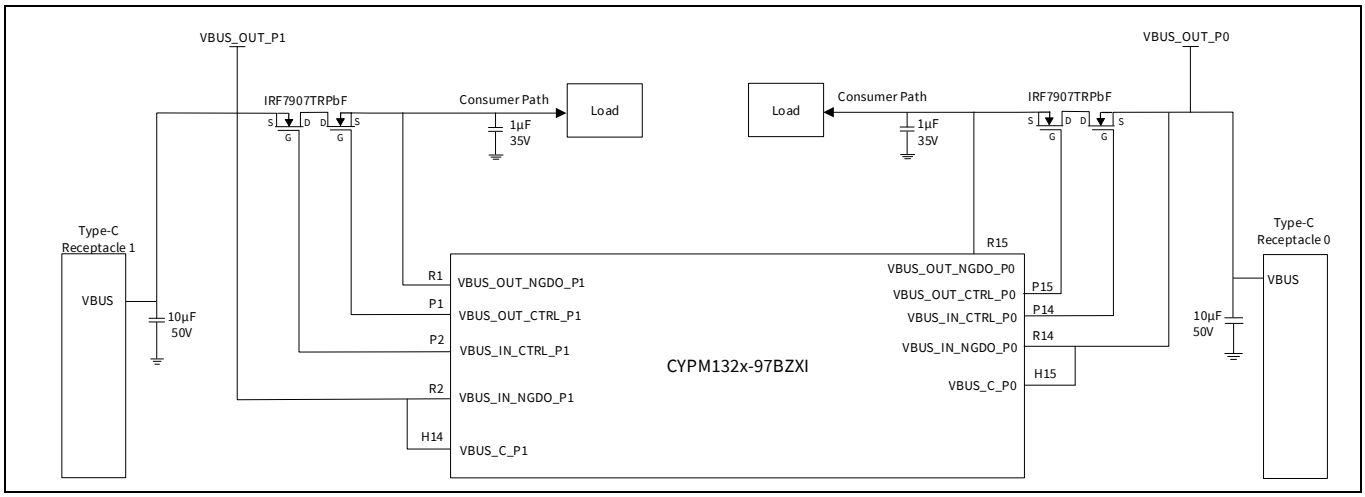


Figure 9 Sink configuration on both Type-C ports using 97-ball BGA

Figure 10 illustrates an application using 97-ball BGA PMG1-S3 where it acts as a power provider on both Type-C ports.

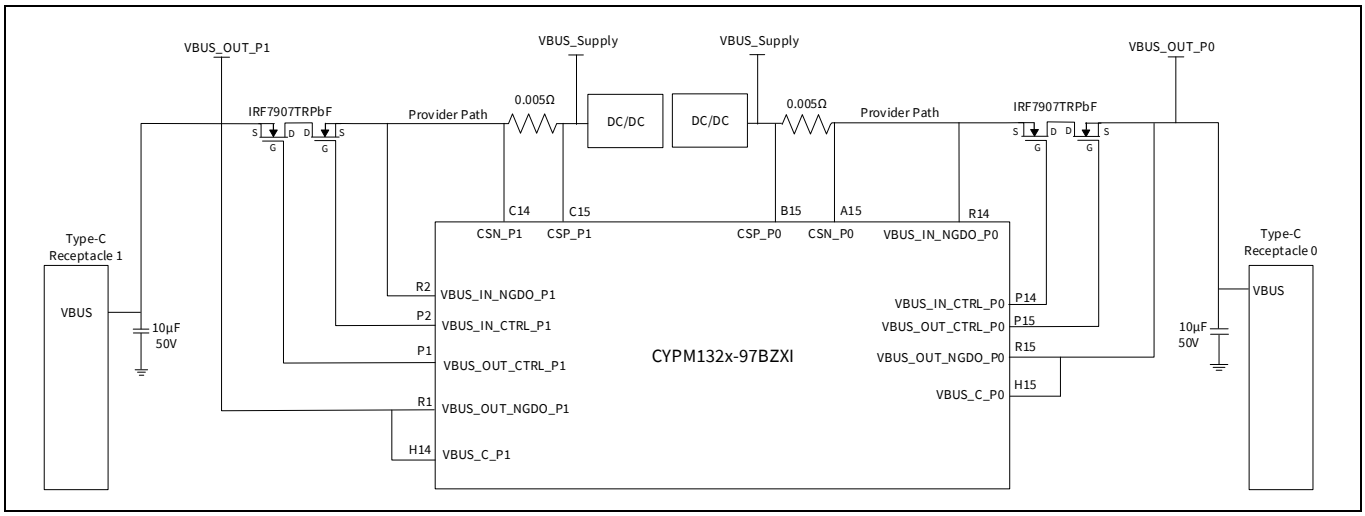


Figure 10 Source configuration on both Type-C ports using 97-ball BGA

Figure 11 illustrates an application using 97-ball BGA PMG1-S3 where it acts as a power provider on one of the Type-C ports and as power consumer on the other Type-C port.

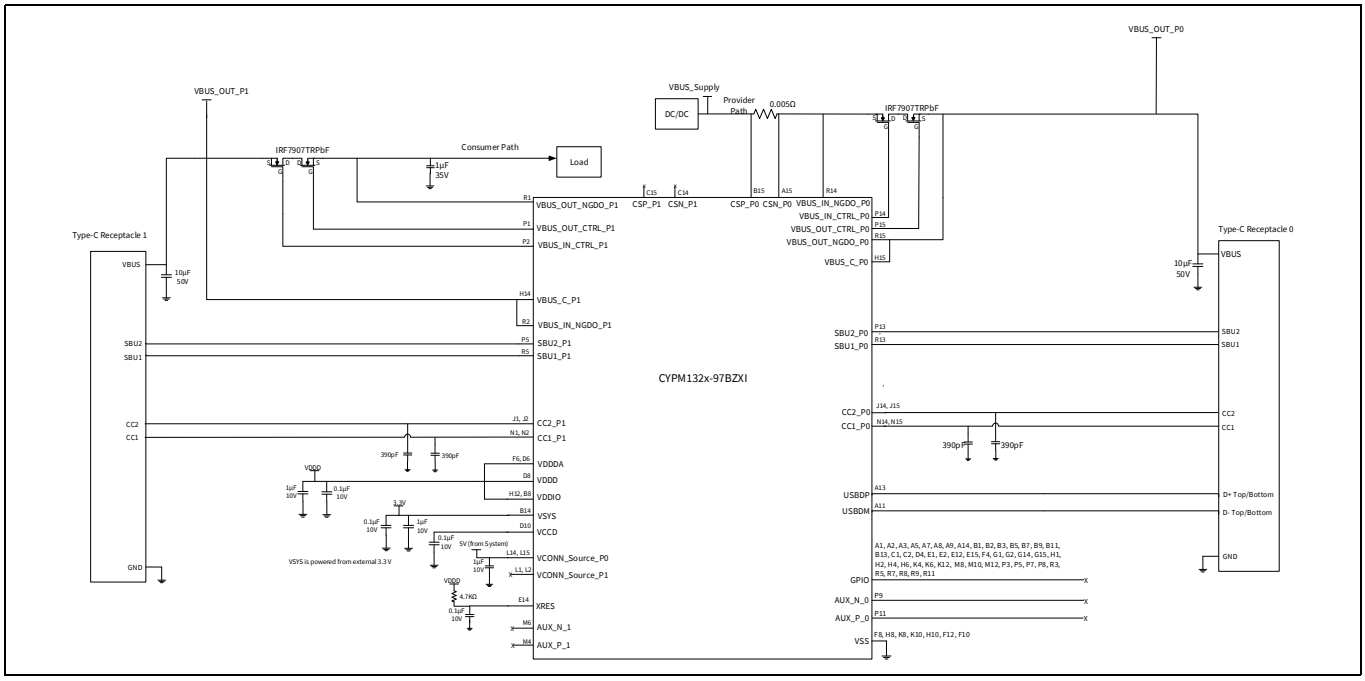


Figure 11 Power provider and consumer application using 97-ball BGA PMG1-S3

In **Figure 12**, Port 0 is configured as a DRP on one of the Type-C ports and consumer on the other Type-C port. For DRP port, both pairs of PMG1-S3 gate driver pins are used and on the consumer path on Port 1, external FETs controlled by a GPIO are used.

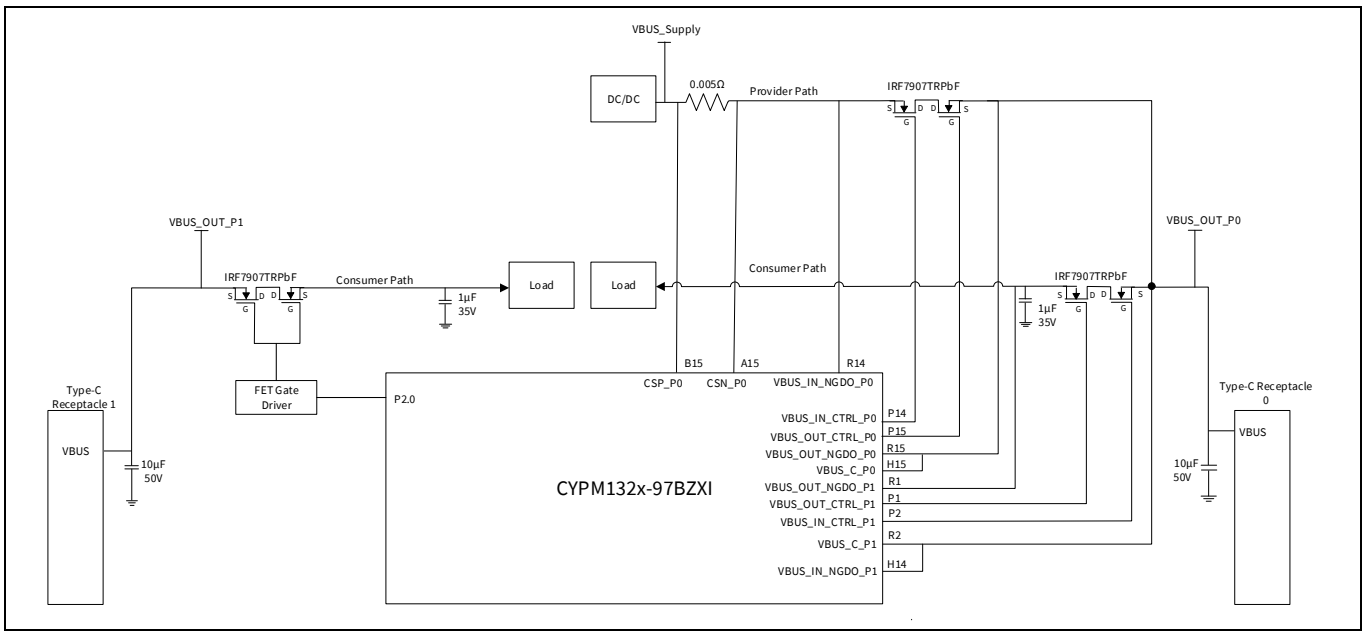


Figure 12 DRP on one Type-C port and sink on the second Type-C port using 97-ball BGA

6 Electrical specifications

6.1 Absolute maximum ratings

Table 3 Absolute maximum ratings[3]

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PWR.ABS#1	V_{DDIO_ABS}	I/O Supply relative to V_{SS} (V_{SSIO} = V_{SSD} = V_{SSA})	–0.5[4]	–	6	V[5]	Absolute minimum-maximum
SID.PWR.ABS#2	V_{CCD_ABS}	Direct digital core voltage input relative to V_{SSD}	–0.5	–	1.95	V	
SID.PWR.ABS#3	V_{GPIO_ABS}	GPIO voltage	–0.5	–	6		Absolute minimum-maximum. It cannot be more than "V_{DDIO} +0.5" at any point.
SID.PWR.ABS#4	$V_{GPIO\_FAILSAFE\_ABS}$	Fail-Safe GPIO voltage	–0.5	–	6		Absolute minimum-maximum
SID.PWR.ABS#5	I_{GPIO_ABS}	Current per GPIO	–25	–	25	mA	
SID.PWR.ABS#6	$I_{GPIO\_injection}$	GPIO injection current per pin	–0.5	–	0.5		
SID.PD.PWR.ABS#1	$V_{CONN\_SOURCE\_ABS}$	Min-max supply voltage relative to V_{SS}	–0.5	–	6	V	
SID.PD.PWR.ABS#2	V_{SYS_ABS}						
SID.PD.PWR.ABS#3	V_{BUS_ABS}	Min-max VBUS_C_P0/1 voltage relative to V_{SS}	–0.3	–	34		Minimum-absolute maximum
SID.PD.PWR.ABS#4	$V_{BUS\_NGDO\_ABS}$	Min-Max VBUS_IN/OUT_P0/1 voltage relative to V_{SS}	–0.3	–	34		Absolute minimum-maximum
SID.PD.PIN.ABS#1	$V_{CC\_PIN\_ABS}$	Min-max voltage on CC1 and CC2 pins	–0.5	–	6		Absolute minimum-maximum. It cannot be more than "V_{DDD} +0.5" at any point.
SID.PD.PIN.ABS#2	$V_{SBU\_PIN\_ABS}$	Min-max voltage on SBU1 and SBU2 pins	–0.5	–	6		
SID.PD.PIN.ABS#3	$V_{USB\_PIN\_ABS}$	Min-max voltage on USBDP and USBDM pins	–0.5	–	6		
SID.PD.PIN.ABS#4	$V_{AUX\_PIN\_ABS}$	Min-max voltage on AUX_N_P0/1 and AUX_P_P0/1 pins	–0.5	–	6		
SID.PD.PIN.ABS#5	$V_{CSA\_PIN\_ABS}$	Min-max voltage on CSP_P0/1 and CSN_P0/1 pins	–0.3	–	34		Absolute minimum-maximum
BID1	TSTG_AMAX	Storage temperature	–55	25	150	°C	Non-operating temperature. Per JESD22-A103 HTSL test.
BID44	ESD_HBM	Electro static discharge voltage	2000	–	–	V	Human body model ESD
BID45	ESD_CDM		500				Charged device model ESD
BID46	I_LU	Latch-up current limits	–100	–	100	mA	Max/min current into any input or output, pin-to-pin, pin-to-supply.

Notes
3. Usage above the absolute maximum conditions listed in **Table 3** may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC Standard JESD22-A103, high temperature storage life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.
4. In a system, if the negative spike exceeds the minimum voltage specified here, it is recommended to add Schottky diode to clamp the negative spike.
5. All voltages are relative to ground unless otherwise specified.

Table 4 Pin based absolute maximum ratings

Sr. No.	Pin (97-ball BGA)	Pin (48-pin QFN)	Name	Absolute minimum (volts)[66]	Absolute maximum (volts)[66]	Remarks
1	H2		P1.0	-0.5	6	Maximum voltage not to exceed VDDIO + 0.5
2	P3	12	P1.1			
3	R3	13	P1.2			
4	K4	14	P1.3			
5	M10	20	P1.4			
6	M12	21	P1.5			
7	K12	22	P1.6			
8	A2		P2.0			
9	B2	48	P2.1			
10	A3	47	P2.2			
11	B5	46	P2.3			
12	A7	45	P2.4			
13	A5		P2.5			
14	B7		P2.6			
15	A8		P2.7			
16	A1	1	P3.0			
17	B3		P3.1			
18	C2		P3.2			
19	B1	2	P3.3			
20	D4		P3.4			
21	F4	3	P3.5			
22	E2	4	P3.6			
23	C1		P3.7			
24	E15	34	P4.0			
25	D12	35	P4.1			
26	G2	7	P5.0			
27	E1	8	P5.1			
28	H6	9	P5.2			
29	H1	10	P5.3			
30	G1		P5.4			
31	H4	11	P5.5			
32	G15		P7.0			
33	G14		P7.1			
34	A14		P7.2			
35	B13		P7.3			
36	B11		P7.4			
37	A9		P7.5			
38	B9		P7.6			

Note
6. All voltages are measured with respect to Vss.

Table 4 Pin based absolute maximum ratings *(continued)*

Sr. No.	Pin (97-ball BGA)	Pin (48-pin QFN)	Name	Absolute minimum (volts)[66]	Absolute maximum (volts)[66]	Remarks
39	R8	17	P0.0/LSRX_P1	–0.5	6	Maximum voltage not to exceed VDDD + 0.5
40	R7		P0.1/LSTX_P1			
41	P7		P0.2/DBG1_P1			
42	K6		P0.3/DBG2_P1			
43	P8		P0.4/DBG2_P0			
44	M8		P0.5/DBG1_P0			
45	R9		P0.6/LSTX_P0			
46	R11		P0.7/LSRX_P0			
47	R5	15	P6.0/SBU1_P1			
48	P5	16	P6.1/SBU2_P1			
49	P13	18	P6.2/SBU2_P0			
50	R13	19	P6.3/SBU1_P0			
51	M4		AUX_P_P1	–0.5	6	Maximum voltage not to exceed VDDD + 0.5
52	M6		AUX_N_P1			
53	P11		AUX_P_P0			
54	P9		AUX_N_P0			
55	A11	40	USBDM	–0.5	6	Maximum voltage not to exceed VDDD + 0.5
56	A13	39	USBDP			
57	A15	37	CSN_P0	–0.3	34	–
58	B15	38	CSP_P0			
59	C14		CSN_P1			
60	C15		CSP_P1			
61	N14	28	CC1_P0	–0.5	6	–
62	N15					
63	N1		CC1_P1			–
64	N2					
65	J14	30	CC2_P0			–
66	J15					
67	J1		CC2_P1			–
68	J2					
69	R14	24	VBUS_IN_NGDO_P0	–0.3	34	–
70	R2		VBUS_IN_NGDO_P1			
71	R15	25	VBUS_OUT_NGDO_P0			
72	R1		VBUS_OUT_NGDO_P1			
73	P14	27	VBUS_IN_CTRL_P0			
74	P2		VBUS_IN_CTRL_P1			
75	P15	26	VBUS_OUT_CTRL_P0	–0.3	42	This is an output only pin
76	P1		VBUS_OUT_CTRL_P1			
77	E14	33	XRES	–0.5	6	Maximum voltage not to exceed VDDIO + 0.5
78	B14	36	VSYS	–0.5	6	–

Note
6. All voltages are measured with respect to Vss.

Table 4 Pin based absolute maximum ratings *(continued)*

Sr. No.	Pin (97-ball BGA)	Pin (48-pin QFN)	Name	Absolute minimum (volts)[66]	Absolute maximum (volts)[66]	Remarks
79	D8	43	VDDD	–	6	Short VDDD to VDDA on board level
80	D6	5	VDDA	–		
81	F6					
82	B8	23	VDDIO	–0.5	6	VDDIO can be at separate level from VSYS, provided VDDIO < VSYS
83	H12	42				
84	D10	41	VCCD	–0.5	1.95	This is output only pin
85	H15	31	VBUS_C_P0	–0.3	34	–
86	H14		VBUS_C_P1			
87	L14	29	VCONN_Source_P0	–0.5	6	–
88	L15					
89	L1		VCONN_Source_P1	–0.5	6	–
90	L2					
91	F10	6	VSS	–	–	–
92	F12	32				
93	F8	44				
94	H10					
95	H8					
96	K10					
97	K8					

Note
6. All voltages are measured with respect to Vss.

6.2 Device level specifications

Table 5 DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PWR#1	V_{DDD}	Regulated output voltage when VSYS powered power supply voltage (not to be driven externally)	$V_{SYS - 0.1}$	–	V_{SYS}	V	–40°C to +85°C T_A; Load current from V_{DDD} = 30 mA
SID.PWR#1A	V_{DDD}	Regulated output voltage when VBUS powered power supply voltage (not to be driven externally)	3	–	3.65		–40°C to +85°C T_A
SID.PWR#1B	V_{DDD}	Power supply voltage for USB bus power	4.25	–	5.35		USB-PHY internal regulator enabled
SID.PWR#1C	V_{DDD}	Power supply voltage for USB PHY in bypass mode, Parameters guaranteed	3.05	–	3.55		USB-PHY internal regulator in Bypass mode
SID.PWR#1D	V_{DDD}	Power supply voltage for USB PHY in bypass mode, Function-ality only guaranteed	2.95	–	3.63		
SID.PWR#2	$V_{DDWRITE}$	Supply voltage for flash write	2.7	–	5.5		–40°C to +85°C T_A, All V_{DDD}
SID.PWR#4	V_{DDIO}	Supply voltage for I/O	1.71	–	V_{DDD}		
SID.PWR#5	V_{DDA}	Supply voltage for I/O CAPSENSE™, Op_amp, Comparator and 12-bit ADC blocks	V_{DDD}	–	V_{DDD}		–40°C to +85°C T_A, All V_{DDD}; V_{DDA} = V_{DDD}
SID.PWR#6	V_{CCD}	Output voltage for core Logic	–	1.8	–		–
SID.PWR#7	Cefc	External regulator voltage bypass for V_{CCD}	80	100	120	nF	X5R ceramic or better
SID.PWR#8	Cexc	External Regulator voltage bypass for V_{DDD}	–	4.7	–	µF	
SID.PWR#9	Cexv	Power supply decoupling capacitor for V5V_0 and V5V_1, V_{SYS}, V_{DDIO}, V_{DDA}	–	1	–		
SID.PD.PWR#1	V5V	Power supply for V_{CONN}	4.85	–	5.5	V	–40°C to +85°C T_A
SID.PD.PWR#2	VSYS_UFP	VSYS valid range	2.8	–	5.5		UFP applications
SID.PD.PWR#2A	VSYS_DFP_DRP		3				DFP/DRP applications
SID.PD.PWR#3	VBUS	VBUS_C_P0/1 valid range	4	–	30		–
SID.PD.PWR#3A	VBUS_NGDO	VBUS_IN/OUT_NGDO_P0/1 valid range	4	–	30		–
Active mode, VDDD = 1.71 V to 5.5 V							
SID16	IDD11	Execute from flash; CPU at 24 MHz	–	5.8	–	mA	Typ = 25°C @ V_{DDD} = 3.3 V
SID19	IDD14	Execute from flash; CPU at 48 MHz	–	11.2	–		
Sleep mode, VDDD = 2.0 V to 5.5 V (Regulator ON)							
SID22	IDD17	I^2C wakeup, WDT, and comparators on 6 MHz	–	1.3	2.2	mA	Typ = 25°C @ V_{DDD} = 3.3 V Max = 85°C @ 5.5 V
SID25	IDD20	I^2C wakeup, WDT, and comparators on. 12 MHz	–	1.85	2.5		

Table 5 DC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
Deep Sleep mode, VDDD = 2.7 V to 5.5 V							
SID34	IDD29	I^2C wakeup and WDT ON	–	250	–	µA	Typ = 25°C @ V_{DDD} = 3.3 V Power source = VSYS, Type-C not attached, CC enabled for wakeup, Rp and Rd connected at 70 ms intervals by CPU. Rp, Rd connection should be enabled for both PD ports. If VBUS_IN_NGDO and VBUS_OUT_NGDO also present, refer to SID.PD.GD#11 and SID.PD.GD#12
SID_DS1	IDD_DS1	VSYS = 3.3 V Port-0 and 1: CC wakeup ON, Type-C not connected	–	200	–		Power source = VSYS, Type-C not attached, CC enabled for wakeup, Rp and Rd connected at 70 ms intervals by CPU. Rp, Rd connection should be enabled for both PD ports. If VBUS_IN_NGDO and VBUS_OUT_NGDO are also present, refer to SID.PD.GD#11 and SID.PD.GD#12
SID_DS3	IDD_DS2	VSYS = 3.3 V Port-1: CC wakeup ON, Port-0: CC/VCONN/SBU/NGDO/ CSA/UVOV enabled and SBU comparators disabled	–	600	–		Power source = VSYS, One Port attached, chip in Deep Sleep Port-1: CC wakeup ON, Port-0: CC/ VCONN/ SBU/NGDO/CSA/ UVOV enabled and SBU comparators disabled
SID_DS3_A	IDD_DS2A	VSYS = 3.3 V Port-0 and 1: CC/ VCONN/SBU/NGDO/CSA/UVOV enabled and SBU comparators disabled	–	1100	–		Both ports attached (CC/ VCONN/ SBU/NGDO/CSA/ UVOV enabled and SBU comparators disabled), chip in Deep Sleep
XRES current							
SID307	IDD_XR	Supply current while XRES asserted	–	130	–	µA	Power source = VSYS = 3.3 V, Type-C not attached, TA = 25°C If VBUS_IN_NGDO and VBUS_OUT_NGDO also present, refer to SID.PD.GD#11a and SID.PD.GD#12a

Table 6 AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.CPU#1	F_{CPU}	CPU frequency	DC	–	48	MHz	–40°C to +85°C TA, All V_{DDD}
SID.CPU#2	T_{SLEEP}	Wakeup from Sleep mode	–	0	–	µs	–
SID.CPU#3	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	35	–		–

6.3 GPIO

Table 7 GPIO DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GPIO.DC#1	Vih_CMOS	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS input
SID.GPIO.DC#2	Vil_CMOS	Input voltage low threshold	–	–	0.3 × V_{DDD}		
SID.GPIO.DC#1a	Vih_VDDIO2.7–	LVTTL input, V_{DDD} < 2.7 V	0.7 × V_{DDD}	–	-		–
SID.GPIO.DC#2a	Vil_VDDIO2.7–	LVTTL input, V_{DDD} < 2.7 V	–	–	0.3 × V_{DDD}		–
SID.GPIO.DC#1b	Vih_VDDIO2.7+	LVTTL input, V_{DDD} ≥ 2.7 V	2	–	–		–
SID.GPIO.DC#2b	Vil_VDDIO2.7+	LVTTL input, V_{DDD} ≥ 2.7 V	–	–	0.8		–
SID.GPIO.DC#1c	Vih_VCCHIB	V_{IH}, 1.8-V input mode	1.26	–	–		–
SID.GPIO.DC#2c	Vil_VCCHIB	V_{IL}, 1.8-V input mode	–	–	0.54		–
SID.GPIO.DC#4	V_{OH}	Output voltage high level	V_{DDD} – 0.6	–	–		Ioh = 4 mA at 3-V V_{DDD}
SID.GPIO.DC#4a	V_{OH}	Output voltage high level	V_{DDD} – 0.5	–	–		Ioh = 1 mA at 1.8-V V_{DDD}
SID.GPIO.DC#5	V_{OL}	Output voltage low level	–	–	0.6		Iol = 4 mA at 1.8-V V_{DDD}
SID.GPIO.DC#5a	V_{OL}	Output voltage low level	–	–	0.6		Iol = 10 mA at 3-V V_{DDD}
SID.GPIO.DC#5b	V_{OL}	Output voltage low level	–	–	0.4		Iol = 3 mA at 3-V V_{DDD}
SID.GPIO.DC#6	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID.GPIO.DC#7	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5		–
SID.GPIO.DC#8	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25°C, V_{DDD} = 3.0-V
SID.GPIO.DC#8a	I_{IL_CTBM}	Input leakage on CTBm input pins	–	–	4		–
SID.GPIO.DC#9	C_{IN}	Input capacitance	–	–	7	pF	–
SID.GPIO.DC#3b	V_{HYSTTL}	Input hysteresis LVTTL V_{DDD} > 2.7 V	15	40	–	mV	–
SID.GPIO.DC#3	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DDD}	–	–		V_{DDIO} < 4.5V
SID.GPIO.DC#3a	$V_{HYSCMOS55}$	Input hysteresis CMOS	200.0	–	–		
SID.GPIO.DC#3c	V_{HYS_VCCHIB}	Input hysteresis, 1.8 V input mode	90	–	–		
SID.GPIO.DC#10	I_{DIODE}	Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	–
SID.GPIO.DC#11	I_{TOT_GPIO}	Maximum total source or sink chip current when V_{DDIO} supplied externally	–	–	200	mA	–
SID.GPIO.DC#11a	$I_{TOT\_GPIO\_VDDD}$	Maximum total source or sink chip current when V_{DDD} shorted to V_{DDIO} on board	–	–	10		–

Table 8 GPIO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GPIO.AC#1	T_{RISEF}	Rise time in Fast Strong mode	2	–	12	ns	3.3-V V_{DDD}, Cload = 25 pF
SID.GPIO.AC#2	T_{FALLF}	Fall time in Fast Strong mode	2	–	12		
SID.GPIO.AC#3	T_{RISES}	Rise time in Slow Strong mode	10	–	60		
SID.GPIO.AC#4	T_{FALLS}	Fall time in Slow Strong mode	10	–	60		
SID.GPIO.AC#5	$F_{GPIOUT1}$	GPIO Fout; 3.3 V ≤ V_{DDD} ≤ 5.5 V. Fast Strong mode	–	–	33	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID.GPIO.AC#6	$F_{GPIOUT2}$	GPIO Fout; 1.71 V ≤ V_{DDD} ≤ 3.3 V. Fast Strong mode	–	–	16.7		
SID.GPIO.AC#7	$F_{GPIOUT3}$	GPIO Fout; 3.3 V ≤ V_{DDD} ≤ 5.5 V. Slow Strong mode	–	–	7		
SID.GPIO.AC#8	$F_{GPIOUT4}$	GPIO Fout; 1.71 V ≤ V_{DDD} ≤ 3.3 V. Slow Strong mode	–	–	3.5		
SID.GPIO.AC#9	F_{GPIOIN}	GPIO input operating frequency; 1.71 V ≤ V_{DDD} ≤ 5.5 V	–	–	16		90/10% V_{IO}

6.3.1 XRES

Table 9 XRES DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.XRES.DC#1	VIH_XRES	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS input
SID.XRES.DC#2	VIL_XRES	Input voltage low threshold	–	–	0.3 × V_{DDD}		
SID.XRES.DC#3	CIN_XRES	Input capacitance	–	–	7	pF	–
SID.XRES.DC#4	VHYSXRES	Input voltage hysteresis	–	0.05 × V_{DDIO}	–	mV	–
SID.XRES.DC#5	IDIODE	Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	–

Table 10 XRES AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.XRES.AC#1	$T_{RESETWIDTH}$	Reset pulse width	5	–	–	µs	–40°C to +85°C TA, All V_{DDIO}
SID.XRES.AC#2	T_{XRES_GF}	External reset glitch filter period	–	20	–	ns	
BID194	$T_{RESETWAKE}$	Wake-up time from reset release	–	–	2.7	ms	–

6.4 Analog peripherals

Table 11 Opamp specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
IDD: Opamp block current. External load							
SID269	IDD_HI	power = hi	–	1100	1900	µA	–
SID270	IDD_MED	power = Med	–	550	1020		–
SID271	IDD_LOW	power = Lo	–	150	370		–
GBW: Load = 20pF, 0.1mA. VDDA = 2.7V.							
SID272	GBW_HI	power = hi	6	–	–	MHz	Input and output are 0.2 V to V_{DDA} – 0.2 V
SID273	GBW_MED	power = Med	3	–	–		
SID274	GBW_LO	power = Lo	–	1	–		
IOUT_MAX: VDDA=>2.7V, 500 mV from rail							
SID275	IOUT_MAX_HI	power = hi	10	–	–	mA	Output is 0.5 V V_{DDA} – 0.5 V
SID276	IOUT_MAX_MID	power = Med	10	–	–		
SID277	IOUT_MAX_LO	power = Lo	–	5	–		
IOUT: VDDA = 1.71V, 500 mV from rail							
SID278	IOUT_MAX_HI	power = hi	4.0	–	–	mA	Output is 0.5 V V_{DDA} – 0.5 V
SID279	IOUT_MAX_MID	power = Med	4	–	–		
SID280	IOUT_MAX_LO	power = Lo	–	2	–		
IDD_Int: Opamp block current. Internal load.							
SID269_I	IDD_HI_Int	power = Hi	–	1500	1700	µA	–
SID270_I	IDD_MED_Int	power = Med	–	700	980		–
SID271_I	IDD_LOW_Int	power = Lo	–	–	–		–
GBW: VDDA = 2.7V							
SID272_I	GBW_HI_Int	power = Hi	8	–	–	MHz	Output is 0.25 V to V_{DDA} – 0.25 V
SID273_I	GBW_MED_Int	power = Med	4	–	–		
SID274_I	GBW_LO_Int	power = lo	1	–	–		
General opamp specs for both internal and external modes							
SID281	VIN	Charge-pump ON, V_{DDA} => 2.7 V	-0.05	–	V_{DDA} -0.2	V	–
SID282	VCM	Charge-pump ON, V_{DDA} => 2.7 V	-0.05	–			–
VOUT: VDDA=> 2.7V							
SID283	VOUT_1	Power = Hi, Iload = 10mA	0.5	–	V_{DDA} -0.5	V	–
SID284	VOUT_2	Power =Hi, Iload = 1mA	0.2	–	V_{DDA} -0.2		–
SID285	VOUT_3	power = Med, Iload=1mA	0.2	–			–
SID286	VOUT_4	Power = Lo, Iload = 0.1mA	0.2	–			–
SID288	VOS_TR	Offset voltage, trimmed	-1	±0.5	1	mV	High mode, input 0 V to V_{DDA} – 0.2 V
SID288A	VOS_TR	Offset voltage, trimmed	–	+/-1	–		Medium mode, input 0 V to V_{DDA} – 0.2 V
SID288B	VOS_TR		–	+/-2	–		Low mode, input 0 V to V_{DDA} – 0.2 V

Table 11 Opamp specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID290	VOS_DR_TR	Offset voltage drift, trimmed	-10	+/-3	10	µV/C	High mode
SID290A	VOS_DR_TR		–	+/10	–		Medium mode
SID290B	VOS_DR_TR		–	+/-10	–		Low mode
SID291	CMRR	DC	70	80	–	dB	Input is 0 V to V_{DDA} – 0.2 V, Output is 0.2 V to V_{DDA} – 0.2 V
SID292	PSRR	At 1 kHz, 10 mV ripple	70	85	–		V_{DDD} = 3.6 V, high power mode, input is 0.2 V to V_{DDA} – 0.2 V
NOISE							
SID293	VN1	Input-referred, 1 Hz–1 GHz, power = Hi	–	94	–	µVrms	Input and Output are at 0.2 V to V_{DDA} – 0.2 V
SID294	VN2	Input-referred, 1 kHz, power = Hi	–	72	–	nV/rtHz	
SID295	VN3	Input-referred, 10 kHz, power = Hi	–	28	–		
SID296	VN4	Input-referred, 100 kHz, power = Hi	–	15	–		
SID297	CLOAD	Stable up to max. load. Performance specs at 50 pF	–	–	125	pF	–
SID298	SLEW_RATE	Cload = 50 pF, power = Hi, V_{DDA} => 2.7 V	4	–	–	V/µs	–
SID299	T_OP_WAKE	From disable to enable, no external RC dominating	–	–	25	µs	–
SID299A	OL_GAIN	Open loop gain	–	90	–	dB	–
COMP_MODE: Comparator mode; 50 mV drive, Trise = Tfall (approx.)							
SID300	TPD1	Response time; power = Hi	–	150	–	ns	Input is 0.2 V to V_{DDA} – 0.2 V
SID301	TPD2	Response time; power = Med	–	500	–		
SID302	TPD3	Response time; power = Lo	–	2500	–		
SID303	VHYST_OP	Hysteresis	–	10	–	mV	–
SID304	WUP_CTB	Wake-up time from enabled to usable	–	–	25	µs	–
DEEP SLEEP MODE: Mode 2 is lowest current range. Mode 1 has higher GBW							
SID_DS_1	IDD_HI_M1	Mode 1, high current	–	1400	–	µA	25°C
SID_DS_2	IDD_MED_M1	Mode 1, medium current	–	700	–		
SID_DS_3	IDD_LOW_M1	Mode 1, low current	–	200	–	µA	25°C
SID_DS_4	IDD_HI_M2	Mode 2, high current	–	120	–		
SID_DS_5	IDD_MED_M2	Mode 2, medium current	–	60	–		
SID_DS_6	IDD_LOW_M2	Mode 2, low current	–	15	–		
SID_DS_7	GBW_HI_M1	Mode 1, high current	–	4	–	MHz	20 pF load, no DC load, 0.2 V to V_{DDA} – 0.2 V
SID_DS_8	GBW_MED_m1	Mode 1, medium current	–	2	–		
SID_DS_9	GBW_LOW_M!	Mode 1, low current	–	0.5	–		
SID_DS_10	GBW_HI_M2	Mode 2, high current	–	0.5	–		
SID_DS_11	GBW_MED_M2	Mode 2, medium current	–	0.2	–		
SID_DS_12	GBW_Low_M2	Mode 2, low current	–	0.1	–		

Table 11 Opamp specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID_DS_13	VOS_HI_M1	Mode 1, high current	–	5	–	mV	With trim 25°C, 0.2 V to V_{DDA} – 0.2 V
SID_DS_14	VOS_MED_M1	Mode 1, medium current	–	5	–		
SID_DS_15	VOS_LOW_M2	Mode 1, low current	–	5	–		
SID_DS_16	VOS_HI_M2	Mode 2, high current	–	5	–		
SID_DS_17	VOS_MED_M2	Mode 2, medium current	–	5	–		
SID_DS_18	VOS_LOW_M2	Mode 2, low current	–	5	–		
SID_DS_19	IOUT_HI_M!	Mode 1, high current	–	10	–	mA	Output is 0.5 V to V_{DDA} – 0.5 V
SID_DS_20	IOUT_MED_M1	Mode 1, medium current	–	10	–		
SID_DS_21	IOUT_LOW_M1	Mode 1, low current	–	4	–		
SID_DS_22	IOUT_HI_M2	Mode 2, high current	–	1	–		–
SID_DS_23	IOU_MED_M2	Mode 2, medium current	–	1	–		–
SID_DS_24	IOU_LOW_M2	Mode 2, low current	–	0.5	–		–

6.4.1 Comparator

Table 12 Comparator DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID84	$V_{OFFSET1}$	Input offset voltage, factory trim	–	–	±10	mV	–
SID85	$V_{OFFSET2}$	Input offset voltage, custom trim	–	–	±4		–
SID86	V_{HYST}	Hysteresis when enabled	–	10	35		–
SID87	V_{ICM1}	Input common mode voltage in Normal mode	0	–	V_{DDD} – 0.1	V	Modes 1 and 2
SID247	V_{ICM2}	Input common mode voltage in Low-power mode	0	–	V_{DDD}		–
SID247A	V_{ICM3}	Input common mode voltage in Ultra low-power mode	0	–	V_{DDD} – 1.15		$V_{DDD} \geq 2.2$ V at –40°C
SID88	CMRR	Common mode rejection ratio	50	–	–	dB	$V_{DDD} \geq 2.7$ V
SID88A	CMRR	Common mode rejection ratio	42	–	–		$V_{DDD} \leq 2.7$ V
SID89	I_{CMP1}	Block current, Normal mode	–	–	400	µA	–
SID248	I_{CMP2}	Block current, Low-power mode	–	–	100		–
SID259	I_{CMP3}	Block current in Ultra low-power mode	–	6	28		$V_{DDD} \geq 2.2$ V at –40°C
SID90	Z_{CMP}	DC input impedance of comparator	35	–	–	MΩ	–

Table 13 Comparator AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID91	TRESP1	Response time, normal mode, 50 mV overdrive	–	38	110	ns	–
SID258	TRESP2	Response time, low power mode, 50 mV overdrive	–	70	200		–
SID92	TRESP3	Response time, ultra-low power mode, 200 mV overdrive	–	–	35	µs	$V_{DDD} \geq 2.2$ V at –40°C

6.4.2 Temperature sensor

Table 14 Temperature sensor specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID93	TSENSACC	Temperature sensor accuracy	–5	±1	5	°C	–40°C to +85°C

6.4.3 SAR ADC

Table 15 SAR ADC DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID94	A_RES	Resolution	–	–	12	bits	–
SID95	A_CHNLS_S	Number of channels - single ended	–	–	8		8 full speed
SID96	A-CHNKS_D	Number of channels - differential	–	–	4		Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	–		Yes.
SID98	A_GAINERR	Gain error	–	–	±0.1	%	With external reference
SID99	A_OFFSET	Input offset voltage. Guaranteed by characterization	–	–	2	mV	Measured with 1-V reference
SID100	A_ISAR	Current consumption	–	–	1	mA	–
SID101	A_VINS	Input voltage range - single ended	V_{SS}	–	V_{DDA}	V	–
SID102	A_VIND	Input voltage range - differential	V_{SS}	–	V_{DDA}		–
SID103	A_INRES	Input resistance	–	–	2.2	kΩ	–
SID104	A_INCAP	Input capacitance	–	–	10	pF	–
SID260	VREFSAR	Trimmed internal reference to SAR	1.18	1.2	1.22	V	–

Table 16 SAR ADC AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	–
SID107	A_CMRR	Common mode rejection ratio	66	–	–		Measured at 1 V
SID108	A_SAMP	Sample rate	–	–	1	Msps	–
SID109	A_SNR	Signal-to-noise and Distortion ratio (SINAD)	65	–	–	dB	Fin = 10 kHz
SID110	A_BW	Input bandwidth without aliasing	–	–	A_samp/2	kHz	–
SID111	A_INL	Integral non linearity. V_{DDD} = 1.71 to 5.5, 1 Msps	–1.7	–	2	LSB	VREF = 1 to V_{DDD}
SID111A	A_INL	Integral non linearity. V_{DDD} = 1.71 to 3.6, 1 Msps	–1.5	–	1.7		VREF = 1.71 to V_{DDD}
SID111B	A_INL	Integral non linearity. V_{DDD} = 1.71 to 5.5, 500 ksps	–1.5	–	1.7		VREF = 1 to V_{DDD}
SID112	A_DNL	Differential non linearity. V_{DDD} = 1.71 to 5.5, 1 Msps	–1	–	2.2		
SID112A	A_DNL	Differential non linearity. V_{DDD} = 1.71 to 3.6, 1 Msps	–1	–	2		VREF = 1.71 to V_{DDD}
SID112B	A_DNL	Differential non linearity. V_{DDD} = 1.71 to 5.5, 500 ksps	–1	–	2.2		VREF = 1 to V_{DDD}
SID113	A_THD	Total harmonic distortion	–	–	-65	dB	Fin = 10 kHz
SID261	FSARINTREF	SAR Operating speed without external ref. bypass	–	–	100	ksps	12-bit resolution

6.4.4 CSD

Table 17 CSD V2 specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SYS.PER#3	VDD_RIPPLE	Max allowed ripple on power supply, DC to 10 MHz	–	–	±50	mV	V_{DDD} > 2 V (with ripple), 25°C TA, Sensitivity = 0.1 pF
SYS.PER#16	VDD_RIPPLE_1.8	Max allowed ripple on power supply, DC to 10 MHz	–	–	±25		V_{DDD} > 1.75 V (with ripple), 25°C TA, parasitic capacitance (CP) < 20 pF, Sensitivity ≥ 0.4 pF
SID.CSD.BLK	ICSD	Maximum block current	–	–	4000	µA	Maximum block current for both IDACs in dynamic (switching) mode including comparators and switching current
SID.CSD#15	VREF	Voltage reference for CSD and comparator	0.6	1.2	VDDA - 0.6	V	V_{DDA} – 0.6 or 4.4, whichever is lower
SID.CSD#15A	VREF_EXT	External voltage reference for CSD and comparator	0.6	–	VDDA - 0.6		
SID.CSD#16	IDAC1IDD	IDAC1 (7-bits) block current	–	–	1750	µA	–
SID.CSD#17	IDAC2IDD	IDAC2 (7-bits) block current	–	–	1750		–
SID308	VCSD	Voltage range of operation	1.71	–	5.5	V	1.8 V ± 5% or 1.8 V to 5.5 V
SID308A	VCOMPIDAC	Voltage compliance range of IDAC	0.6	–	VDDA –0.6		V_{DDA} - 0.6 or 4.4,whichever is lower
SID309	IDAC1DNL	DNL	-1	–	1	LSB	–
SID310	IDAC1INL	INL	-2	–	2		INL is +/-5.5 LSB for V_{DDA} < 2 V
SID311	IDAC2DNL	DNL	-1	–	1		–
SID312	IDAC2INL	INL	-2	–	2		INL is +/-5.5 LSB for V_{DDA} < 2 V
SID313	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	Ratio	Capacitance range of 5 to 35 pF, 0.1 pF sensitivity. All use cases. V_{DDA} > 2 V
SID314	IDAC1CRT1	Output current of IDAC1 (7 bits) in low range	4.2	–	5.4	µA	LSB = 37.5 nA typ.
SID314A	IDAC1CRT2	Output current of IDAC1 (7 bits) in medium range	34	–	41		LSB = 300 nA typ.
SID314B	IDAC1CRT3	Output current of IDAC1 (7 bits) in high range	275	–	330		LSB = 2.4 µA typ.
SID314C	IDAC1CRT12	Output current of IDAC1 (7 bits) in low range, 2X mode	8	–	10.5		LSB = 75 nA typ.
SID314D	IDAC1CRT22	Output current of IDAC1 (7 bits) in medium range, 2X mode	69	–	82		LSB = 600 nA typ.
SID314E	IDAC1CRT32	Output current of IDAC1 (7 bits) in high range, 2X mode	540	–	660		LSB = 4.8 µA typ.
SID315	IDAC2CRT1	Output current of IDAC2 (7 bits) in low range	4.2	–	5.4		LSB = 37.5 nA typ.
SID315A	IDAC2CRT2	Output current of IDAC2 (7 bits) in medium range	34	–	41		LSB = 300 nA typ.
SID315B	IDAC2CRT3	Output current of IDAC2 (7 bits) in high range	275	–	330		LSB = 2.4 µA typ.
SID315C	IDAC2CRT12	Output current of IDAC2 (7 bits) in low range, 2X mode	8	–	10.5		LSB = 75 nA typ.

Table 17 CSD V2 specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID315D	IDAC2CRT22	Output current of IDAC2 (7 bits) in medium range, 2X mode	69	–	82	µA	LSB = 600 nA typ.
SID315E	IDAC2CRT32	Output current of IDAC2 (7 bits) in high range, 2X mode	540	–	660		LSB = 4.8 µA typ.
SID315F	IDAC3CRT13	Output current of IDAC in 8-bit mode in low range	8	–	10.5		LSB = 37.5 nA typ.
SID315G	IDAC3CRT23	Output current of IDAC in 8-bit mode in medium range	69	–	82		LSB = 300 nA typ.
SID315H	IDAC3CRT33	Output current of IDAC in 8-bit mode in high range	540	–	660		LSB = 2.4 µA typ.
SID320	IDACOFFSET	All zeros input	–	–	1	LSB	Polarity set by Source or Sink. offset is +/-2 LSBs for 37.5 nA LSB mode.
SID321	IDACGAIN	Full-scale error less offset	–	–	±10	%	–
SID322	IDACMIS-MATCH1	Mismatch between IDAC1 and IDAC2 in Low mode	–	–	9.2	LSB	LSB = 37.5 nA typ.
SID322A	IDACMIS-MATCH2	Mismatch between IDAC1 and IDAC2 in Medium mode	–	–	5.6		LSB = 300 nA typ.
SID322B	IDACMIS-MATCH3	Mismatch between IDAC1 and IDAC2 in High mode	–	–	6.8		LSB = 2.4 µA typ.
SID323	IDACSET8	Settling time to 0.5 LSB for 8-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID324	IDACSET7	Settling time to 0.5 LSB for 7-bit IDAC	–	–	10		
SID325	CMOD	External modulator capacitor	–	2.2	–	nF	5-V rating, X7R or NP0 cap.

6.5 Digital peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

6.5.1 Timer/counter/PWM

Table 18 TCPWM specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.TCPWM#1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	µA	All modes (Timer/counter/PWM)
SID.TCPWM#2	ITCPWM2	Block current consumption at 12 MHz	–	–	155		
SID.TCPWM#2A	ITCPWM3	Block current consumption at 48 MHz	–	–	650		
SID.TCPWM#3	TCPWMFREQ	Operating frequency	–	–	Fc	MHz	Fc max = Fcpu. Maximum = 48 MHz
SID.TCPWM#4	TPWMENEXT	Input trigger pulse width for all trigger[7] events	2/Fc	–	–	ns	Trigger events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.
SID.TCPWM#5	TPWMEXT	Output trigger * pulse widths	2/Fc	–	–		Minimum possible width of Overflow, underflow, and CC (Counter equals Compare value) trigger outputs
SID.TCPWM#5A	TCRES	Resolution of counter	1/Fc	–	–		Minimum time between successive counts
SID.TCPWM#5B	PWMRES	PWM resolution	1/Fc	–	–		Minimum pulse width of PWM Output
SID.TCPWM#5C	QRES	Quadrature inputs resolution	1/Fc	–	–		Minimum pulse width between Quadrature phase inputs

Note
7. Trigger events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.

6.5.2 I²C

Table 19 Fixed I²C DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID149	II2C1	Block current consumption at 100 kHz	–	–	60	µA	–
SID150	II2C2	Block current consumption at 400 kHz	–	–	185		–
SID151	II2C3	Block current consumption at 1 Mbps	–	–	650		–
SID152	II2C4	Block current consumption when I2C enabled in Deep Sleep mode	–	1	–		–

Table 20 Fixed I2C AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID153	FI2C1	Bit Rate	–	–	1	Mbps	–
SID.I2C#1	FSCLI2C_SM	I2C SCL clock frequency	0	–	100	kHz	Standard Mode
SID.I2C#2	FSCLI2C_FM		0	–	400		Fast Mode
SID.I2C#33	FSCLI2C_FMP		0	–	1000		Fast Mode Plus
SID.I2C#3	THDSTAI2C_SM	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4	–	–	µs	Standard Mode
SID.I2C#4	THDSTAI2C_FM		0.6	–	–		Fast Mode
SID.I2C#34	THDSTAI2C_FMP		0.26	–	–		Fast Mode Plus
SID.I2C#5	TSUSTAI2C_SM	Setup time for a repeated START condition	4.7	–	–		Standard Mode
SID.I2C#6	TSUSTAI2C_FM		0.6	–	–		Fast Mode
SID.I2C#35	TSUSTAI2C_FMP		0.26	–	–		Fast Mode Plus
SID.I2C#7	TLOWI2C_SM	LOW period of the SCL clock	4.7	–	–		Standard Mode
SID.I2C#8	TLOWI2C_FM		1.3	–	–		Fast Mode
SID.I2C#36	TLOWI2C_FMP		0.5	–	–		Fast Mode Plus
SID.I2C#9	THIGHI2C_SM	HIGH period of the SCL clock	4	–	–		Standard Mode
SID.I2C#10	THIGHI2C_FM		0.6	–	–		Fast Mode
SID.I2C#37	THIGHI2C_FMP		0.3	–	–		Fast Mode Plus
SID.I2C#11	THDDATI2C	Data hold time	0	–	–		All I2C Speeds
SID.I2C#12	TSUDATI2C_SM	Data setup time	250.0	–	–		Standard Mode
SID.I2C#13	TSUDATI2C_FM		100	–	–		Fast Mode
SID.I2C#38	TSUDATI2C_FMP		50	–	–		Fast Mode Plus
SID.I2C#14	TSUSTOI2C_SM	Setup time for I2C STOP condition	4	–	–		Standard Mode
SID.I2C#15	TSUSTOI2C_FM		0.6	–	–		Fast Mode
SID.I2C#39	TSUSTOI2C_FMP		0.26	–	–	µs	Fast Mode Plus
SID.I2C#16	CB_SM	Capacitive load for each I2C bus line	–	–	400	pF	Standard Mode
SID.I2C#17	CB_FM		–	–	400		Fast Mode
SID.I2C#40	CB_FMP		–	–	550		Fast Mode Plus
SID.I2C#18	TVDDATI2C_SM	Data valid time	–	–	3.45	µs	Standard Mode
SID.I2C#19	TVDDATI2C_FM		–	–	0.9		Fast Mode
SID.I2C#41	TVDDATI2C_FMP		–	–	0.45		Fast Mode Plus
SID.I2C#20	TVDACKI2C_SM	Data valid acknowledge time	–	–	3.45		Standard Mode
SID.I2C#21	TVDACKI2C_FM		–	–	0.9		Fast Mode
SID.I2C#42	TVDACKI2C_FMP		–	–	0.45		Fast Mode Plus

Table 20 Fixed I2C AC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.I2C#22	TSPI2C_FM	Pulse width of spikes suppressed by input filter	–	–	50	ns	Fast Mode
SID.I2C#43	TSPI2C_FMP		–	–	50		Fast Mode Plus
SID.I2C#23	TBUFI2C_SM	Bus free time between a STOP and START condition	4.7	–	–	µs	Standard Mode
SID.I2C#24	TBUFI2C_FM		1.3	–	–	µs	Fast Mode
SID.I2C#44	TBUFI2C_FMP		0.5	–	–		Fast Mode Plus
SID.I2C#25	VIL_I2C	Input low voltage	–0.5	–	0.3 × V_{DDIO}	V	Fast and Standard mode I^2C speeds
SID.I2C#26	VIH_I2C	Input high voltage	0.7 × V_{DDIO}	–	–		Fast and Standard mode I^2C speeds
SID.I2C#27	VOL_I2C_L	Output low voltage, low supply range	–	–	0.2 × V_{DDIO}		Fast and Standard mode I^2C Speeds, V_{DDIO} < 2 V, 2 mA Sink
SID.I2C#28	VOL_I2C_H	Output low voltage, high supply range	–	–	0.4		Fast and Standard mode I^2C speeds, V_{DDIO} < 2 V, 2 mA sink
SID.I2C#29	IOL_I2C_SM	I2C output low current	3	–	–	mA	Standard mode, 1.71 V ≤ V_{DDIO} ≤ 5.5 V, load = CB_SM, VOL = 0.4 V
SID.I2C#30	I2C_VHYS_HV	I2C input hysteresis	0.05 × VDDIO	–	–	mV	Fast and Standard mode I^2C speeds, 2 V ≤ V_{DDIO} ≤ 4.5 V
SID.I2C#30A	I2C_VHYS_5V		200	–	–		Fast and Standard mode I^2C speeds, V_{DDIO} > 4.5 V
SID.I2C#31	I2C_VHYS_LV		0.10 × VDDIO	–	–		Fast and Standard mode I^2C speeds, V_{DDIO} < 2 V
COM.REQ#7	I2C_ADD	I2C address width	–	–	8	bits	7-bit address and 1 RW bit
SID.I2C#32	IOL_I2C_FM	I2C output low current	6	–	–	mA	Fast mode, 1.71 V ≤ V_{DDIO} ≤ 5.5 V, load = CB_SM, VOL = 0.6 V
SID.I2C#45	IOL_I2C_FMP	I2C output low current, high voltage range	20	–	–	mA	Fast Mode Plus, 3.0 V ≤ V_{DDD} ≤ 5.5 V, load = CB_FMP, –40°C to 85°C TA, GPIO_FAILSAFE port only
SID.I2C#45A	IOL_I2C_FMP	I2C output low current, low voltage range	3	–	–	mA	Fast Mode Plus, 1.71 V ≤ V_{DDD} ≤ 3.0 V, load = CB_FMP, –40°C to 85°C TA

6.5.3 UART

Table 21 Fixed UART DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID160	IUART1	Block current consumption at 100 Kbps	–	–	125	µA	–
SID161	IUART2	Block current consumption at 1000 Kbps	–	–	312		–

Table 22 Fixed UART AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID162	FUART	Bit Rate	–	–	1	Mbps	–

6.5.4 SPI

Table 23 Fixed SPI DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID163	ISPI1	Block current consumption at 1 Mbps	–	–	360	µA	–
SID164	ISPI2	Block current consumption at 4 Mbps	–	–	560		–
SID165	ISPI3	Block current consumption at 8 Mbps	–	–	600		–

Table 24 Fixed SPI AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID166	FSPI	SPI operating frequency (master; 6X oversampling)	–	–	8	MHz	–

Table 25 Fixed SPI master mode AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID167	TDMO	MOSI valid after SClock driving edge	–	–	15	ns	–
SID168	TDSI	MISO valid before SClock capturing edge	20	–	–		Full clock, late MISO sampling
SID169	THMO	Previous MOSI data hold time	0	–	–		Referred to Slave capturing edge

Table 26 Fixed SPI slave mode AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID170	TDMI	MOSI valid before Sclock capturing edge	40	–	–	ns	–
SID171	TDSO	MISO valid after Sclock driving edge	–	–	48 + (3 × Tcpu)		Tcpu = 1/Fcpu
SID171A	TDSO_EXT	MISO valid after Sclock driving edge in Ext. Clk. mode	–	–	48		–
SID172	THSO	Previous MISO data hold time	0	–	–		–
SID172A	TSSELSCK	SSEL valid to first SCK valid edge	100	–	–		–

6.5.5 Memory

Table 27 Flash DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID173	V_{PE}	Erase and program voltage	1.71	–	5.5	V	–
SID173A	I_{PW}	Page write current at 16 MHz	–	–	3.5	mA	5.5 V V_{DDD}

Table 28 Flash AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID174	$T_{ROWWRITE}$	Row (block) write time (erase and program)	–	–	20	ms	Row (Block) = 256 bytes
SID175	$T_{ROWERASE}$	Row erase time	–	–	16		–
SID176	$T_{ROWPROGRAM}$	Row program time after erase	–	–	7		–
SID178	$T_{BULKERASE}$	Bulk erase time (32K bytes)	–	–	35		–
SID180	$T_{DEVPROG}$	Total device program time	–	–	7	seconds	–
SID181	F_{END}	Flash endurance	100K	–	–	cycles	–
SID182	F_{RET}	Flash retention. TA ≤ 55°C, 100K P/E cycles	20	–	–	years	–
SID182a		Flash retention. TA ≤ 85°C, 10K P/E cycles.	10	–	–		–
SID256	T_{WS48}	Number of wait states at 48 MHz	2	–	–		CPU execution from flash
SID257	T_{WS24}	Number of wait states at 24 MHz	1	–	–		

6.6 System resources

6.6.1 Power-on-reset with brown-out DC specifications

Table 29 Power-on-reset specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.POR#1	SR_ POWER_UP	Power supply slew rate	1	–	67	V/ms	–40°C to +85°C TA, All V_{DDD}; at power-up
SID.POR#2	$V_{RISEIPOR}$	Rising trip voltage	0.8	–	1.5	V	–
SID.POR#3	$V_{FALLIPOR}$	Falling trip voltage	0.7	–	1.4		–

Table 30 Brown-out detect (BOD) for VCCD

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.BOD#1	$V_{FALLPPOR}$	BOD trip voltage in Active and Sleep modes	1.48	–	1.62	V	–
SID.BOD#2	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep	1.1	–	1.5		–

6.6.2 SWD

Table 31 SWD interface

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.SWD#1	F_SWDCLK1	3.3 V ≤ V_{DDD} ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 FCPU
SID.SWD#2	F_SWDCLK2	1.71 V ≤ V_{DDD} ≤ 3.3 V	–	–	7		
SID.SWD#3	T_SWDI_ SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
SID.SWD#4	T_SWDI_ HOLD		0.25 × T	–	–		–
SID.SWD#5	T_SWDO_ VALID		–	–	0.5 × T		–
SID.SWD#6	T_SWDO_ HOLD		1	–	–		–

6.6.3 Internal main oscillator

Table 32 IMO DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.IMO.DC#1	IIMO1	IMO operating current at 48 MHz	–	–	250	µA	–
SID.IMO.DC#2	IIMO2	IMO operating current at 24 MHz	–	–	180		–

Table 33 IMO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.IMO.AC#1	FIMO	IMO frequency	–	48	–	MHz	–40°C to +85°C TA, All V_{DDD}
SID.IMO.AC#2	FIMO_RES	IMO frequency resolution	–	0.25	–	%	
SID.IMO.AC#3	IMO_STL	IMO settling time when trim register is changed	–	–	200	ns	25°C TA, All V_{DDD}, FIMO = 48 MHz
SID.IMO.AC#4	FIMOTOL1	Frequency variation at 24, 32 and 48 MHz (trimmed)	–	–	±2	%	2.7 V ≤ V_{DDD} < 5.5 V. –25°C ≤ TA ≤ 85°C
SID.IMO.AC#4a	FIMOTOLVCCD		–	–	±4		All conditions
SID.IMO.AC#5	IMO_HOP_ RANGE	FIMO variation range with TRIM registers	–10	–	10		25°C TA, All V_{DDD}, 48 MHz = F_{IMO}
SID.IMO.AC#6	TSTARTIMO	IMO startup time	–	–	7	µs	–
SID.IMO.AC#7	TJITRMSIMO2	RMS jitter at 24 MHz	–	145	–	–	–

6.6.4 Internal low-speed oscillator

Table 34 ILO DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.ILO.DC#1	IILO1	ILO operating current at 32 kHz	–	0.3	1.05	µA	–
SID.ILO.DC#2	IILOLEAK	ILO leakage current	–	2	15	nA	–

Table 35 ILO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.ILO.AC#1	FILO	Operating frequency	20.0	40.0	80.0	kHz	–
SID.ILO.AC#2	TSTARTILO1	ILO start-up time	–	–	2	ms	–
SID.ILO.AC#3	TLIODUTY	ILO duty cycle	40	50	60	%	–

6.7 USBDPD peripherals

6.7.1 Analog to digital converter

Table 36 ADC DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.ADC.DC#1	Resolution	ADC resolution	–	–	–	–	–
SID.PD.ADC.DC#2	INL	Integral non-linearity	–1.5	–	1.5	LSB	–
SID.PD.ADC.DC#3	DNL	Differential non-linearity	–2.5	–	2.5		–
SID.PD.ADC.DC#4	Gain Error	Gain error	–1.5	–	1.5		–
SID.PD.ADC.DC#5	VREF_ADC1	Reference voltage of ADC	V_{DDDmin}	–	V_{DDDmax}	V	Reference voltage generated from V_{DDD}
SID.PD.ADC.DC#6	VREF_ADC2		1.96	2	2.04		Reference voltage generated from Deep Sleep reference

Table 37 ADC DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.ADC.AC#7	SLEW_Max	Rate of change of sampled voltage signal	–	–	3	V/ms	–

6.7.2 VBUS regulator

Table 38 VBUS regulator DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.20VREG.DC#1	VBUSREG1	VBUS regulator output voltage (minimum VBUS = 4.2 V to 28 V)	3	–	3.65	V	Chip powered through VBUS_C_P1/VBUS_C_P2 and output measured on V_{DDD}
SID.PD.20VREG.DC#2	VBUSREG2	VBUS regulator output voltage (minimum VBUS = 4 V to 4.2 V)					

Table 39 VBUS regulator AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.20VREG.AC#1	Tstart	Total start up time for the regulator supply outputs	–	–	200	µs	Apply VBUS and measure start time on VDDD pin
SID.PD.20VREG.AC#2	Tstop	Regulator power down time from vreg_en = 0 to regulator disable	–	–	4		Time from assertion of an internal disable signal for load current on V_{DDD} to decrease from 30 mA to 10 µA

6.7.3 CSA

Table 40 CSA specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.HS-CSA.DC#1	Isense_scp	Current sense accuracy for SCP at 6 A, 10 A	–	±10	–	%	–
SID.PD.HS-CSA.DC#1a	Isense_scp_epr		–	±12	–		For 30-V EPR
SID.PD.HS-CSA.DC#2	Vsense_rcp	RCP sensing threshold across “Rsense”	–	2	4	mV	–
SID.PD.HS-CSA.DC#3a	Isense_ocp_2A	Current sense accuracy for OCP at 2 A, 3 A, and 4 A	–	±15	–	%	–
SID.PD.HS-CSA.DC#3b	Isense_ocp_5A	Current sense accuracy for OCP at 5 A	–	±10	–		–
SID.PD.HS-CSA.DC#3c	Isense_ocp_5A_epr		–	±12	–		For 30-V EPR
SID.PD.HS-CSA.DC#3	Isense_ocp_1A	Current sense accuracy for OCP at 1 A	–	±20	–		–
SID.PD.HS-CSA.DC#4	Rsense	External Rsense	4.95	5	5.05	mΩ	–
SID.PD.HS-CSA.DC#5	Vtrip_slow_rcp_33pct	Slow RCP trip points set at 5V with 33% tap point selected	4.5	–	5.5	V	–
SID.PD.HS-CSA.DC#5a	Vtrip_slow_rcp_10pct	Slow RCP trip points set at 20V with 10% tap point selected	18	–	22		–
SID.PD.HS-CSA.DC#5b	Vtrip_slow_rcp_6pct	Slow RCP trip points set at 30V with 60% tap point selected	27	–	33		–
SID.PD.HS-CSA.DC#9	Isb_csp_5v	CSP pin input leakage when SCP, OCP and RCP blocks are OFF	–	–	6	µA	CSP = CSN = 5 V
SID.PD.HS-CSA.DC#10	Isb_csn_5v		–	–	5		
SID.PD.HS-CSA.DC#9a	Isb_csp_30v		–	–	26		CSP = CSN = 30 V
SID.PD.HS-CSA.DC#10a	Isb_csn_30v		–	–	5		
SID.PD.HS-CSA.DC#17	I_CSP_SCP_ON_OCP_ON_RCP_ON	CSP pin current when SCP, OCP and RCP blocks are ON	–	–	500	µA	–
SID.PD.HS-CSA.DC#18	I_CSN _SCP_ON_OCP_ON_RCP_ON		–	–	65		–
SID.PD.HS-CSA.AC#1	Tdelay_scp_6A	SCP delay in 6 A mode (5-mV overdrive)	–	–	300	ns	Guaranteed By design
SID.PD.HS-CSA.AC#2	Tdelay_scp_10A	SCP delay in 10 A mode (5-mV overdrive)	–	–	300		
SID.PD.HS-CSA.AC#3	Tdelay_rcp	RCP delay (5-mV overdrive)	–	–	250		
SID.PD.HS-CSA.AC#4	Tdelay_ocp	OCP delay (5-mV overdrive)	–	–	250		

6.7.4 VBUS discharge

Table 41 VBUS discharge specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.VBUS_DISC#1	Ron1	20 V NMOS ON resistance (with dischg_ds<0> = 1; dischg_ds<4:1> = 0)	1500	–	3000	Ω	–
SID.PD.VBUS_DISC#2	Ron2	20 V NMOS ON resistance (with dischg_ds<1:0> = 1; dischg_ds<4:2> = 0)	750	–	1500		–
SID.PD.VBUS_DISC#3	Ron3	20 V NMOS ON resistance (with dischg_ds<2:0> = 1; dischg_ds<4:3> = 0)	500	–	1000		–
SID.PD.VBUS_DISC#4	Ron4	20 V NMOS ON resistance (with dischg_ds<3:0> = 1; dischg_ds<4> = 0)	375	–	750		–
SID.PD.VBUS_DISC#5	Ron5	20 V NMOS ON resistance (with dischg_ds<4:0> = 1)	300	–	600		–

6.7.5 UVOV

Table 42 UVOV specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.UVOV#1	VTHUVOV1	Voltage threshold accuracy - in Active mode using bandgap ref	–	+/-3	–	%	–
SID.PD.UVOV#2	VTHUVOV2	Voltage threshold accuracy - in Deep Sleep mode using Deep Sleep references	–	+/-5	–		–
SID.PD.COMP_ACC#1	COMP_ACC	Comparator input offset at 4 sigma	–15	–	15.0	mV	–
SID.PD.UVOV.AC#1	Tov_gate	Delay from 0 V threshold trip to external NFET power gate turn off	–	–	50	µs	–

6.7.6 SBU

Table 43 SBU switch specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.SBU.DC#1	Ron_hs1	Switch on resistance in HS range (input from 0 V to 0.4 V range)	–	–	4.5	Ω	–
SID.PD.SBU.DC#2	Ron_fs	Switch on resistance in FS range (input from 0 V to 3.6 V range)	–	–	6.5		–
SID.PD.SBU.DC#3	Ron_flat_hs1	Switch flat resistance in HS range (input from 0 V to 0.4 V range)	–	–	0.5		–
SID.PD.SBU.DC#4	Ron_flat_fs	Switch flat resistance in FS range (input from 0 V to 3.6 V range)	–	–	2.5		–
SID.PD.SBU.DC#7	Ileak1	Pin leakage current for SBU1, SBU2 @ 3.6 V with AUX_P/AUX_N floating, V_{DDD} = 3.3 V @ 85°C	–4.5	–	4.5	µA	–
SID.PD.SBU.DC#7a	Ileak2	Pin leakage current for AUX_P/AUX_N @ 3.6 V with SBU1, SBU2 floating, V_{DDD} = 3.3 V @ 85°C	–1	–	1		–
SID.PD.SBU.DC#8	Rpu_aux_1	Pull up resistance on AUX_N	80	–	120	kΩ	–
SID.PD.SBU.DC#9	Rpu_aux_2	Pull up resistance on AUX_P	0.8	–	1.2	MΩ	–
SID.PD.SBU.DC#10	Rpd_aux_1	Pull down resistance on AUX_P	80	–	120	kΩ	–
SID.PD.SBU.DC#11	Rpd_aux_2	Pull down resistance on AUX_N	0.8	–	1.2	MΩ	–
SID.PD.SBU.DC#12	Rpd_aux_3	Pull down resistance on AUX_P	329	–	611	kΩ	–
SID.PD.SBU.DC#13	Rpd_aux_4	Pull down resistance on AUX_N	3.29	–	6.11	MΩ	–
SID.PD.SBU.AC#1	Con	Switch on capacitance	–	–	50	pF	–
SID.PD.SBU.AC#2	Coff	Switch off capacitance- connector side	–	–	25		–
SID.PD.SBU.AC#3	Off_isolation	Switch isolation at F = 1 MHz	–	–	–50	dB	Guaranteed by design
SID.PD.SBU.AC#4	X_talk_AC	Cross talk of switch at F = 1 MHz IN1/2 to IN2/1 when is data transferred from OUT	–	–	–50		

6.7.7 VCONN switch

Table 44 VCONN switch specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.VCONN.DC#1	Ron	Switch ON resistance at V5V = 5 V with 215 mA load current	–	0.7	1.3	Ω	–
SID.PD.VCONN.DC#3	Ileak	Connector side pin leakage current	–	–	10	µA	–
SID.PD.VCONN.DC#4	VTHDETECT_V5V	Threshold voltage of the v5v detector	2.05	–	2.65	V	–
SID.PD.VCONN.DC#9	Iocp	Overcurrent detection range for CC1/CC2	550	–	–	mA	–
SID.PD.VCONN.DC#12	OCP_hysteresis	Overcurrent detection hysteresis	20	–	80		–
SID.PD.VCONNAC#1	Ton	Switch turn-on time	–	–	200	µs	–
SID.PD.VCONNAC#2	Toff	Switch turn-off time	–	–	3		–
SID.PD.VCONN.DC#14	Rfrs_pd	Fast role swap request transmit driver resistance (excluding cable resistance)	–	–	5	Ω	–

6.7.8 VSYS

Table 45 VSYS regulator

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.vdddsw.DC#1	Res_sw	Resistance from supply input to the output supply V_{DDD}	–	–	1.5	Ω	Measured with a load current of 5 mA to 10 mA on V_{DDD}.

6.7.9 Gate driver specifications

Table 46 NFET gate driver

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.GD#1	GD_VGS	Gate to source overdrive during ON condition	4.5	–	10.5	V	NFET driver is ON
SID.PD.GD#3	GD_VGS_OFF	External-FET gate to source during OFF condition	VBUS_NGDO_ABS	–	+VBUS_NGDO_ABS		External NFET must be able to tolerate “VGS<–VBUS_NGDO_ABS” in OFF state as the Gate is pulled-down to “0 V”
SID.PD.GD#11	ISB_VBUS_IN_NGDO	Leakage current from VBUS_IN_NGDO when NGDO is lowest power state (disabled)	–	–	70	µA	VBUS_IN_NGDO = 5 V; en_hv = 1, ngdo_en = 1, keepoff_dis = 1, cp_en = 0, gdrv_en = 0, en_g1_chrg = 0, equalizers-off
SID.PD.GD#11a	Ixres_VBUS_IN_NGDO	Leakage current from VBUS_IN_NGDO when chip XRES asserted	–	–	650		VBUS_IN_NGDO = 5 V; Chip XRES asserted; Guaranteed by design
SID.PD.GD#12	ISB_VBUS_OUT_NGDO	Leakage current from VBUS_OUT_NGDO when NGDO is lowest power state (disabled)	–	–	140		VBUS_OUT_NGDO = 5 V; en_hv = 1, ngdo_en = 1, keepoff_dis = 1, cp_en = 0, gdrv_en = 0, en_g1_chrg = 0, equalizers-off
SID.PD.GD#12a	Ixres_VBUS_OUT_NGDO	Leakage current from VBUS_OUT_NGDO when chip XRES asserted	–	–	500		VBUS_OUT_NGDO = 5 V; Chip XRES asserted; Guaranteed by design
SID.PD.ngdo_fet_sys.AC#2	Ton	NGDO turn-on time (VBUS_IN_NGDO = 5 V)	–	10	–	ms	Time taken for VBUS_CTRL_1 to rise from 0.5 to VBUS_IN_NGDO+1V with 3nF load cap
SID.PD.ngdo_fet_sys.AC#3	Toff	NGDO turn-off time (non-fault) (VBUS_IN_NGDO = 5 V)	–	7	–	µs	Time taken for VBUS_CTRL_1 to fall from VBUS_IN_NGDO + 10 V to VBUS_OUT_NGDO (10 µF cap) with 3 nF load cap
SID.PD.ngdo_fet_sys.AC#4	Toff-fault	NGDO turn-off in response to SCP/RCP events (VBUS_IN_NGDO = 5 V)	–	1	–		NGDO turning off by VGS equalization of VBUS_CTRL_0 pin in response to RCP Event NGDO turning off by VBUS_CTRL_1 = 0.8 V for in response to SCP event

Table 47 CC-PHY PD specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.cc_shvt.DC#1	vSwing	Transmitter output high voltage	1.05	–	1.2	V	–
SID.PD.cc_shvt.DC#2	vSwing_low	Transmitter output low voltage	–	–	0.075		–
SID.PD.cc_shvt.DC#3	zDriver	Transmitter output impedance	33	–	75	Ω	–
SID.PD.cc_shvt.DC#4	zBmcRx	Receiver input impedance	10	–	–	MΩ	Guaranteed by design
SID.PD.cc_shvt.DC#5	Idac_std	Source current for USB standard advertisement	64	–	96	µA	–
SID.PD.cc_shvt.DC#6	Idac_1p5a	Source current for 1.5A @ 5 V advertisement	165.6	–	194.4		–
SID.PD.cc_shvt.DC#7	Idac_3a	Source current for 3A @ 5 V advertisement	303.6	–	356.4		–
SID.PD.cc_shvt.DC#8	Rd	Pull down termination resistance when acting as upstream facing port (UFP)	4.59	–	5.61	kΩ	–
SID.PD.cc_shvt.DC#9	Rd_db	Pull down termination resistance when acting as UFP, with dead battery (upstream facing port)	4.08	–	6.12		–
SID.PD.cc_shvt.DC#10	zOPEN	CC impedance to ground when disabled	108	–	–		–
SID.PD.cc_shvt.DC#11	DFP_ default_0p2	CC voltages on DFP side-Standard USB	0.15	–	0.25	V	–
SID.PD.cc_shvt.DC#12	DFP_1.5A_0p4	CC voltages on DFP side - 1.5 A	0.35	–	0.45		–
SID.PD.cc_shvt.DC#13	DFP_3A_0p8	CC voltages on DFP side - 3 A	0.75	–	0.85		–
SID.PD.cc_shvt.DC#14	DFP_3A_2p6		2.45	–	2.75		–
SID.PD.cc_shvt.DC#15	UFP_de- fault_0p66	CC voltages on UFP side-Standard USB	0.61	–	0.7		–
SID.PD.cc_shvt.DC#16	UFP_1.5A_ 1p23	CC voltages on UFP side - 1.5 A	1.16	–	1.31		–
SID.PD.cc_shvt.DC#17	Vattach_ds	Deep Sleep attach threshold	0.3	–	0.6	%	–
SID.PD.cc_shvt.DC#18	Rattach_ds	Deep Sleep pull-up resistor	10	–	50	kΩ	–
SID.PD.cc_shvt.DC#19	VTX_step	TX drive voltage step size	80	–	120	mV	No for user and datasheet
SID.PD.cc_shvt.DC#30	FS_0p53	Voltage threshold for fast swap detect	0.49	–	0.58	V	–

6.7.10 Charger detect

Table 48 Charger-detect DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.PD.chgdet.DC#1	VDAT_REF	Data detect voltage in charger detect mode	250	–	400	mV	–
SID.PD.chgdet.DC#2	VDM_SRC	dn voltage source in charger detect mode	500	–	700		–
SID.PD.chgdet.DC#3	VDP_SRC	dp voltage source in charger detect mode	500	–	700		–
SID.PD.chgdet.DC#4	IDM_SINK	dn sink current in charger detect mode	25	–	175	µA	–
SID.PD.chgdet.DC#4a	IDM_SINK_trim	dn sink current in 35 µA current mode	25	–	45		VDAT_SINK ≥ 0.2 5 V
SID.PD.chgdet.DC#5	IDP_SINK	dp sink current in charger detect mode	25	–	175		–
SID.PD.chgdet.DC#5a	IDP_SINK_trim	dp sink current in 35 µA current mode	25	–	45		VDAT_SINK ≥ 0.25 V
SID.PD.chgdet.DC#6	IDP_SRC	Data contact detect current source	7	–	13		–
SID.PD.chgdet.DC#27	RDP_UP	Qualcomm pull-up termination on dp/dm	0.9	–	1.575	kΩ	–
SID.PD.chgdet.DC#32	RDM_UP	Dp/Dm pull-up voltage	0.9	–	1.575		–
SID.PD.chgdet.DC#28	RDP_DWN	Qualcomm pull-down termination on dp/dm	14.25	–	24.8		–
SID.PD.chgdet.DC#31	RDM_DWN	Dp/Dm pull-down resistance	14.25	–	24.8		–
SID.PD.chgdet.DC#29	RDAT_LKG	Data line leakage on dp/dm	300	–	500		–
SID.PD.chgdet.DC#34	VSETH	Logic threshold	1.26	–	1.54	V	–
SID.PD.chgdet_afc.DC#30	RLOAD_DET	AFC Rload detect threshold. vpwrhv > 2.6 V.	1.4	–	2		–
SID.PD.chgdet_afc.DC#31	VAFC_TX_HI	AFC TX valid output high. vpwrhv > 2.6 V.	1.44	–	–		–
SID.PD.chgdet_afc.DC#32	VAFC_TX_LO	AFC TX valid output low. vpwrhv > 2.6V.	–	–	0.16		–
SID.PD.chgdet_afc.DC#33	VAFC_VIH	AFC RX valid input high. vpwrhv > 2.6 V.	–	–	1		–
SID.PD.chgdet_afc.DC#34	VAFC_VIL	AFC RX valid input low. vpwrhv > 2.6 V.	0.4	–	–		–
SID.PD.chgdet_afc.DC#35	SAMS_RCVR_ HYS	Samsung receiver hysteresis. vpwrhv > 2.6 V.	10	–	–	mV	–
SID.PD.chgdet_afc.DC#36	VQCOM_VIH	QCOM RX valid input high. vpwrhv > 2.6 V.	–	–	2	V	–
SID.PD.chgdet_afc.DC#37	VQCOM_VIL	QCOM RX valid input low. vpwrhv > 2.6 V.	0.8	–	–		–
SID.PD.chgdet_afc.DC#38	QCOM_RCVR_ HYS	Qualcomm receiver hysteresis. vpwrhv > 2.6 V.	10	–	–	mV	–
SID.PD.ccg6.dpdm.DC#14	RDCP_DAT	Dedicated charging port resistance across DP and DN	–	–	40	Ω	–

Table 49 Charger-detect AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.PD.chgdet_afc.AC#4	Trise	AFC TX D- rise time. vpwrhv > 2.7 V.	0.5	–	3.6	µs	–
SID.PD.chgdet_afc.AC#.5	Tfall	AFC TX D- fall time. vpwrhv > 2.7 V.	0.5	–	3.6		–
SID.PD.chgdet.AC#6	AFC_DATA_RATE	Data toggling rate for AFC for transmitting and receiving. vddd > 2.7 V.	35	–	45		–

7 Ordering information

PMG1-S3 part numbers and features are listed in the following table.

Table 50 PMG1-S3 MPN features

Product	GPIO				SCB			Programmable analog					
	GPIO (TOTAL)	GPIO (VDDIO)	Fail-Safe GPIO (VDDIO)	GPIO (VDDD)	I^2C	SPI	UART	12-Bit SAR ADC inputs	12-Bit SAR ADC output	SAR ADC VREF	Opamps	LP-Comp	TCPWM
CYPM1311-48LDXI CYPM1311-48LDXIT	26	19	2	5	7	5	5	4	0	1	2	2	8 (TCPWM1 output pins are not available)
CYPM1322-97BZXI CYPM1322-97BZXIT	50	36	2	12	8	8	8	8	1	1	2	2	8
CYPM1321-97BZXI CYPM1321-97BZXIT	50	36	2	12	8	8	8	8	1	1	2	2	8

Product	Type-C ports	Dead battery terminations	Termination resistors	SBU - MUX	VCONN	SCP/RCP/OCP	NGDO	20Vreg	VDDD switch	8-bit PD ADC	FS-PHY	Charger detect	Role	Package	Silicon ID
CYPM1311-48LDXI CYPM1311-48LDXIT	1	Yes	R_P, R_D, R_{D-DB}	0	1	1	1	1	1	1	1	1	DRP	48-pin QFN	0×3501
CYPM1322-97BZXI CYPM1322-97BZXIT	2	No	R_P, R_D	2	2	2	2	2	1	2	1	1	DRP	97-ball BGA	0×3500
CYPM1321-97BZXI CYPM1321-97BZXIT	2	Yes	R_P, R_D, R_{D-DB}	2	2	2	2	2	1	2	1	1	DRP	97-ball BGA	0×3521

7.1 Ordering code definitions

The part numbers are of the form CYPM1ABC-DEFGHIJ where the fields are defined as follows.

Field	Description	Values	Meaning
CY	CYPRESS™ prefix	CY	Company ID
PM	Marketing code	PM	PM = Power delivery MCU family
1	PM Gen 1 family	1	Product family generation
A	Family	0	S0
		1	S1
		2	S2
		3	S3
B	PD Ports	1	1-PD port
		2	2-PD port
C	Application specific	X	Application specific
DE	Pin	XX	Number of pins in the package
FG	Package code	LD	QFN
		BZ	BGA
		FN	CSP
H	Lead free	X	Lead: X = Pb-free
I	Temperature range	I	Industrial
J	Only for T&R	T	Tape and reel

8 Packaging

Table 51 Package characteristics

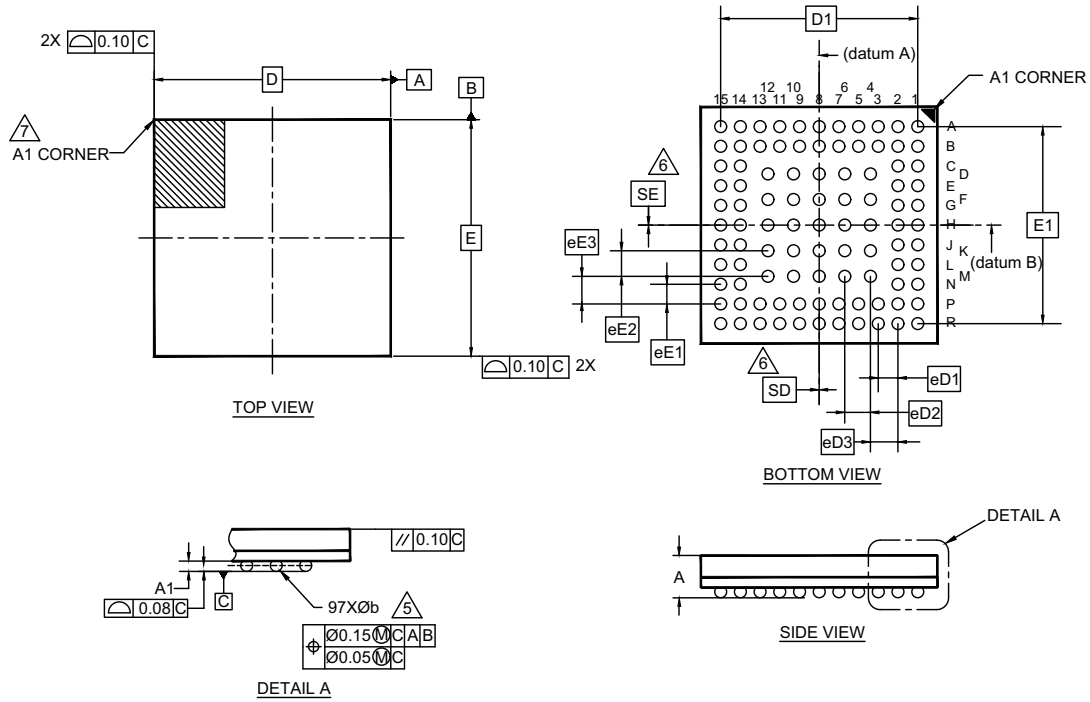
Parameter	Description	Conditions	Min	Typ	Max	Unit
T_A	Operating ambient temperature	Industrial	-40	25	85	°C
T_J	Operating junction temperature				125	
T_{JA}	Package θ_{JA} (97-ball BGA)	–	–	42	–	°C/W
T_{JC}	Package θ_{JC} (97-ball BGA)		–	15.9	–	
T_{JA}	Package θ_{JA} (48-pin QFN)		–	16.6	–	
T_{JC}	Package θ_{JC} (48-pin QFN)		–	6.5	–	

Table 52 Solder reflow peak temperature

Package	Maximum peak temperature	Maximum time within 5°C of peak temperature
97-ball BGA	260°C	30 s
48-pin QFN		

Table 53 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2

Package	MSL
97-ball BGA	MSL 3
48-pin QFN	



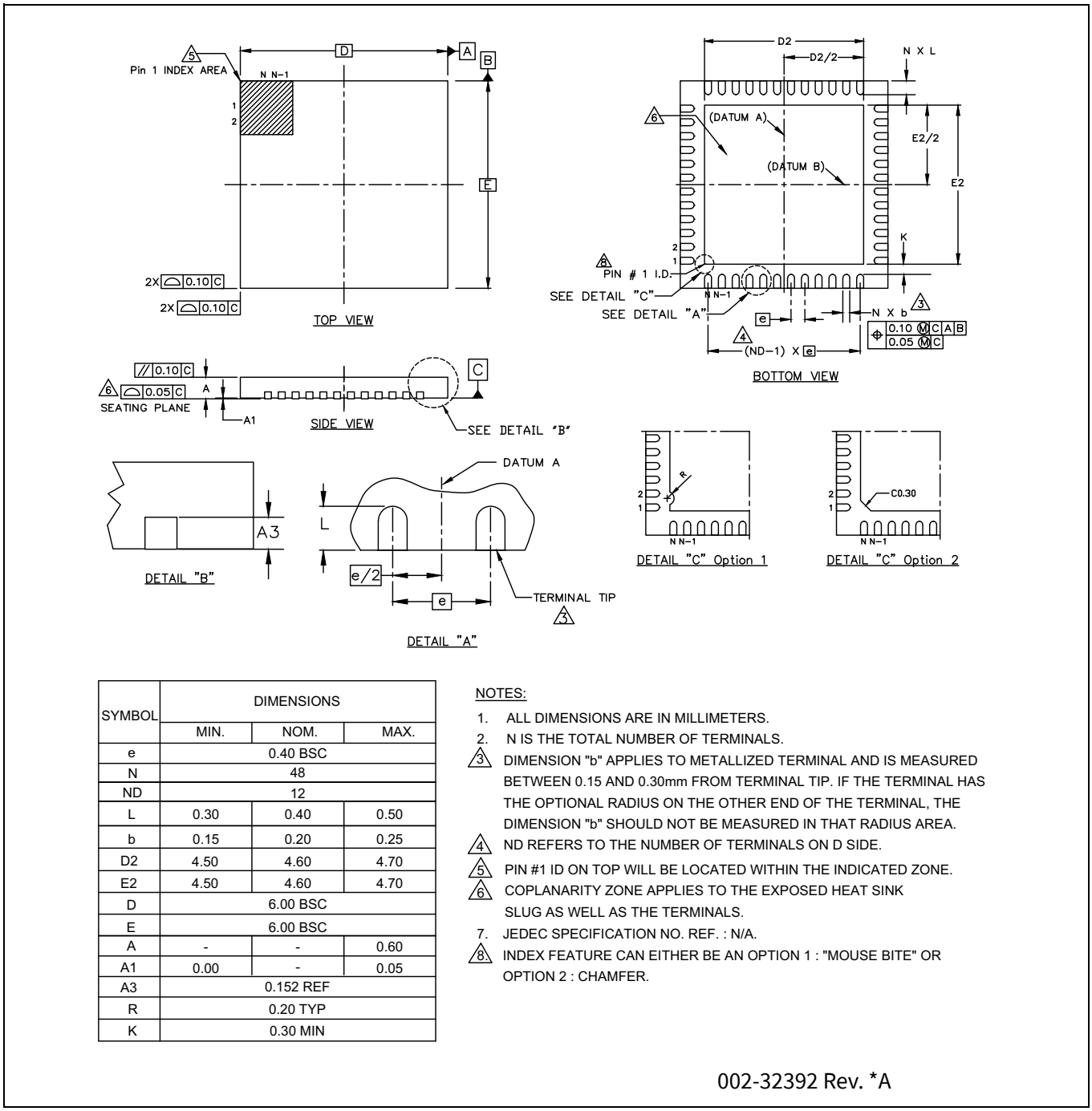
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.16	-	-
D	6.00 BSC		
E	6.00 BSC		
D1	5.00 BSC		
E1	5.00 BSC		
MD	11		
ME	11		
N	97		
Ø b	0.25	0.30	0.35
eD1	0.50 BSC		
eE1	0.50 BSC		
eD2	0.65 BSC		
eE2	0.65 BSC		
eD3	0.70 BSC		
eE3	0.70 BSC		
SD	0.00		
SE	0.00		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF. : MO-225.

002-31241 Rev. *A

Figure 13 97-ball VFBGA ((6.0 × 6.0 × 1.0 mm) BZ97A) package outline (PG-VFBGA-97), 002-31241



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e		0.40 BSC	
N		48	
ND		12	
L	0.30	0.40	0.50
b	0.15	0.20	0.25
D2	4.50	4.60	4.70
E2	4.50	4.60	4.70
D		6.00 BSC	
E		6.00 BSC	
A	-	-	0.60
A1	0.00	-	0.05
A3		0.152 REF	
R		0.20 TYP	
K		0.30 MIN	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE TOTAL NUMBER OF TERMINALS.
3. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
4. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE.
5. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
6. COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
7. JEDEC SPECIFICATION NO. REF. : N/A.
8. INDEX FEATURE CAN EITHER BE AN OPTION 1 : "MOUSE BITE" OR OPTION 2 : CHAMFER.

002-32392 Rev. *A

Figure 14 48-lead QFN ((6.0 × 6.0 × 0.6 mm) LD48B 4.6 × 4.6 mm E-Pad (Sawn)) package outline (PG-VQFN-48), 002-32392

9 Acronyms

Table 54 Acronyms used in this document

Acronym	Description
AC	Apple charging
ADC	analog-to-digital converter
AES	advanced encryption standard
AFC	adaptive fast charging
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus
API	application programming interface
Arm®	advanced RISC machine, a CPU architecture
BC	battery charging
BMC	Biphase Mark Code
CC	configuration channel
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CS	current sense
DFP	downstream facing port
DIO	digital input/output, GPIO with only digital capabil- ities, no analog. See GPIO.
DRP	dual role port
ECC	Elliptic Curve Cryptography
EEPROM	electrically erasable programmable read-only memory
EMCA	electronically marked cable assembly, a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports
EMI	electromagnetic interference
ESD	electrostatic discharge
FS	full-speed
GPIO	general-purpose input/output
HPD	hot plug detect
IC	integrated circuit
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
IOSS	input/output subsystem
I/O	input/output, see also GPIO
LDO	low-dropout regulator
LVD	low-voltage detect
LVTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit
MMIO	memory mapped input/output

Table 54 Acronyms used in this document *(continued)*

Acronym	Description
NC	no connect
NMI	nonmaskable interrupt
NVIC	nested vectored interrupt controller
opamp	operational amplifier
OCP	overcurrent protection
OVP	overvoltage protection
PASS	programmable analog sub-system
PCB	printed circuit board
PD	power delivery
PGA	programmable gain amplifier
PHY	physical layer
POR	power-on reset
PRES	precise power-on reset
PWM	pulse-width modulator RAM
QC	quick charge
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RSA	Rivest Shamir Adleman
RTC	real-time clock
RX	receive
SAR	successive approximation register
SBU	sideband use
SCB	serial communication block
SCL	I2C serial clock
SDA	I2C serial data
S/H	sample and hold
SHA	secure hash algorithm
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TCPWM	timer/counter pulse-width modulator
Thunderbolt	Trademark of Intel
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
USB	Universal Serial Bus
USB-FS	USB Full-Speed
USBIO	USB input/output, PMG1-S3 pins used to connect to a USB port

Table 54 Acronyms used in this document *(continued)*

Acronym	Description
USB PD	USB Power Delivery
USBPD SS	USB PD subsystem
VDM	vendor defined messages
XRES	external reset I/O pin

10 Document conventions

10.1 Units of measure

Table 55 Units of measure

Symbol	Unit of measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

Revision history

Document revision	Date	Description of changes
*E	2021-11-27	Publish to Web.
*F	2022-02-01	Updated **Features**: Updated description. Updated **Functional overview**: Updated **USB-PD sub-system**: Updated **USB-PD physical layer**: Updated description. Updated **Electrical specifications**: Updated **Analog peripherals**: Updated **SAR ADC**: Updated **Table 15**. Updated **Packaging**: Removed spec 002-32392 *A. Added spec 001-57280 *E. Updated to new template.
*G	2022-03-16	Updated **Pinouts**: Updated **Table 2**. Updated **Electrical specifications**: Updated **Absolute maximum ratings**: Added **Table 4** (for pin based absolute maximum ratings). Updated **Ordering information**: Updated **Table 50** (Updated part numbers, added “Type-C ports”, “Dead battery terminations”, “DTermination resistors” columns).
*H	2022-12-22	Updated **EZ-PD™ PMG1 family general description**: Updated **Table 1**. Updated **Block diagram**. Updated **Functional overview**: Updated **USB-PD sub-system**: Updated **Load switch controller**: Updated description. Updated **Application diagrams**: Updated description. Updated **Figure 8**. Added **Figure 9**. Added **Figure 10**. Updated **Figure 11**. Added **Figure 12**. Updated **Ordering information**: Updated **Table 50** (Updated part numbers).
*I	2024-02-13	Replaced “OVT” with “Fail-Safe” in all instances across the document. Updated **EZ-PD™ PMG1 family general description**: Updated **Figure 1**. Updated **Table 1**. Updated **Features**: Updated description. Updated **Block diagram**.

Document revision	Date	Description of changes
*I (cont.)	2024-02-13	Updated **Functional overview**: Updated **System resources**: Updated **Clock system**: Updated description. Updated **Analog blocks**: Updated **12-bit SAR ADC**: Updated description. Updated **Continuous time block mini (CTBm)**: Updated description. Updated **USB-PD sub-system**: Updated **8-bit SAR ADC**: Replaced “ADC” with “8-bit SAR ADC” in heading. Updated description. Updated **SBU mux**: Updated description. Updated **Figure 4**. Updated **Load switch controller**: Updated description. Updated **USB2.0 full speed device and charger detection**: Updated description. Updated **Fixed-function digital**: Updated **SCB**: Updated description. Updated **GPIO interface**: Added **Fail-Safe GPIOs**. Updated **Pinouts**: Updated **Table 2**. Updated **Figure 7**. Updated **Electrical specifications**: Updated **Absolute maximum ratings**: Updated **Table 3**. Updated **Device level specifications**: Updated **Table 5**. Updated **GPIO**: Updated **Table 7**. Updated **Table 8**. Updated **XRES**: Updated **Table 9**. Updated **Analog peripherals**: Updated **SAR ADC**: Updated **Table 16**. Updated **CSD**: Updated **Table 17**. Updated **Digital peripherals**: Updated **I2C**: Updated **Table 20**. Updated **Memory**: Updated **Table 27**. Updated **System resources**: Updated **SWD**: Updated **Table 31**. Updated **Ordering information**: Updated **Table 50** (Removed “Opamps inputs/outputs” column, updated details under “TCPWM” column). Updated to new template.

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2024-02-13
Published by
Infineon Technologies AG
81726 Munich, Germany

Do you have a question about this document?
Email:
erratum@infineon.com

Document reference
002-31288 Rev. *I

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.