300V Current Sensing Single Channel MOSFET/IGBT Driver

Description

UMW IR21271STR is a high voltage, high speed power MOSFET and IGBT driver. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL outputs,down to 3.3V. The protection circuity detects over-current in the driven power transistor and terminates the gate drive voltage. An open drain FAULT signal is provided to indicate that an over-current shutdown has occurred. The output driver features a high pulse current buffer stage designed for minimum cross-conduction.The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side or low side configuration which operates up to 300 volts.

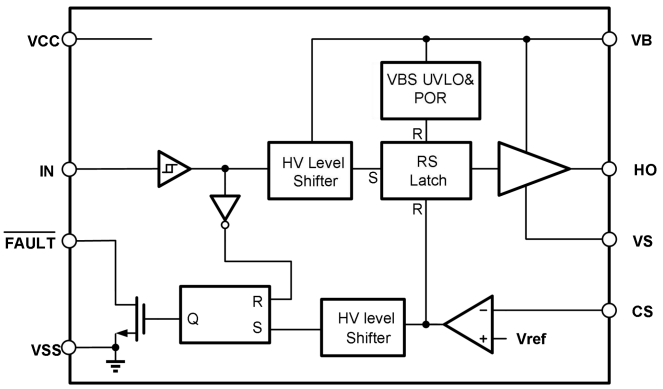
Application

- Motor control and drive
- Robot technology
- Fast charging of electric vehicles

Features and Benefits

- Floating channel designed for bootstrap operation
- Fully operational to +300 V
- 3.3V, 5V and 15V input logic compatible
- dV/dt noise Immunity ±50 V/nsec
- Allowable negative Vs capability: -5V
- Output in phase with input
- Gate drive supply range from 8V to 22V
- Undervoltage lockout for both channels --UVLO 6.8V/7.2V
- Propagation delay --Ton/Toff =150ns/150ns
- Wide operating temperature range -40°C ~125°C
- Fault lead indicates shutdown has occurred
- RoSH compatible SOIC8(S)

Functional Block Diagram



Function Pin Description

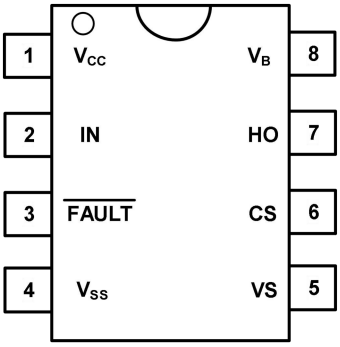


Figure7-1 8-Pin SOIC8 Top view

Table7-1 Lead Definitions

Number	Symbol	Description
1	V_{CC}	Power supply
2	IN	Logic input for high side gate driver output (HO), in phase
3	$\overline{FAULT}$	Indicates over-current shutdown has occurred,negative logic
4	V_{SS}	Logic ground
5	V_S	High side floating supply return
6	CS	Current sense input to current sense comparator
7	HO	High side gate drive output
8	V_B	High side floating supply

Absolute Maximum Ratings

Exceeding the limit maximum rating may cause permanent damage to the device. All voltage parameters are rated with reference to VSS and an ambient temperature of 25°C.

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	-0.3	322	V
V_S	High side floating supply return	V_B – 22	V_B + 0.3	
V_{HO}	High side gate drive output	V_S -0.3	V_B + 0.3	
V_{CC}	Low side and main power supply	-0.3	22	
V_{IN}	Logic input of IN	-0.3	V_{CC} + 0.3	
V_{FLT}	$\overline{FAULT}$ output voltage	-0.3	V_{CC} + 0.3	
V_{CS}	Current sense voltage	V_S - 0.3	V_B + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient	—	50	V/ns
ESD	HBM Model	2	—	kV
	Machine Model	500	—	V
P_D	Package Power Dissipation @ TA ≤25°C	—	0.625	W
Rth_{JA}	Thermal Resistance, Junction to Ambient	--	200	°C/W
T_J	Junction Temperature	—	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

For proper operation, the device should be used under the following recommended conditions. The bias ratings of VS and VSS are measured at a supply voltage of 15V, and unless otherwise specified, the ratings of all voltage parameters are referenced to VSS and the ambient temperature is 25°C.

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	VS + 8	VS + 20	V
V_S	High side floating supply return	-5	300	
V_{HO}	High side gate drive output	V_S	V_B	
V_{CC}	Low side and main power supply	8	20	
V_{IN}	Logic input of IN	0	V_{CC}	
V_{FLT}	$\overline{FAULT}$ output voltage	0	V_{CC}	
V_{CS}	Current sense signal voltage	V_S	Vs+5	
T_A	Ambient temperature	-40	125	°C

Note1：Transient negative VS can be used for VSS-50V with a pulse width of 50ns, guaranteed by design.

Electrical Characteristics

T_A= 25°C, V_{CC}=V_B= 15V, C_L=1nF, unless otherwise specified

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
t_{ON}	Turn-on propagation delay	—	150	250	ns	V_S=0V
t_{OFF}	Turn-off propagation delay	—	150	250	ns	V_S=300V
t_R	Turn-on rise time	—	80	130	ns	
t_F	Turn-off fall time	—	40	70	ns	
t_{BL}	Start-up blanking time	550	750	950	ns	
t_{CS}	CS shutdown propagation delay	—	65	360	ns	
t_{flt}	CS to $\overline{FAULT}$ pull-up propagation delay	—	270	510	ns	

Static electrical characteristics

Valid for temperature range at T_A= 25ºC, V_{CC}=V_B= 15V, C_L=1nF, unless otherwise specified.

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
V_{IH}	Logic “1”(IN) input voltage	2.5	—	—	V	VCC=10Vto 20V
V_{IL}	Logic “0” (IN) input voltage	—	—	0.8	V	
V_{CSTH+}	CS input positive going threshold	1.5	1.8	2.1	V	
V_{BSUV+}	VBS supply UVLO threshold	6.3	7.2	8.2	V	
V_{BSUV-}		6.0	6.8	7.7	V	
I_{LK}	High-side floating supply leakage current	—	—	50	μA	V_B=V_S=300V
I_{QBS}	Quiescent VB supply current	—	300	800	μA	V_{IN}=0V or 5V
I_{QCC}	Quiescent VCC supply current	—	60	120	μA	V_{IN}=0V or 5V
I_{CS+}	“High”CS bias current	—	—	5	μA	CS=3V
I_{CS-}	“High”CS bias current	—	—	5	μA	CS=0V
V_{OH}	High level output voltage, VBIAS - VO	—	—	0.2	V	I_O=2mA
V_{OL}	Low level output voltage, VO	—	—	0.1	V	
I_{IN+}	Logic “1” Input bias current	—	7	15	μA	V_{IN}=5V
I_{IN-}	Logic “0” Input bias current	—	0	5	μA	V_{IN}=0V
I_{O+}	Output high short circuit pulsed current	200	300	—	mA	V_O=0V PW≤10us
I_{O-}	Output low short circuit pulsed current	420	600	—	mA	V_O=15V PW≤10us
$R_{on,FLT}$	FAULT-low on resistance	—	125	—	Ω	

Function Description

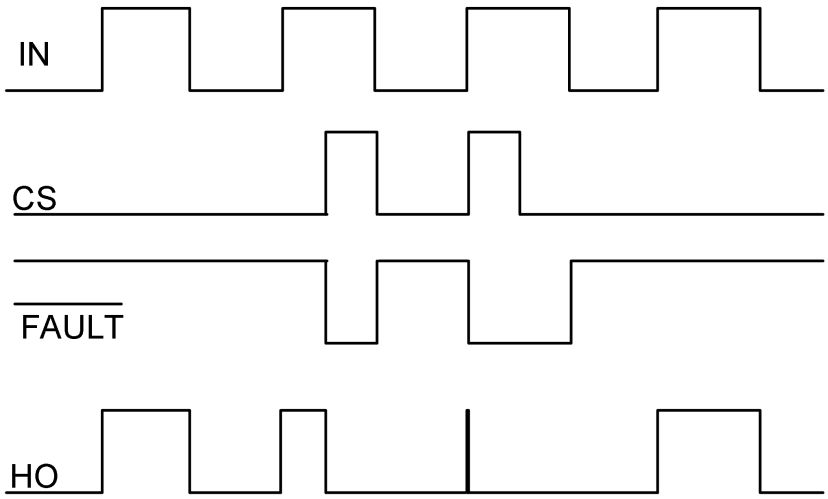


Figure 9-1 IR21271STR Input and output timing waveform

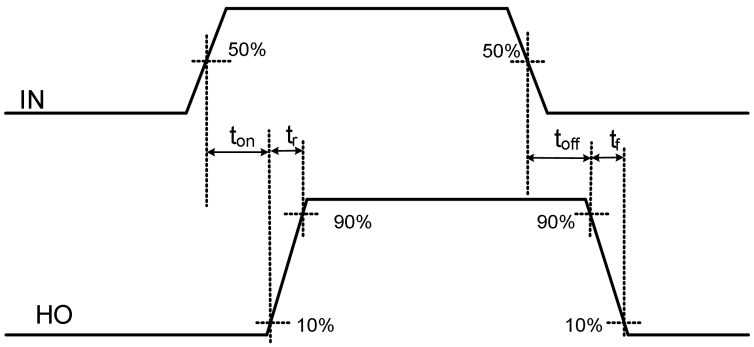


Figure 9-2 Switching Time Waveform Definition

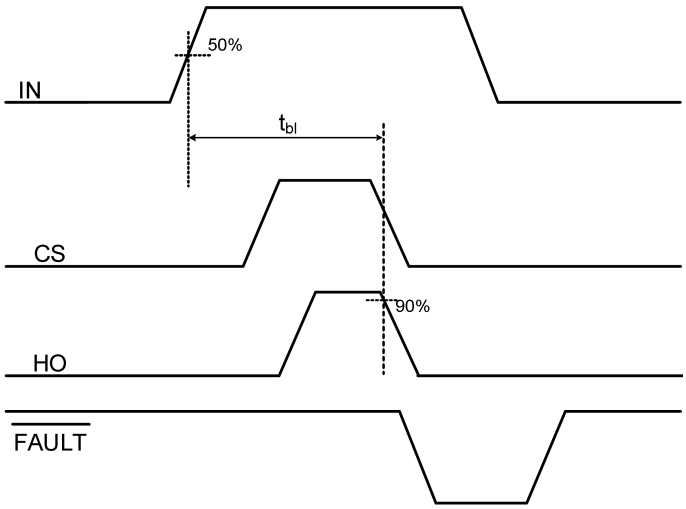


Figure 9-3 Start-up Blanking Time Waveform Definitions

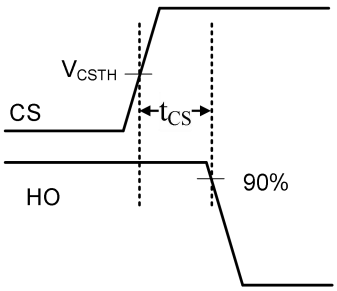


Figure 9-4 CS Shotdown Waveform Definitions

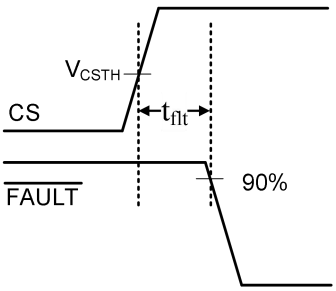


Figure 9-5 CS to FAULT Waveform Definitions

Function Block Diagram

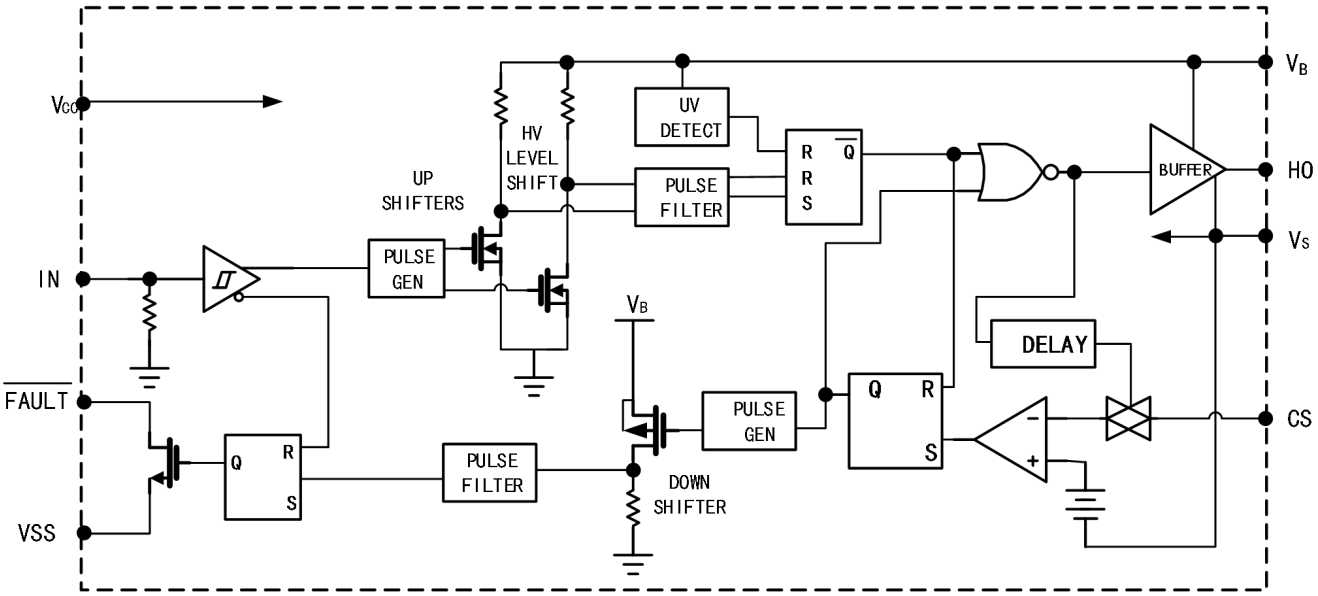


Figure10-1 Function Block Diagram of IR21271STR

Application message

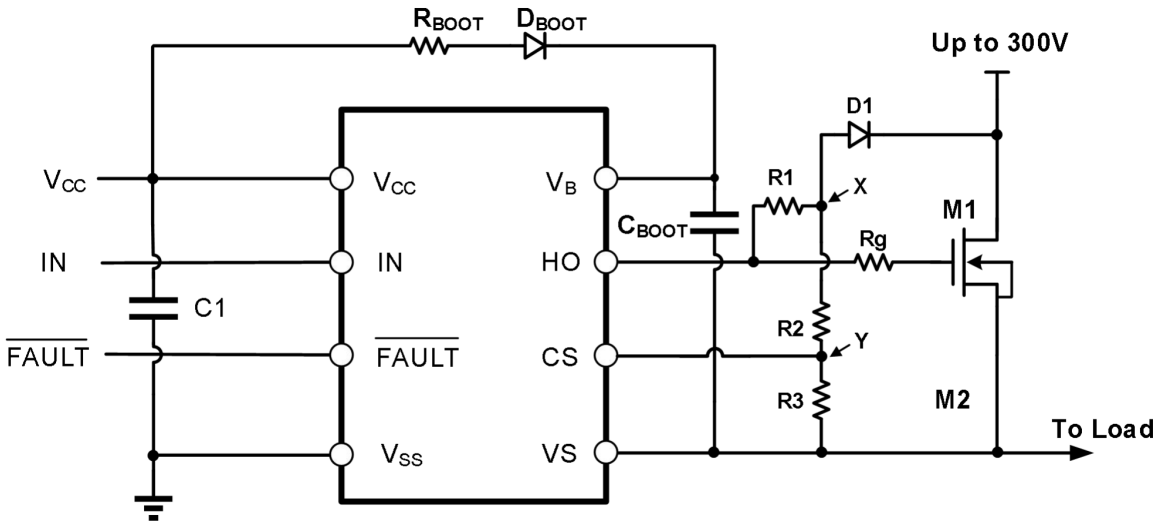


Figure10-2 Typical application circuit of IR21271STR

To Calculate the resistor values use the following guidelines.

Rg is the gate resistor, and the value is chosen to optimize switching speed and switching losses.

R1 is typically chosen to be 10k (12V Vbs)/22k (15V Vbs)/33k (18V Vbs); this high value helps to minimize the increased miller capacitance effect from diode D1, and makes sure there is not significant current being drawn from the HO output. Note diode D1 must have the same characteristics as the bootstrap diode.

When the HO output goes high MOSFET (or it could be an IGBT) Q1 turns on. Now point X in fig 10-2) will be pulled down to a voltage which equals the voltage across the FET (V_{DS}) plus the voltage across diode D1.

Therefore in an overload condition we want to shut down the driver output when the voltage across the FET (or IGBT) Q1 equals a set limit that indicates on overload condition has occurred (for example 8V).

Therefore with a 8V Vds on Q1. V_{D1} is typically 1.2V for a small 1A ultra fast recovery diode.

$$V_X=V_{D1}+V_{DS}$$

$$V_X=1.2+8$$

$$V_X=9.2V$$

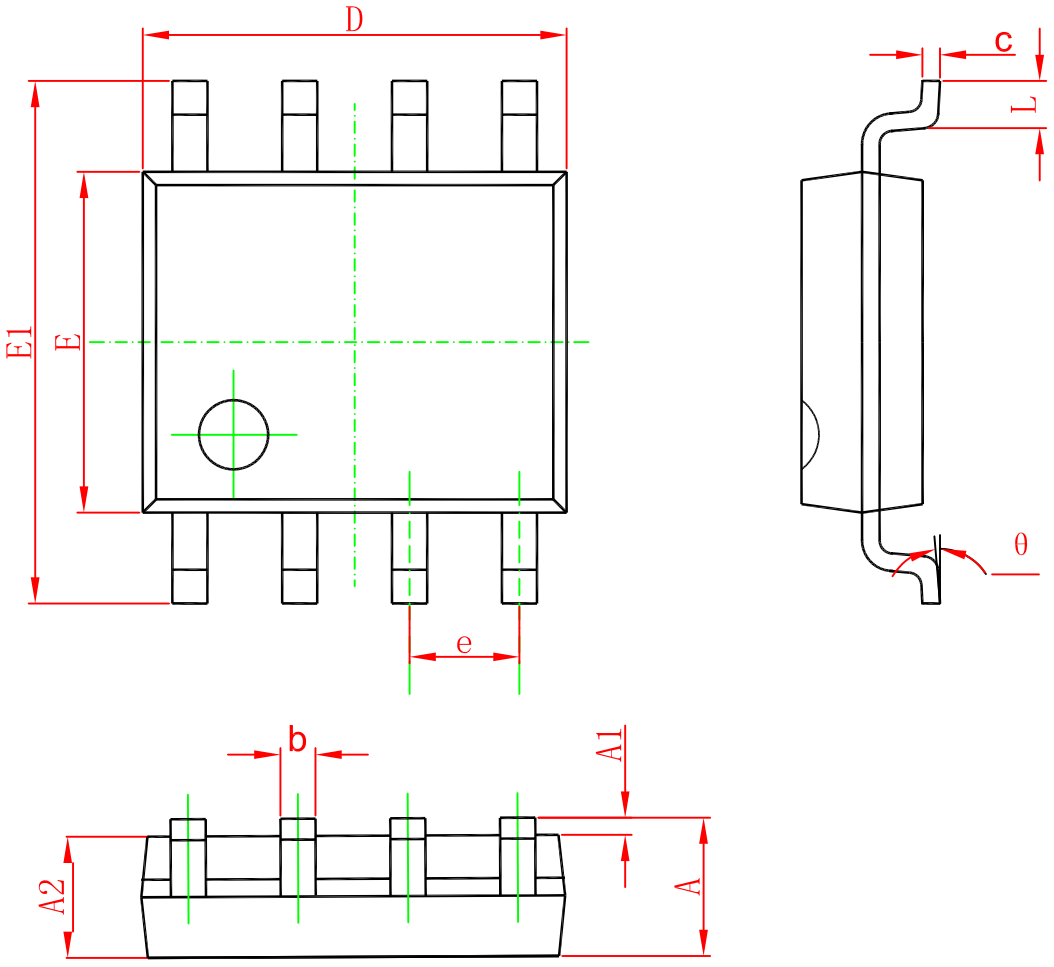
For a IR21271STR the CS pin threshold is 1.8V,therefore we need to divide V_X,so that when V_X=11.2V,then V_Y=1.8V.

$$V_Y=V_X \cdot R3/(R2+R3) \qquad \text{let } R2=33k$$

$$R3=6.319K$$

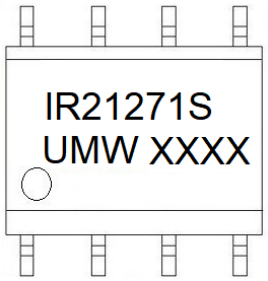
PACKAGING INFORMATION

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
UMW IR21271STR	SOP-8	2500	Tape and reel