Description

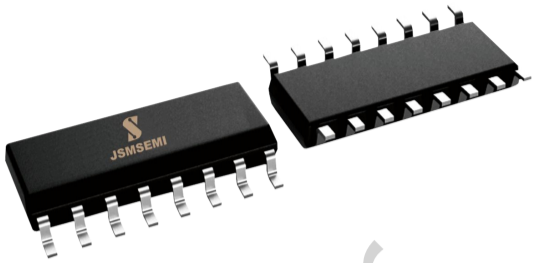
The ULN2003, ULN2004,are high voltage,high current Darlingtonarrays each containing even open collector Darlington pairs with common emitters.

Each channel ratedat 500mA and can with stand peak currents of 600mA.Suppression diodes are include for inductive load driving and the inputs are pinned opposite the outputs to simplify board layout.

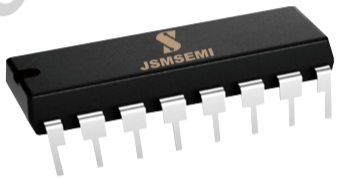
The versions interface to all commonlogic families:

--ULN2003(5VTTL,CMOS)

--ULN2004(6-15VCMOS,PMOS)



SOP-16

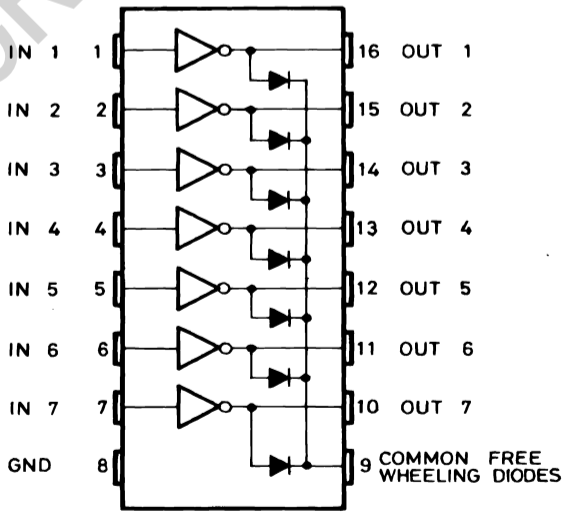


DIP-16

Features

- Seven Darlingtons per package
- Output current 500 mA per driver (600 mA peak)
- Output voltage 50 V
- Integrated suppression diodes for inductive loads
- Outputs can be paralleled for higher current
- TTL/CMOS/PMOS/DTL compatible inputs
- Inputs pinned opposite outputs to simplify

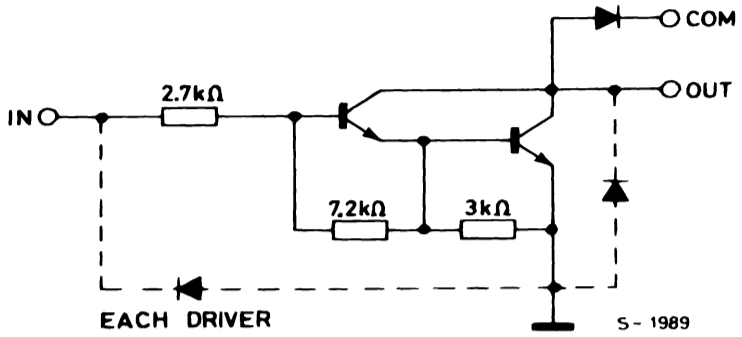
Pinconfiguration



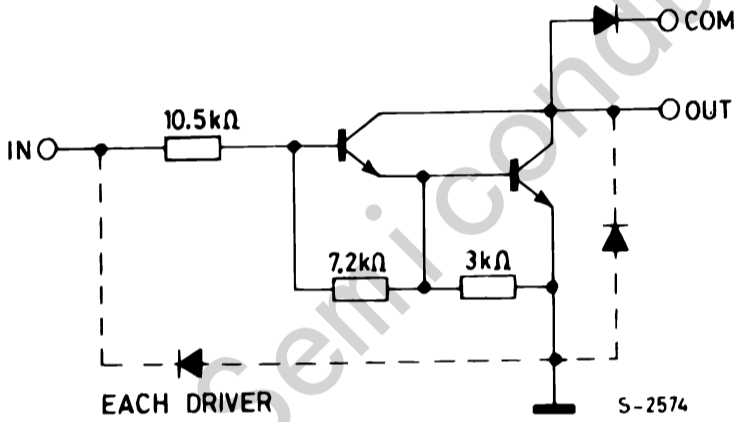
(top view)

Diagram

Schematic diagram



ULN2003 (each



ULN2004 (each driver)

Maximum ratings

Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_O	Output voltage	50	V
V_I	Input voltage (for ULN2003A/D - 2004A/D)	30	V
I_C	Continuous collector current	500	mA
I_B	Continuous base current	25	mA
T_A	Operating ambient temperature range	- 40 to 85	°C
T_{STG}	Storage temperature range	- 55 to 150	°C
T_J	Junction temperature	150	°C

Thermal data

Symbol	Parameter	DIP-16	SO-16	Unit
R_{thJA}	Thermal resistance junction-ambient, Max.	70	120	°C/W

Electricalcharacteristics

T_A = 25 °C unless otherwise specified.

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{CEX}	Output leakage current	V_{CE} = 50 V, (*Figure 1.*)			50	µA
		T_A = 85°C, V_{CE} = 50 V (*Figure 1.*)			100	
		T_A = 85°C for ULN2002, V_{CE} = 50 V, V_I = 6 V (*Figure 2.*)			500	
		T_A = 85°C for ULN2002, V_{CE} = 50 V, V_I = 1V (*Figure 2.*)			500	
$V_{CE(SAT)}$	Collector-emitter saturation voltage (*Figure 3.*)	I_C = 100 mA, I_B = 250 µA		0.9	1.1	V
		I_C = 200 mA, I_B= 350 µA		1.1	1.3	
		I_C = 350 mA, I_B= 500 µA		1.3	1.6	
$I_{I(ON)}$	Input current (*Figure 4.*)	for ULN2002, V_I = 17 V		0.82	1.25	mA
		for ULN2003, V_I = 3.85 V		0.93	1.35	
		for ULN2004, V_I = 5 V		0.35	0.5	
		V_I = 12 V		1	1.45	
$I_{I(OFF)}$	Input current (*Figure 5.*)	T_A = 85°C, I_C = 500 µA	50	65		µA
$V_{I(ON)}$	Input voltage (*Figure 6.*)	V_{CE}= 2 V, for ULN2002 I_C = 300 mA for ULN2003 I_C = 200 mA I_C = 250 mA I_C = 300 mA for ULN2004 I_C = 125 mA I_C = 200 mA I_C = 275 mA I_C = 350 mA			13 2. 42. 7 3 5 6 7 8	V
h_{FE}	DC Forward current gain (*Figure 3.*)	for ULN2001, V_{CE} = 2 V, I_C = 350 mA	1000			
C_I	Input capacitance			15	25	pF
t_{PLH}	Turn-on delay time	0.5 V_I to 0.5 V_O		0.25	1	µs
t_{PHL}	Turn-off delay time	0.5 V_I to 0.5 V_O		0.25	1	µs
I_R	Clamp diode leakage current (*Figure 7.*)	V_R = 50 V			50	µA
		T_A = 85°C, V_R = 50 V			100	
V_F	Clamp diode forward voltage (*Figure 8.*)	I_F = 350 mA		1.7	2	V

Test circuits

Figure 1. Output leakage currentFigure

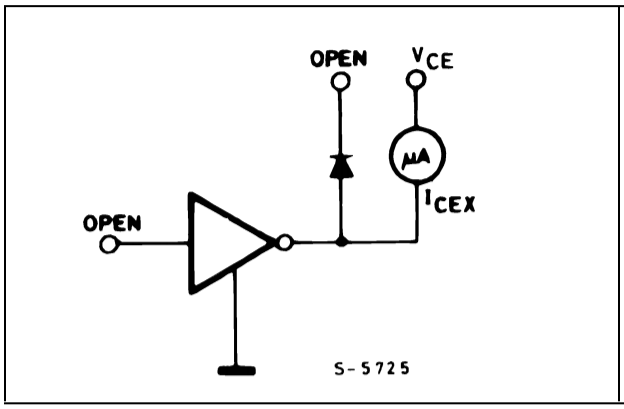


Figure 2. Output leakage current

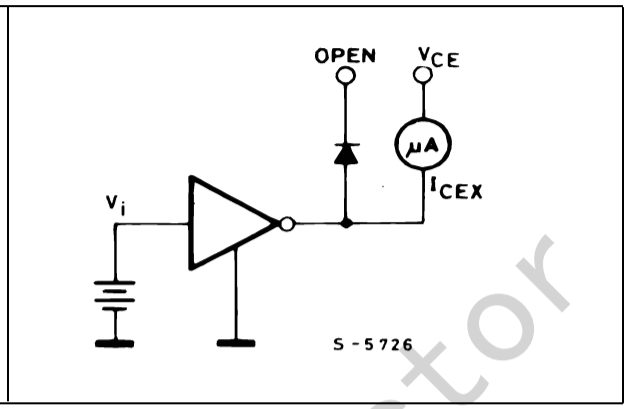


Figure 3.Collector-emitter saturation voltage

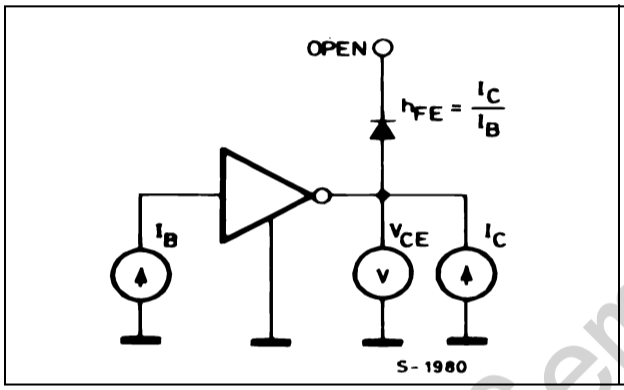


Figure 4.Input current (ON)

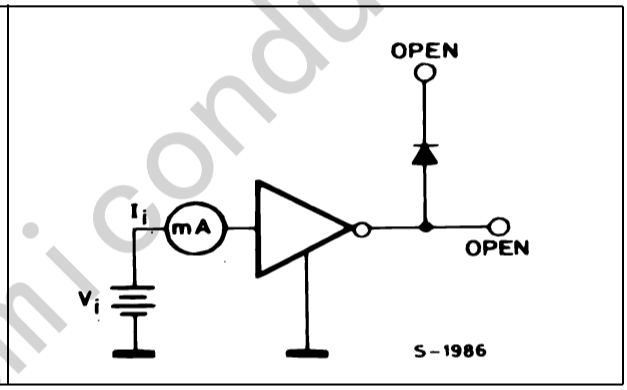


Figure 5.Input current (OFF)

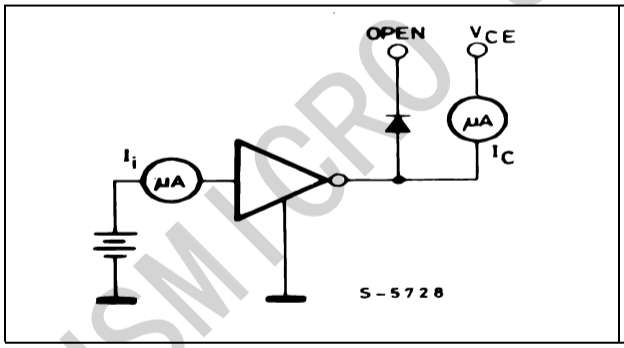


Figure 6.Input voltage

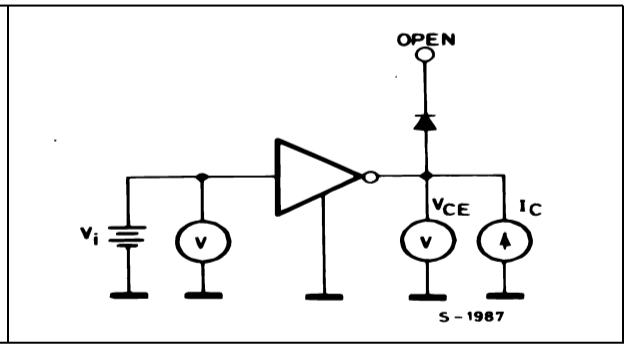


Figure 7.Clamp diode leakage current

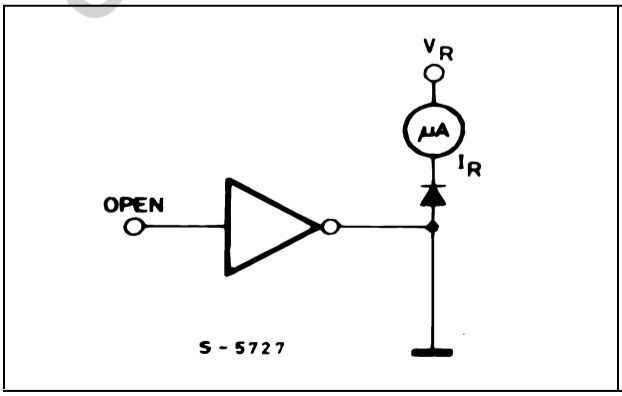
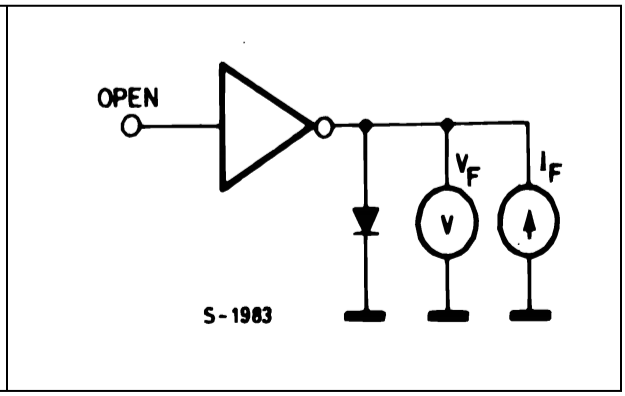


Figure 8.Clamp diode forward voltage



Typical performance characteristics

Figure 9.Collector current vs. saturation voltage (T_J = 25°C)

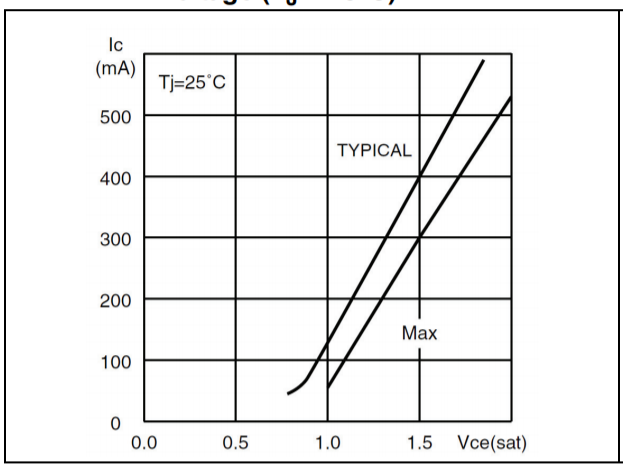


Figure 10.Collector current vs. saturation voltage

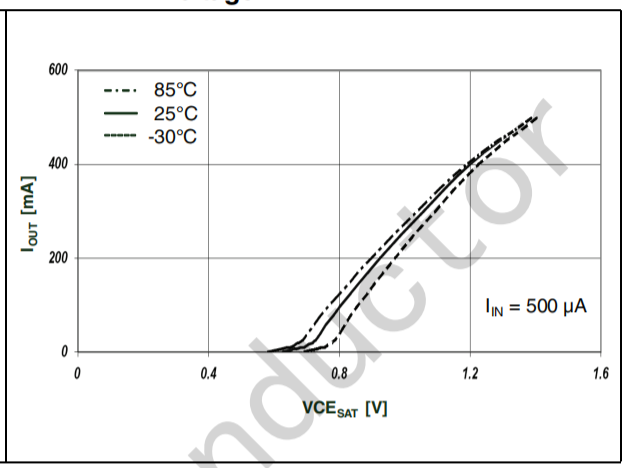


Figure 11.Input current vs. input voltage

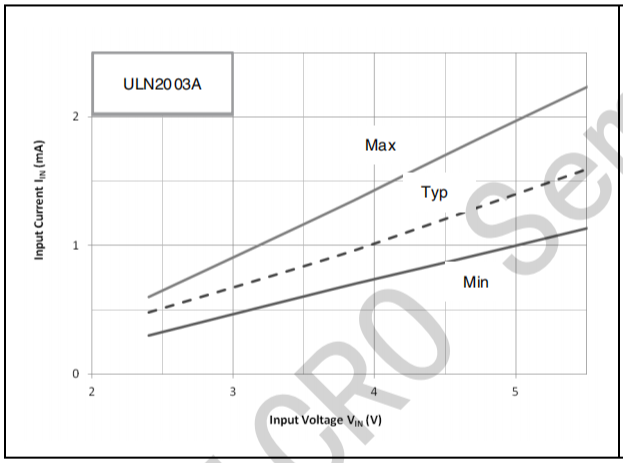


Figure 12.Input current vs. input voltage (Ta = 25°C)

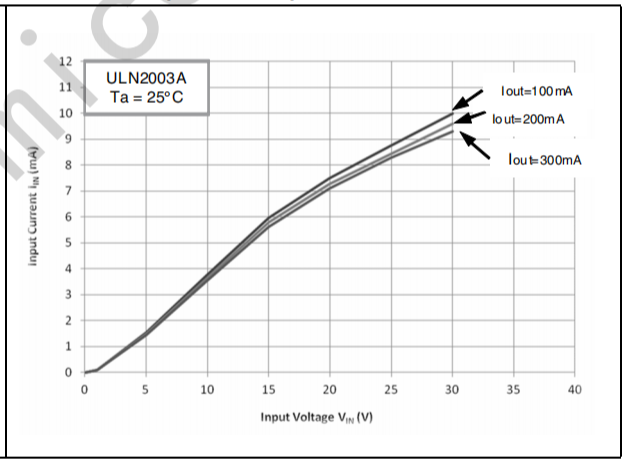


Figure 13.Collector current vs. input current

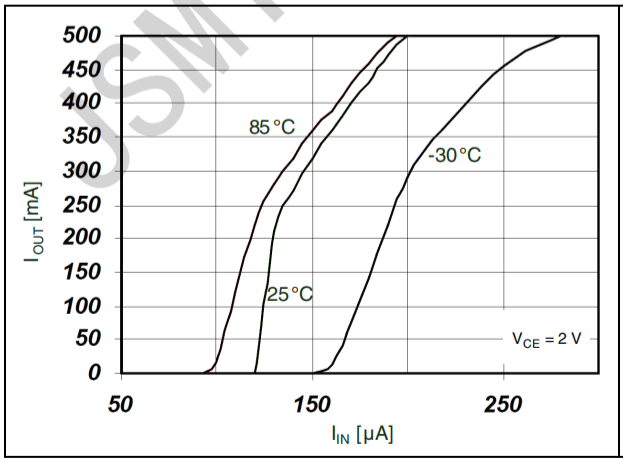


Figure 14.h_{FE} vs. output current

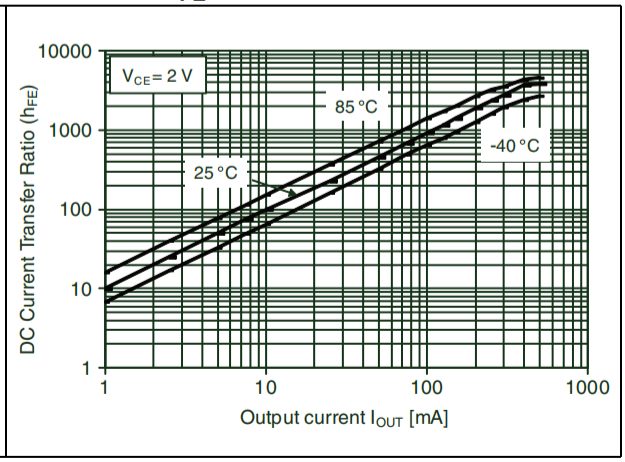


Figure 15.Peak collector current vs. duty cycle (DIP-16)

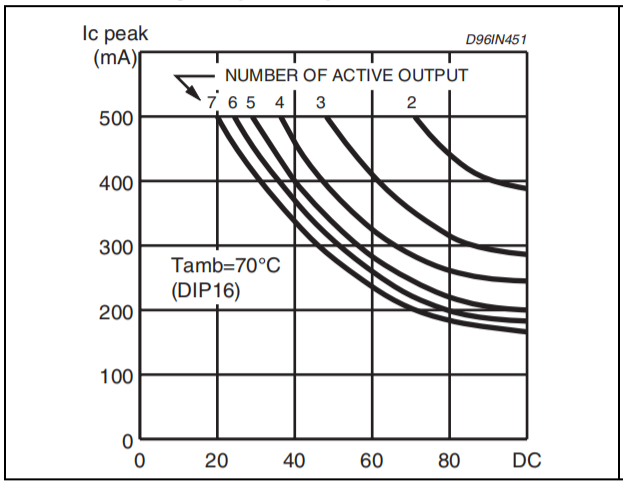


Figure 16.Peak collector current vs. duty cycle (SO-16)