NS4225 18Wx2 FILTER-FREE STEREO CLASS-D AUDIO POWER AMPLIFIER

1 Features

- Supply Voltage from 6V to 16V
- Output power at 12V or 16V supply:

10W×2 (VCC=12V,8Ω load,10% THD+N,BTL Output)

17W×2 (VCC=12V,4Ω load,10% THD+N,BTL Output)

18W×2 (VCC=16V,8Ω load,10% THD+N,BTL Output)

20W (VCC=12V,4Ω load,10% THD+N,PBTL Output)

36W (VCC=16V,4Ω load,10% THD+N,PBTL Output)

- Filterless Class-D operation
- Low shutdown current: 1μA (typical)
- Short-circuit & thermal protection
- Available TSSOP-24 Package

2 Applications

- Televisions
- Multimedia internet devices

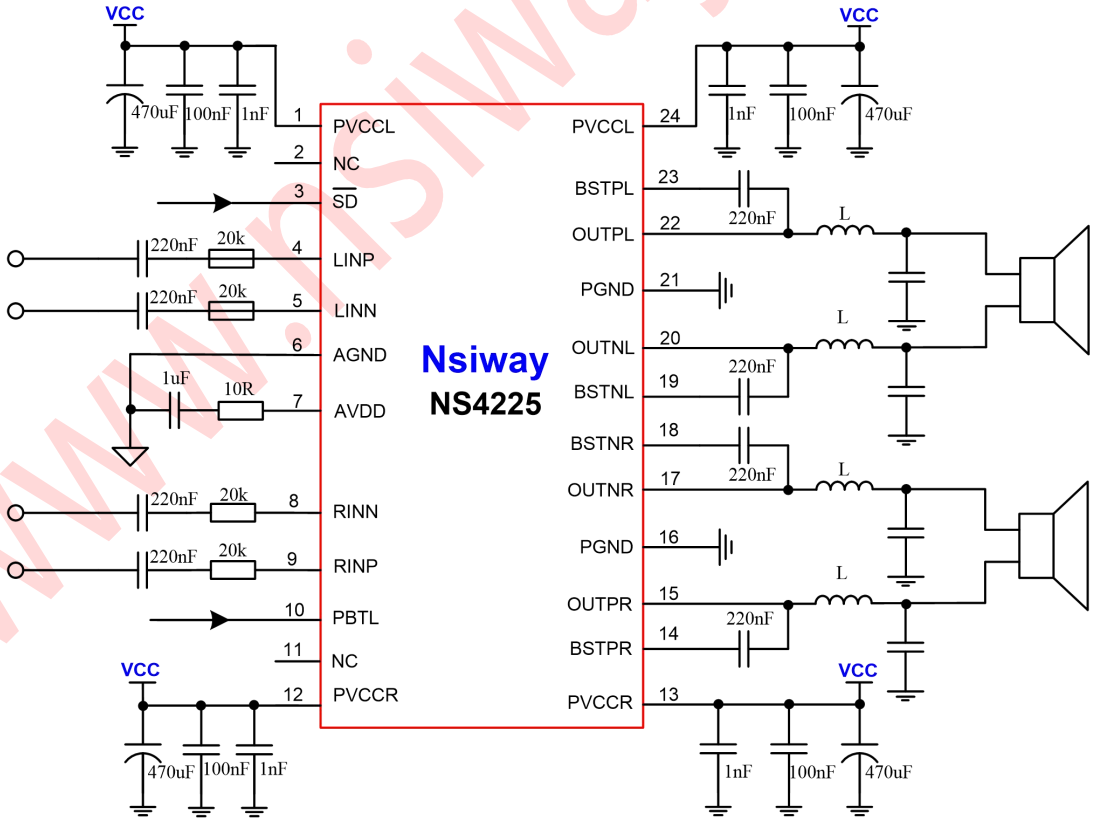
3 General Description

The NS4225 is a stereo, filterless, Class-D audio power amplifier. It operates from 6V to 16V supply. When powered with 16V supply voltage, the NS4225 is capable of delivering 18W (per channel) into 8Ω load, with THD+D less than 10%.

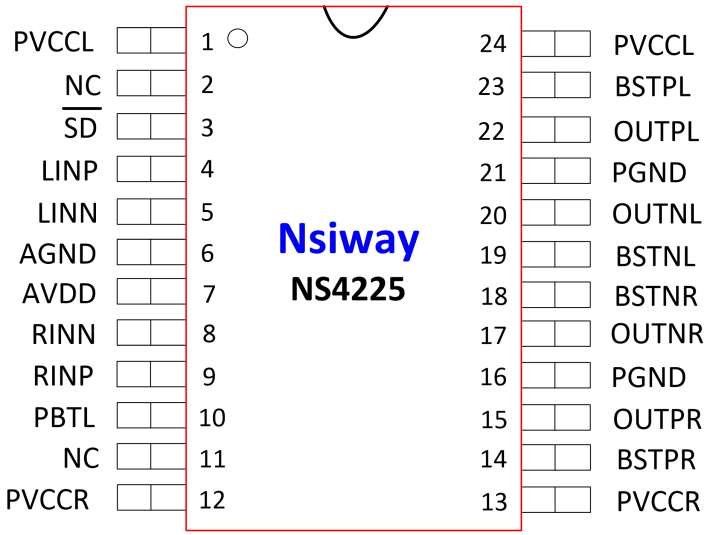
As a Class-D power amplifier, the NS4225 features high efficiency (up to 90%) and high PSRR (65dB at 217Hz), which make the device ideal for use in cellular handsets and other portable devices.

The NS4225 is available in TSSOP-24 package and is specified over the -40℃ to +85℃ temperature range.

4 Typical Application Circuit



5 Pins Configuration



NS: Corporation Code
4225: Partino 4225
YYWW: Date Code

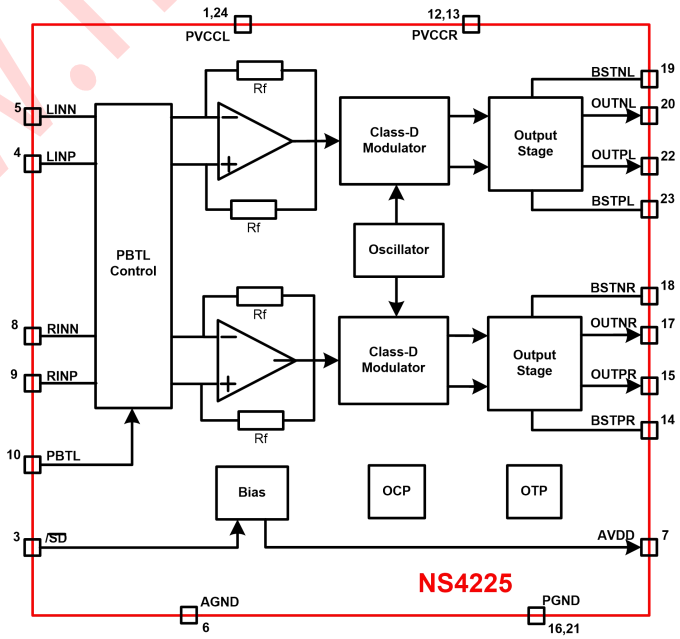
Pin NO.	Pin Name	Description
1,24	PVCCL	Power supply for left channel H-bridge. Right channel and left channel power supply inputs are connect internally.
2	NC	Not connected
3	$\overline{SD}$	Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled).
4	LINP	Positive audio input for left channel.
5	LINN	Negative audio input for left channel.
6	AGND	Analog signal ground. Connect to the thermal pad.
7	AVDD	5V LDO Output
8	RINN	Negative audio input for right channel
9	RINP	Positive audio input for right channel
10	PBTL	Parallel BTL mode switch
11	NC	Not connected
12,13	PVCCR	Power supply for right channel H-bridge. Right channel and left channel power supply inputs are connect internally
14	BSTPR	Bootstrap I/O for right channel, positive high-side FET.
15	OUTPR	Class-D H-bridge positive output for right channel.
16	PGND	Power ground for the H-bridges.
17	OUTNR	Class-D H-bridge negative output for right channel.
18	BSTNR	Bootstrap I/O for right channel, negative high-side FET.
19	BSTNL	Bootstrap I/O for left channel, negative high-side FET.
20	OUTNL	Class-D H-bridge negative output for left channel.
21	PGND	Power ground for the H-bridges.
22	OUTPL	Class-D H-bridge positive output for left channel.
23	BSTPL	Bootstrap I/O for left channel, positive high-side FET.

6 Absolute Maximum Ratings

Parameter	Min	Max	Unit	Note
Supply Voltage PVCC	6	17	V	
$\overline{SD}$	-0.3	5	V	
PBTL	-0.3	5	V	
LINP	-0.3	5	V	
LINN	-0.3	5	V	
RINP	-0.3	5	V	
RINN	-0.3	5	V	
Junction Temperature		125	℃	
Storage Temperature	-65	150	℃	
Lead Temperature (Soldering 10 Seconds0)		260	℃	
Package Thermal Resistance JA		90	℃/W	
Operating Ambient Temperature	-40	85	℃	
ESD Rating		2000	V	Human Body Model

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7 Block Diagram

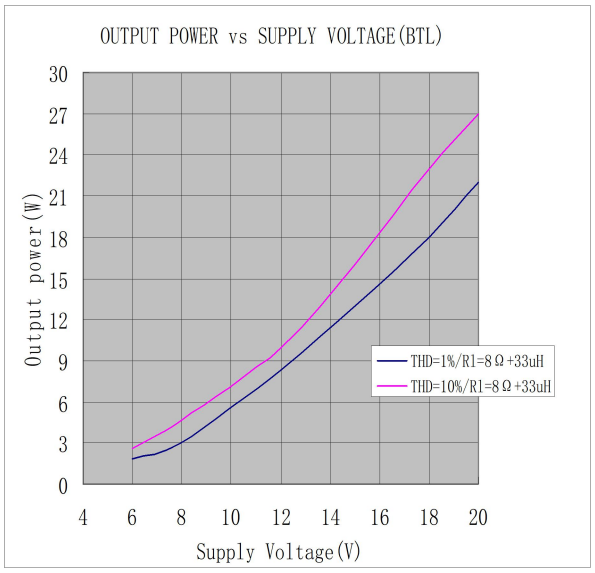


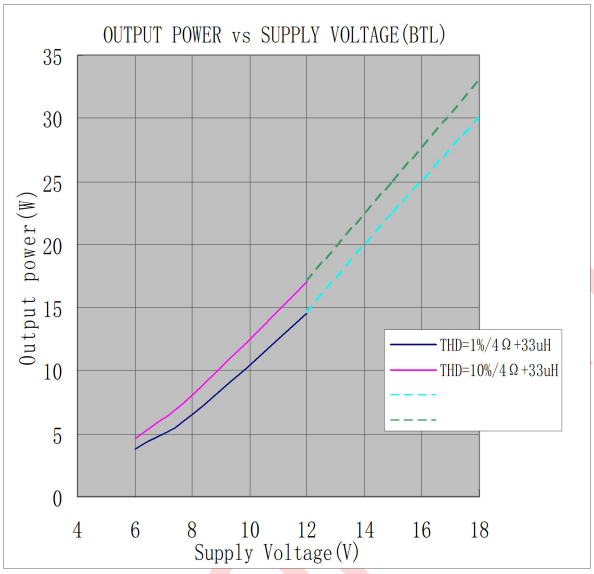
8 Electrical Characteristics

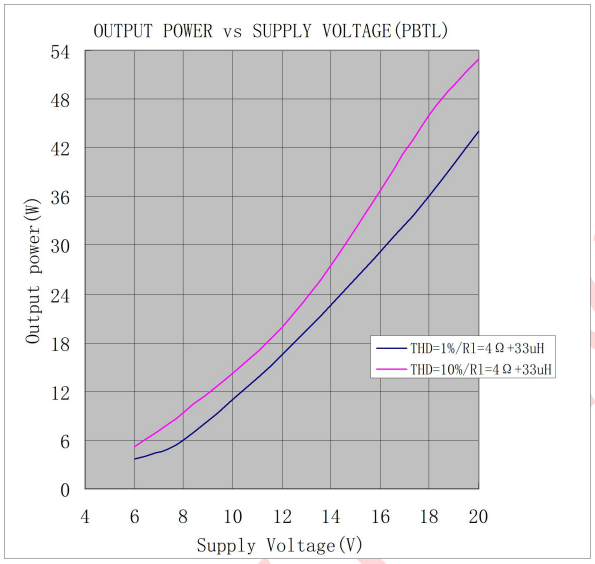
VCC=12V, TA=25°C, RL=8 Ω, unless otherwise specified.

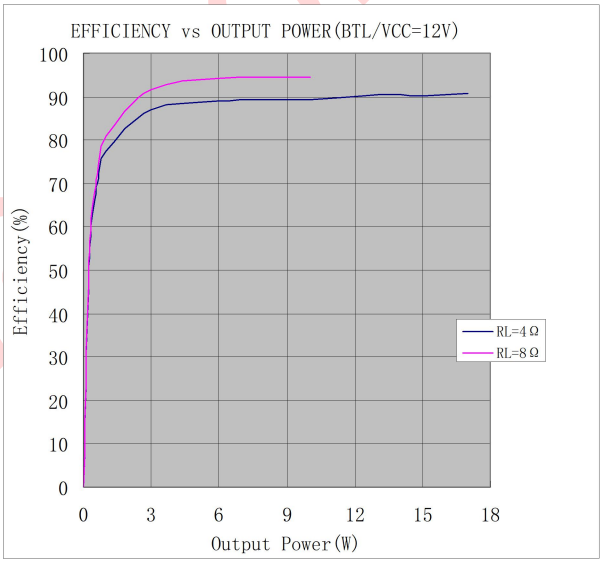
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Supply Voltage		6		16	V
I_{DD}	Quiescent Current	V_{IN}＝0V,No load		35		mA
I_{SD}	Shutdown Current	$V_{/SD}$ =0V		1		μA
V_{OS}	Output offset voltage	V_{IN}＝0V,Gain=20dB		20		mV
PSRR	Power-Supply Rejection Ratio	217Hz		-65		dB
		20KHz		-60		dB
CMRR	Common-Mode Rejection Ratio			-70		dB
f_{SW}	Carrier clock frequency			280		kHz
η	Efficiency	Po=8W×2,RL =8Ω		94		%
V_{IH}	High–level input voltage	Logic High	2.8			V
V_{IL}	Low–level input voltage	Logic Low			0.4	
P_O 输出功率	VCC=12V	THD＝1%,f=1KHz, R_L=4Ω,PBTL R_L=4Ω,BTL R_L=8Ω,BTL		 16 14 8		W
		THD＝10%,f=1KHz R_L=4Ω,PBTL R_L=4Ω,BTL R_L=8Ω,BTL		 20 17 10		W
	VCC=16V	THD＝1%,f=1KHz R_L=4Ω,PBTL R_L=8Ω,BTL		 28 15		W
		THD＝10%,f=1KHz R_L=4Ω,PBTL R_L=8Ω,BTL		 36 18		W
THD+N	Total Harmonic Distortion Plus Noise	Gain=20dB,f=1kHz R_L=8Ω,Po=4W		0.06		%
SNR	Signal-to-noise ratio	Gain=20dB,f=1kHz R_L=8Ω,Po=8W		90		dB
Vnoise	Output integrated noise	20Hz-20kHz,Gain=20dB		270		uV
CS	Over Temperature Hysteresis	Gain=20dB,f=1kHz R_L=8Ω,Po=8W		-90		dB
OTP	Over Temperature Protection			150		℃
OTH	Over Temperature Hysteresis			20		℃

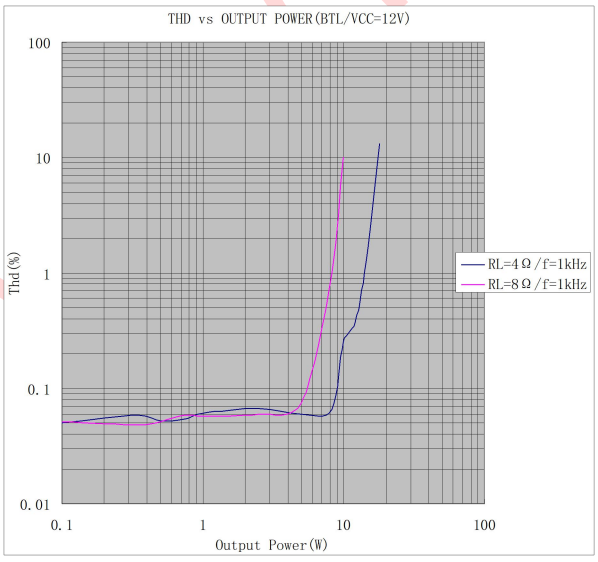
9 Typical Characteristics

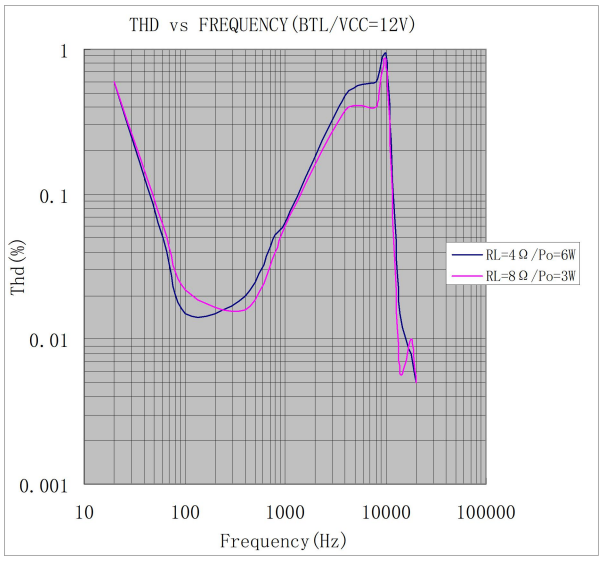












10 Application Specification

10.1 $\overline{SD}$ OPERATION

The NS4225 employs a shutdown mode of operation designed to reduce supply current (ICC) to the absolute minimum level during periods of nonuse for power conservation. The $\overline{SD}$ input terminal should be held high (see specification table for trip point) during normal operation when the amplifier is in use. Pulling $\overline{SD}$ low causes the outputs to mute and the amplifier to enter a low-current state. Never leave $\overline{SD}$ unconnected, because amplifier operation would be unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown mode prior to removing the power.

$\overline{SD}$ Pin Level	Operation Mode
High–level	Power ON
Low–level	SHUT DOWN
NC	SHUT DOWN

10.2 PBTL Select

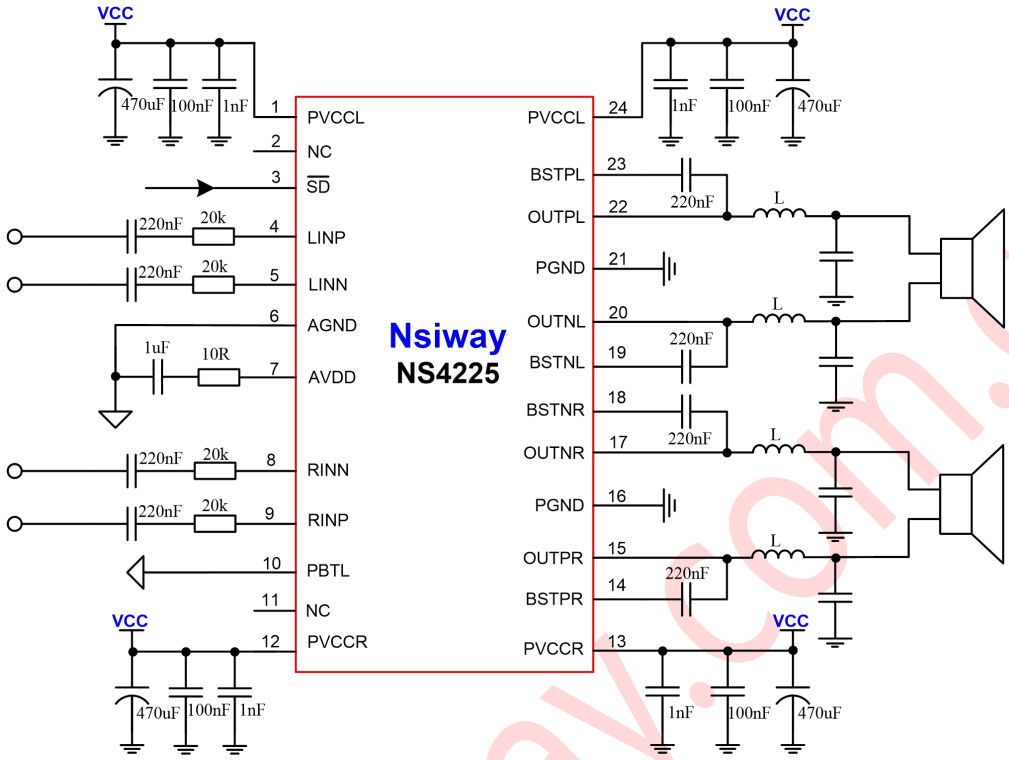
NS4225 offers the feature of parallel BTL operation with two outputs of each channel connected directly. If the PBTL pin (pin 10) is tied high, the positive and negative outputs of each channel (left and right) are synchronized and in phase. To operate in this PBTL (mono) mode, apply the input signal to the RIGHT input and place the speaker between the LEFT and RIGHT outputs. Connect the positive and negative output together for best efficiency. The voltage slew rate of the PBTL pin must be restricted to no more than 10V/ms. For higher slew rates, use a 100kΩ resistor in series with the terminals. For an example of the PBTL connection, see the schematic in the APPLICATION INFORMATION section.

For normal BTL operation, connect the PBTL pin to local ground.

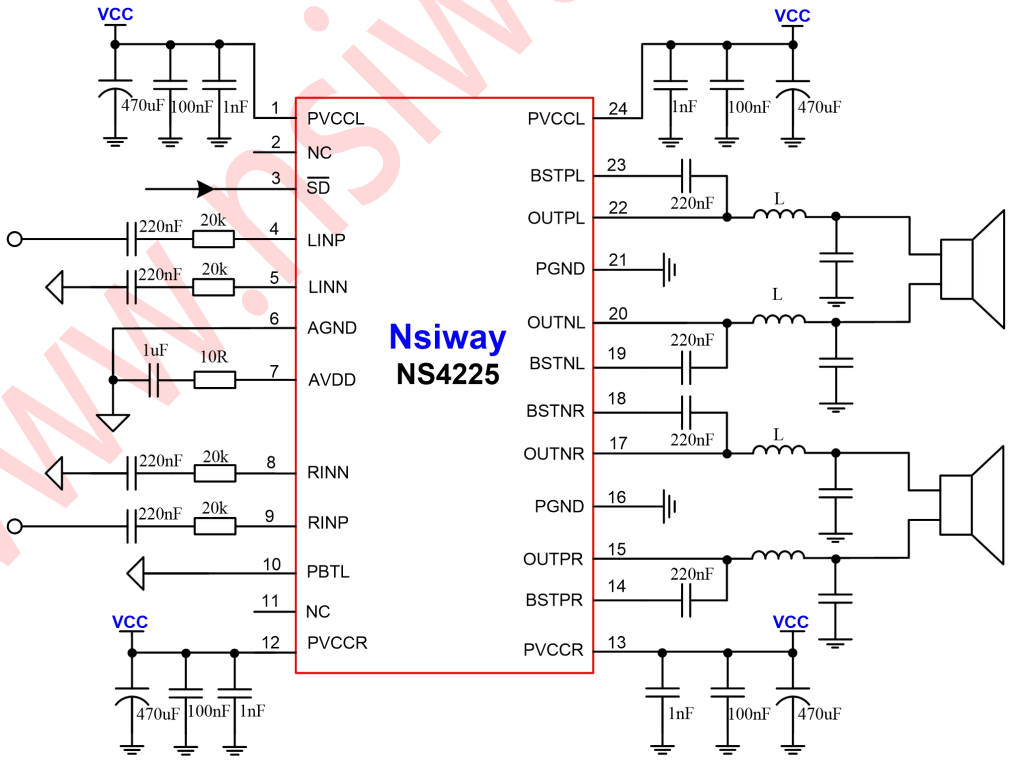
PBTL Pin	MODE
High–level	PBTL
Low–level	BTL
NC	BTL

11 APPLICATION INFORMATION

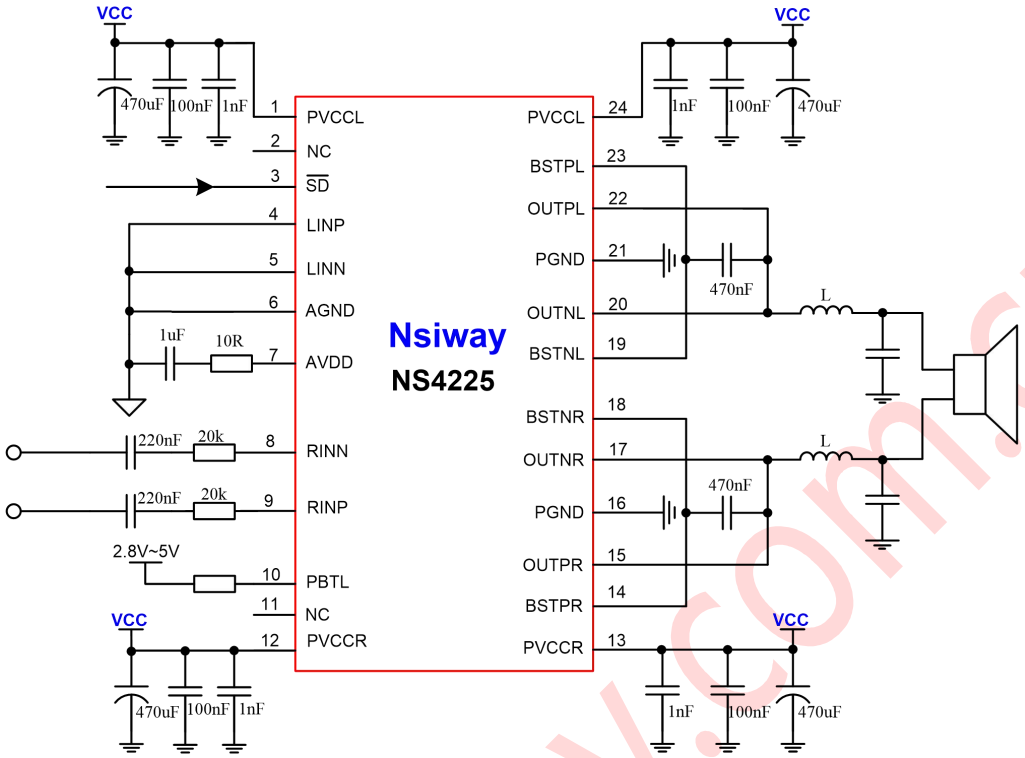
11.1 Stereo Class-D Amplifier with BTL Output and Differential-Ended Inputs



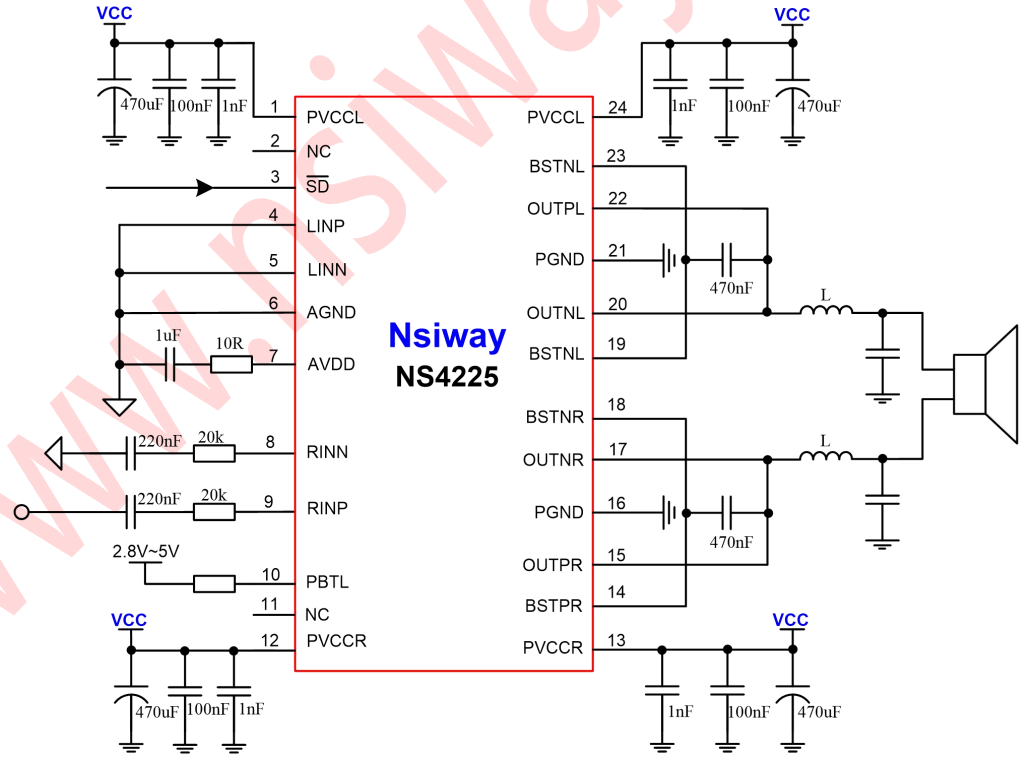
11.2 Stereo Class-D Amplifier with BTL Output and Single-Ended Inputs



11.3 Stereo Class-D Amplifier with PBTL Output and Differential-Ended Inputs



11.4 Stereo Class-D Amplifier with BTL Output and Single-Ended Inputs



11.5 INPUT RESISTANCE

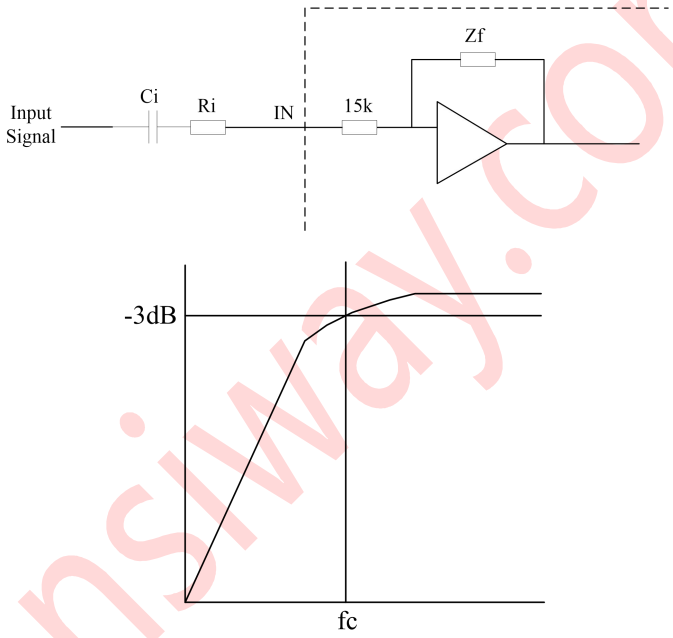
The input resistors (Ri) set the gain of the amplifier according to Equation :

$$A_{VD} = \frac{270K\Omega}{R_{IN}}$$

11.6 INPUT CAPACITOR, C_{IN}

Changing the gain setting can vary the input resistance of the amplifier from its smallest value. As a result, if a single capacitor is used in the input high-pass filter, the -3 dB or cutoff frequency may change when changing gain steps.

$$fc = \frac{1}{2\pi \cdot R_{IN} \cdot C_{IN}}$$



The value of CI is important, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where Ri is 20 kΩ and the specification calls for a flat bass response down to 36 Hz. In this example, CI is 0.22 µF; so, one would likely choose a value of 0.22 µF as this value is commonly used.

11.7 POWER SUPPLY DECOUPLING, Cs

The NS4225 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. Optimum decoupling is achieved by using a network of capacitors of different types that target specific types of noise on the power supply leads. For higher frequency transients due to parasitic circuit elements such as bond wire and copper trace inductances as well as lead frame capacitance, a good quality low equivalent-series-resistance (ESR) ceramic capacitor of value between 220 pF and 1000 pF works well. This capacitor should be placed as close to the device PVCC pins and system ground (either PGND pins or PowerPad) as possible. For mid-frequency noise due to filter resonances or PWM switching transients as well as digital hash on the line, another good quality capacitor typically 0.1 µF to 1 µF placed as close as possible to the device PVCC leads works best For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 470 µF or greater placed near the audio power amplifier is recommended. The

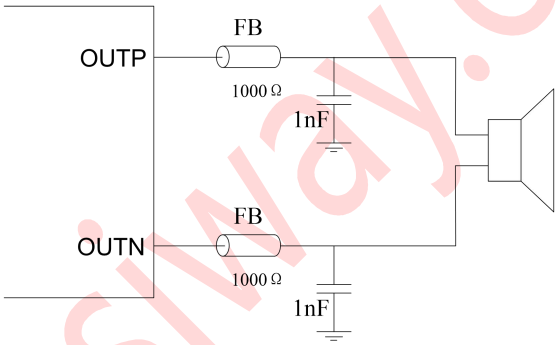
220 µF capacitor also serves as a local storage capacitor for supplying current during large signal transients on the amplifier outputs. The PVCC terminals provide the power to the output transistors, so a 470 µF or larger capacitor should be placed on each PVCC terminal. A 10 µF capacitor on the AVCC terminal is adequate. Also, a small decoupling resistor between AVCC and PVCC can be used to keep high frequency class D noise from entering the linear input amplifiers.

11.8 When to Use an Output Filter for EMI Suppression

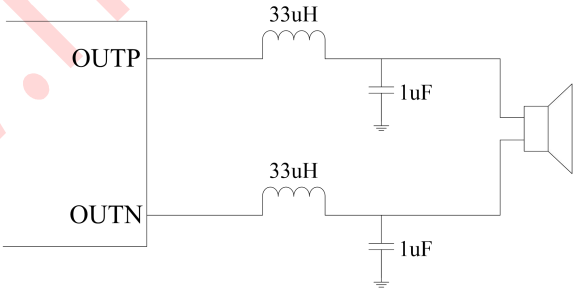
The NS4225 has been tested with a simple ferrite bead filter for a variety of applications including long speaker wires up to 125 cm and high power. The NS4225 EVM passes FCC Class B specifications under these conditions using twisted speaker wires. The size and type of ferrite bead can be selected to meet application requirements. Also, the filter capacitor can be increased if necessary with some impact on efficiency.

There may be a few circuit instances where it is necessary to add a complete LC reconstruction filter. These circumstances might occur if there are nearby circuits which are sensitive to noise. In these cases a classic second order Butterworth filter similar to those shown in the figures below can be used.

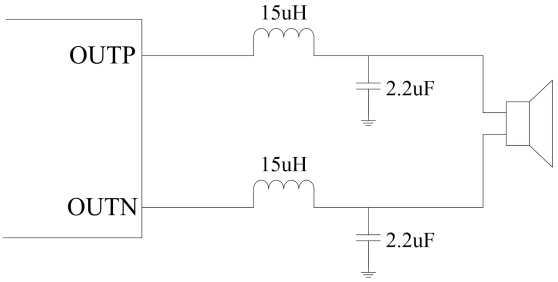
Some systems have little power supply decoupling from the AC line but are also subject to line conducted interference (LCI) regulations. These include systems powered by "wall warts" and "power bricks." In these cases, it LC reconstruction filters can be the lowest cost means to pass LCI tests. Common mode chokes using low frequency ferrite material can also be effective at preventing line conducted interference.



Typical Ferrite Chip Bead Filter (Chip Bead Example:)



Typical LC Output Filter, Cutoff Frequency of 27 kHz, Speaker Impedance = 8 Ω



Typical LC Output Filter, Cutoff Frequency of 27 kHz, Speaker Impedance = 4 Ω

11.9 PRINTED-CIRCUIT BOARD (PCB) LAYOUT

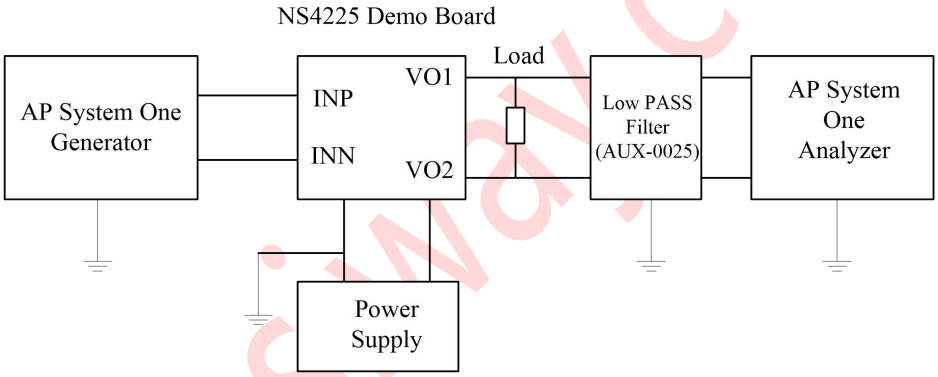
The NS4225 can be used with a small, inexpensive ferrite bead output filter for most applications. However, since the Class-D switching edges are fast, it is necessary to take care when planning the layout of the printed circuit board. The following suggestions will help to meet EMC requirements.

Decoupling capacitors—The high-frequency decoupling capacitors should be placed as close to the PVCC and AVCC terminals as possible. Large (220 µF or greater) bulk power supply decoupling capacitors should be placed near the NS4225 on the PVCCL and PVCCR supplies. Local, high-frequency bypass capacitors should be placed as close to the PVCC pins as possible. These caps can be connected to the thermal pad directly for an excellent ground nnecticoon. Consider adding a small, good quality low ESR ceramic capacitor between 220 pF and 1000 pF and a larger mid-frequency cap of value between 0.1µF and 1µF also of good quality to the PVCC connections at each end of the chip.

Keep the current loop from each of the outputs through the ferrite bead and the small filter cap and back to PGND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.

Analog ground and power ground should be connected at the thermal pad, which should be used as a central ground connection or star ground for the NS4225.

11.10 Test Setup for Performance Testing

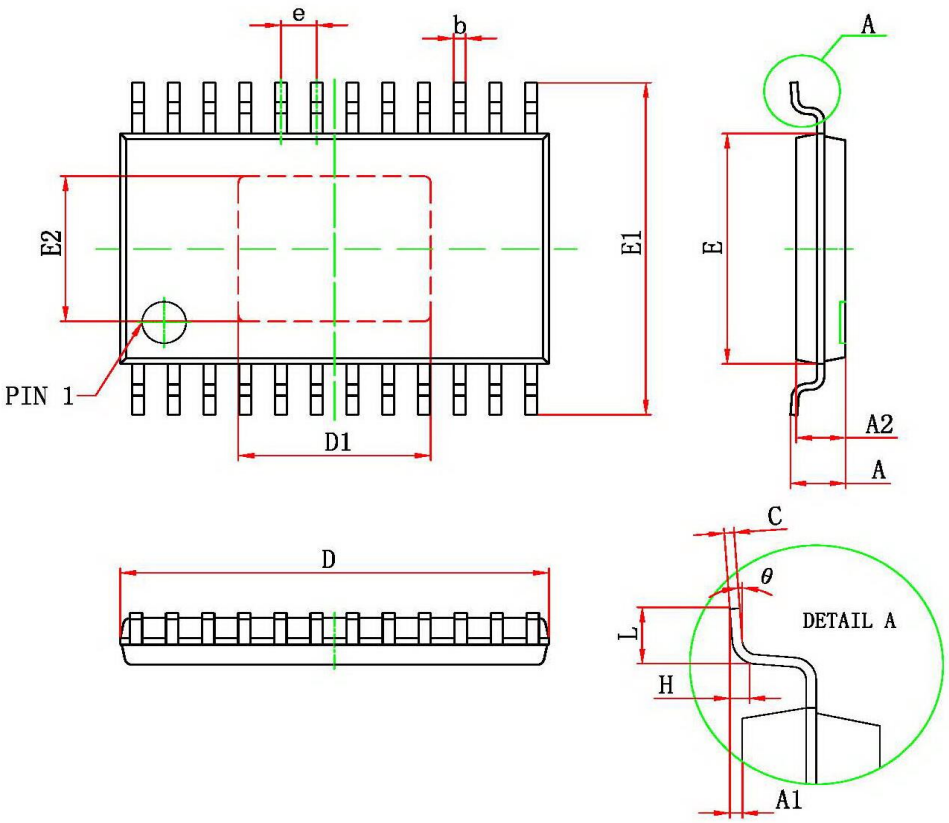


Typical Testing Circuit

Notes

1. The AP AUX-0025 low pass filter is necessary for class-D amplifier measurement with AP analyzer.
2. Two33µH inductors are used in series with load resistor to emulate the small speaker for efficiency measurement.

12 Physical Size of Chip Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	7.700	7.900	0.303	0.311
D1	3.950	4.150	0.156	0.163
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
E2	2.750	2.950	0.108	0.116
A		1.100		0.043
A2	0.800	1.000	0.031	0.039
A1	0.020	0.150	0.001	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°