Description：

74HC32 is a low-power 2-input or gate integrated circuit designed using advanced CMOS technology. It is internally integrated with four sets of 2 input or gate circuits, each of which is designed with a buffer stage push-pull output, and has strong anti-interference and driving capabilities. Its logic functions and standard pin definitions are compatible with the 54/74LS series logic gates.

Features：

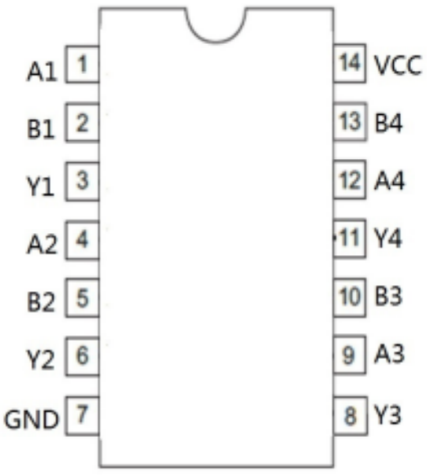
-Low input current: ≤ 1uA
-Low static power consumption: Icc ≤ 5.5uA, @ VCC=6V, Ta=25 ℃
-Wide working voltage range: 2.0V to 6.0V
-Packaging form: DIP14, SOP14

Application:

-Digital logic driven
-Industrial control applications (such as answering machines, programmable devices), etc
-Other application areas

Pin Assignment：

PIN NO. DIP14/SOP14	Pin Definition	PIN NO. DIP14/SOP14	Pin Definition
1	A1	14	VCC
2	B1	13	B4
3	Y1	12	A4
4	A2	11	Y4
5	B2	10	B3
6	Y2	9	A3
7	GND	8	Y3

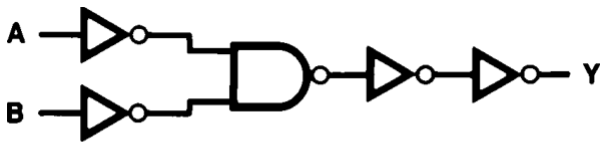


Absolute Maximum Ratings：

parameter	symbol	Limit value	UNIT
working voltage	V_{CC}	6.5	V
Input/output voltage	V_{IN}、V_{OUT}	-0.3-Vcc+0.3V	V
Single pin output current	I_{OUT}	±25	mA
VCC or GND current	I_{CC}	±50	mA
Dissipated power	P_D	500	mW
working temperature	T_A	0-70	℃
Storage temperature	T_S	-65-150	℃
Pin welding temperature	T_W	260,10s	℃

Note: Limit parameters refer to the limit values that cannot be exceeded under any conditions. If this limit value is exceeded, it may cause physical damage such as product degradation; At the same time, it cannot be guaranteed that the chip can function properly when approaching the limit parameters.

Principle logic diagram



$Y = A + B$

Truth table

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H=High logic level

L=low logic level

Recommended operating conditions

parameter	symbol		min	typ	max	unit
working voltage	V_{CC}		2	5	6	V
Input and output voltage	V_{IN}、Vout		0		VCC	V
Input rise/ Descent time	t_{THL} t_{TLH}	VCC=2.0V	0		1000	ns
		VCC=4.5V	0		500	ns
		VCC=6.0V	0		400	ns
working temperature	T_A		0		60	℃

electrical characteristic (TA=25°C, Unless otherwise specified)

DC electrical characteristics

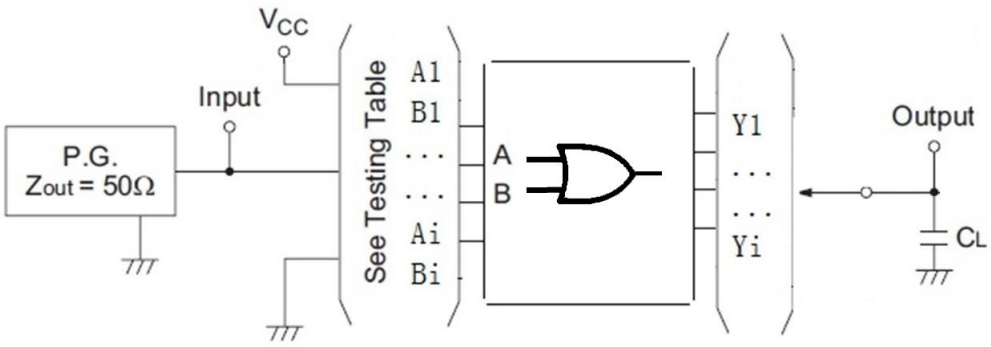
symbol	parameter	Test conditions		VCC(V)	min	typ		unit
V_{IH}	High level effective input voltage			2.0	1.5			V
				4.5	3.15			V
				6.0	4.2			V
V_{IL}	Low level effective input voltage			2.0			0.5	V
				4.5			1.35	V
				6.0			1.8	V
V_{OH}	High level output voltage	V_I= V_{IH} or V_{IL} $|I_{OUT}|\leqslant$20μA		2.0	1.9			V
				4.5	4.4			V
				6.0	5.9			V
		V_I= V_{IH} or V_{IL}	$|I_{OUT}|\leqslant$4.0mA	4.5	3.7	4.4		V
			$|I_{OUT}|\leqslant$5.2mA	6.0	5.2	5.8		V
V_{OL}	Low level output voltage	V_I= V_{IH} or V_{IL} $|I_{OUT}|\leqslant$20μA		2.0			0.1	V
				4.5			0.1	V
				6.0			0.1	V
		V_I= V_{IH} or V_{IL}	$|I_{OUT}|\leqslant$4.0mA	4.5		0.06	0.4	V
			$|I_{OUT}|\leqslant$5.2mA	6.0		0.07	0.5	V
I_{IN}	Input current	V_I=V_{CC} or GND		6.0			1	uA
I_{CC}	Working current	V_I=V_{CC} or GND,I_{OUT}=0μA		6.0			5.5	uA

AC electrical characteristics: Ta=25 ℃ VCC=5.0V, tr=tf ⩽ 20ns, see test method.

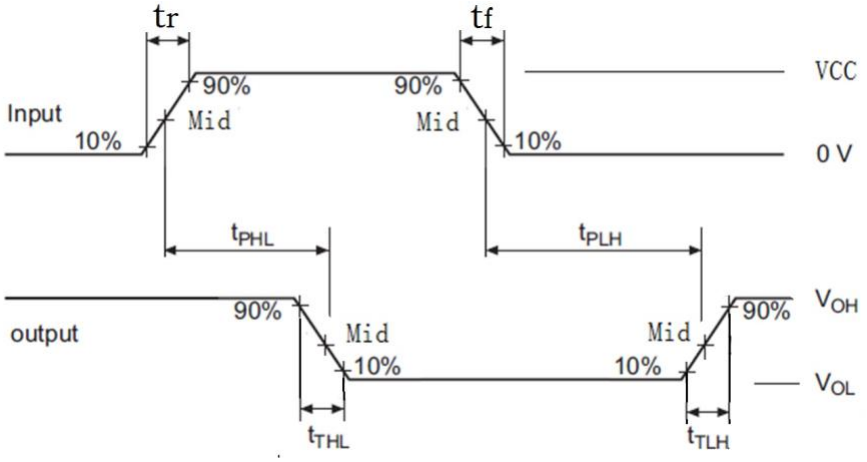
parameter	symbol	test conditions	min	typ	max	unit
Maximum transmission delay time A、B to Y	t_{PHL}	C_L=15pF		18		ns
	t_{PLH}	C_L=15pF		15		ns

test method

1. Test wiring diagram



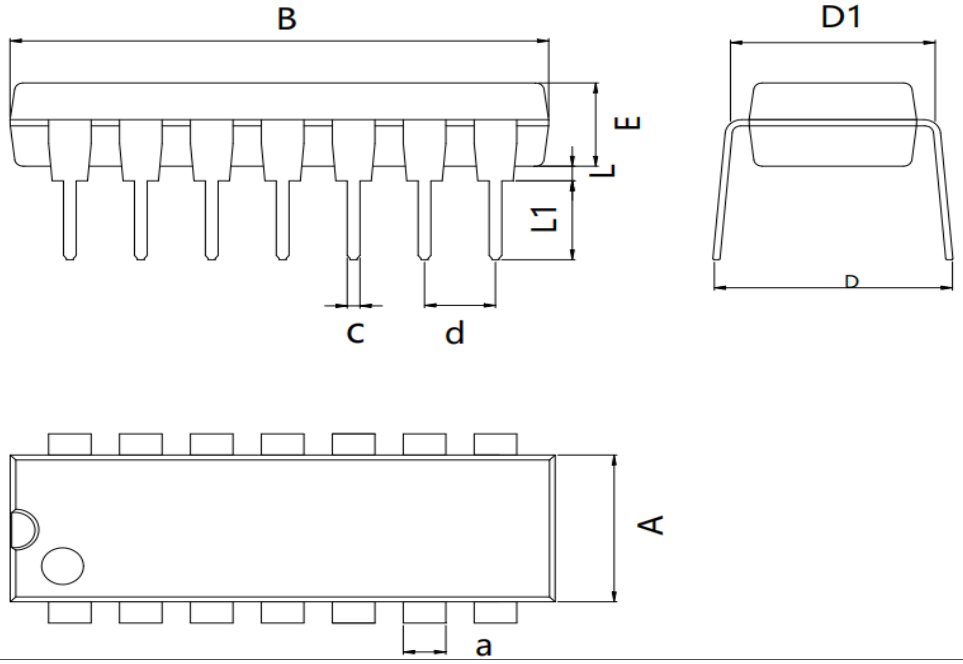
2. Diagram of waveform measurement



Note: 1. See Testing Table refers to the corresponding testing items in the AC electrical characteristics table;
2. The CL capacitor is an external patch capacitor (0603), which is connected near the output pin and grounded near the chip GND;
3. Input: Port input level, f=500kHz, D=50%; Tr=tf ≤ 20ns;
4. Output: Y-end output test.

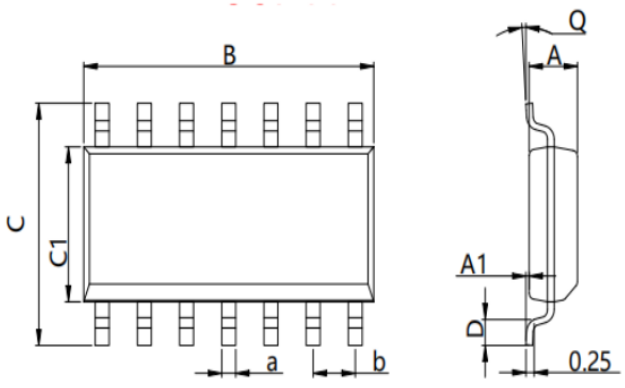
PACKAGE MECHANICAL DATA

DIP14



Dimensions In Millimeters(DIP14)										
Symbol:	A	B	D	D1	E	L	L1	a	C	d
Min:	6.10	18.94	8.40	7.42	3.10	0.50	3.00	1.50	0.40	2.54 BSC
Max:	6.68	19.56	9.00	7.82	3.55	0.70	3.60	1.55	0.50	

SOP14



Dimensions In Millimeters(SOP14)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	8.55	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	8.75	6.20	4.00	0.80	8°	0.45	