General Description

The 74HC74 are dual positive edge triggered D-type flip-flop. They have individual data (nD), clock (nCP), set ($n\overline{SD}$) and reset ($n\overline{RD}$) inputs, and complementary nQ and $n\overline{Q}$ outputs. Data at the nD-input, that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition, is stored in the flip-flop and appears at the nQ output. Schmitt-trigger action in the clock input, makes the circuit highly tolerant to slower clock rise and fall times. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

Features:

- Symmetrical output impedance
- Low power dissipation
- Balanced propagation delays
- Specified from -40℃ to +105℃
- Packaging information: DIP14/SOP14.

Block Diagram And Pin Description

、Block Diagram

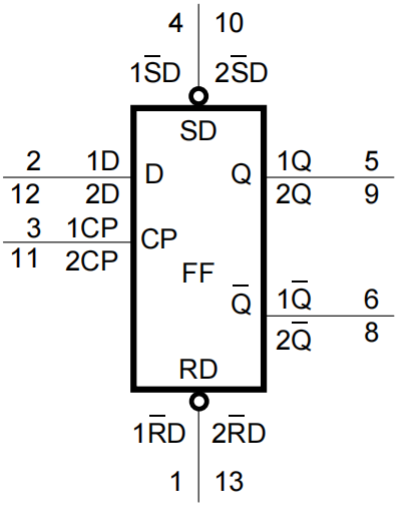


Figure 1. Logic symbol

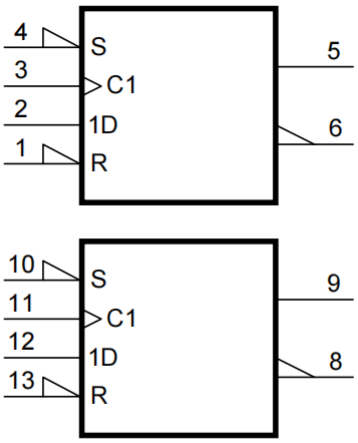


Figure 2. IEC logic symbol

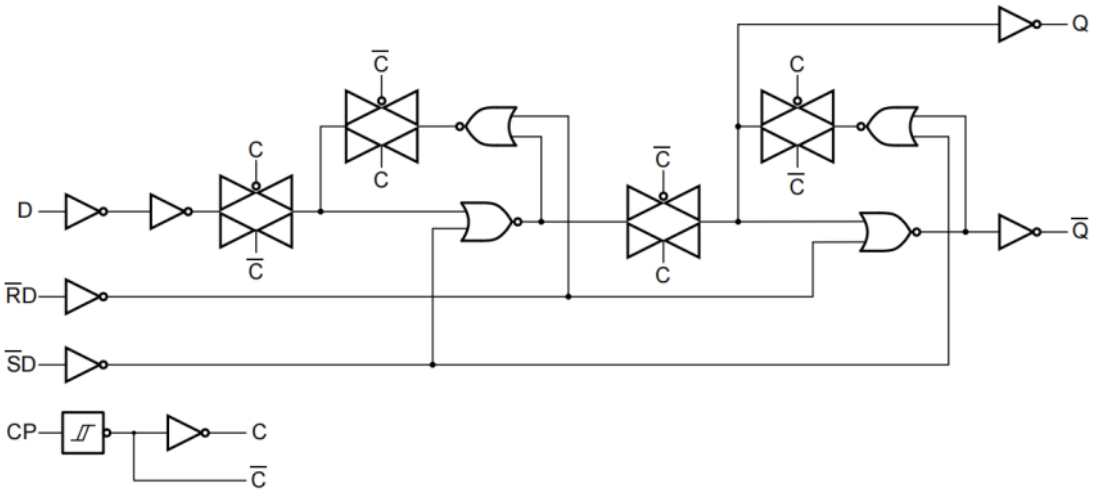


Figure 3. Logic diagram for one flip-flop

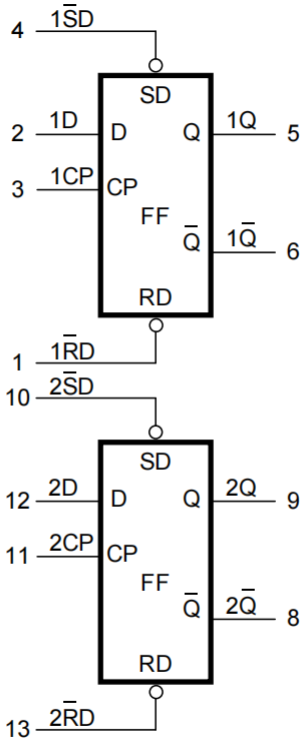
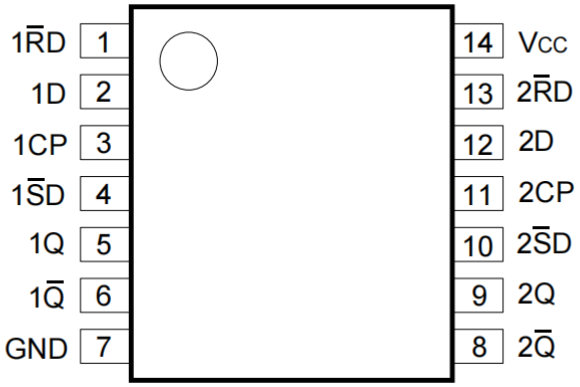


Figure 4. Functional diagram

Pin Configurations



Pin No.	Pin Name	Description
1	1$\overline{R}$D	asynchronous reset-direct input (active LOW)
2	1D	data input
3	1CP	clock input (LOW-to-HIGH, edge-triggered)
4	1$\overline{S}$D	asynchronous set-direct input (active LOW)
5	1Q	output
6	1$\overline{Q}$	complement output
7	GND	ground (0V)
8	2$\overline{Q}$	complement output
9	2Q	output
10	2$\overline{S}$D	asynchronous set-direct input (active LOW)
11	2CP	clock input (LOW-to-HIGH, edge-triggered)
12	2D	data input
13	2$\overline{R}$D	asynchronous reset-direct input (active LOW)
14	V_{CC}	supply voltage

Function Table

Input				Output	
n$\overline{S}$D	**n$\overline{R}$D**	**nCP**	**nD**	**nQ**	**n$\overline{Q}$**
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

Input				Output	
n$\overline{S}$D	**n$\overline{R}$D**	**nCP**	**nD**	**nQ_{n+1}**	**$n\overline{Q}_{n+1}$**
H	H	↑	L	L	H
H	H	↑	H	H	L

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care;
↑=LOW-to-HIGH transition; Qn+1=state after the next LOW-to-HIGH CP transition.

Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{CC}	-		-0.5	+7	V
input clamping current	I_{IK}	$V_I < -0.5V$ or $V_I > V_{CC}+0.5V$		-	±20	mA
output clamping current	I_{OK}	$V_O < -0.5V$ or $V_O > V_{CC}+0.5V$		-	±20	mA
output current	I_O	$-0.5V < V_O < V_{CC}+0.5V$		-	±25	mA
supply current	I_{CC}	-		-	100	mA
ground current	I_{GND}	-		-100	-	mA
total power dissipation	P_{tot}	-		-	500	mW
storage temperature	T_{stg}	-		-65	+150	℃
soldering temperature	T_L	10s	DIP	245		℃
			SOP	250		

Note:

[1] For DIP14 packages: above 70℃ the value of P_{tot} derates linearly with 12mW/K.

[2] For SOP14 packages: above 70℃ the value of P_{tot} derates linearly with 8mW/K.

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
74HC74						
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	$\Delta t/\Delta V$	V_{CC}=2.0V	-	-	625	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	83	ns/V
ambient temperature	T_{amb}	-	-40	-	+105	℃

DC Characteristics

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
74HC74							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	1.2	-	V
		V_{CC}=4.5V		3.15	2.4	-	V
		V_{CC}=6.0V		4.2	3.2	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	0.8	0.5	V
		V_{CC}=4.5V		-	2.1	1.35	V
		V_{CC}=6.0V		-	2.8	1.8	V
HIGH-level output voltage	V_{OH}	$V_I=V_{IH}$ or V_{IL}	I_O=-4.0mA; V_{CC}=4.5V	3.84	4.32	-	V
			I_O=-5.2mA; V_{CC}=6.0V	5.34	5.81	-	V
LOW-level output voltage	V_{OL}	$V_I=V_{IH}$ or V_{IL}	I_O=4.0mA; V_{CC}=4.5V	-	0.15	0.33	V
			I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.33	V
input leakage current	I_I	$V_I=V_{CC}$ or GND; V_{CC}=6.0V		-	-	±1.0	uA
supply current	I_{CC}	$V_I=V_{CC}$ or GND; I_O=0A; V_{CC}=6.0V		-	-	40	uA
input capacitance	C_I	-		-	3.5	-	pF

AC Characteristics

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
74HC74							
nCP to nQ,n$\overline{Q}$ propagation delay	t_{pd}	see Figure 6[1]	V_{CC}=2.0V	-	47	220	ns
			V_{CC}=4.5V	-	17	44	ns
			V_{CC}=5.0V;C_L=15pF	-	14	-	ns
			V_{CC}=6.0V	-	14	37	ns
n$\overline{SD}$ to nQ,n$\overline{Q}$ propagation delay	t_{pd}	see Figure 7[1]	V_{CC}=2.0V	-	50	250	ns
			V_{CC}=4.5V	-	18	50	ns
			V_{CC}=5.0V;C_L=15pF	-	15	-	ns
			V_{CC}=6.0V	-	14	43	ns
n$\overline{RD}$ to nQ,n$\overline{Q}$ propagation delay	t_{pd}	see Figure 7[1]	V_{CC}=2.0V	-	52	250	ns
			V_{CC}=4.5V	-	19	50	ns
			V_{CC}=5.0V;C_L=15pF	-	16	-	ns
			V_{CC}=6.0V	-	15	43	ns
nQ,n$\overline{Q}$ transition time	t_t	see Figure 6[2]	V_{CC}=2.0V	-	19	95	ns
			V_{CC}=4.5V	-	7	19	ns
			V_{CC}=6.0V	-	6	16	ns
CP pulse width	t_W	see Figure 6	V_{CC}=2.0V	100	19	-	ns
			V_{CC}=4.5V	20	7	-	ns
			V_{CC}=6.0V	17	6	-	ns
n$\overline{SD}$, n$\overline{RD}$ pulse width	t_W	see Figure 7	V_{CC}=2.0V	100	19	-	ns
			V_{CC}=4.5V	20	7	-	ns
			V_{CC}=6.0V	17	6	-	ns
n$\overline{SD}$, n$\overline{RD}$ recovery time	t_{rec}	see Figure 7	V_{CC}=2.0V	40	3	-	ns
			V_{CC}=4.5V	8	1	-	ns
			V_{CC}=6.0V	7	1	-	ns
nD to nCP set-up time	t_{su}	see Figure 6	V_{CC}=2.0V	75	6	-	ns
			V_{CC}=4.5V	15	2	-	ns
			V_{CC}=6.0V	13	2	-	ns
nD to nCP hold time	t_h	see Figure 6	V_{CC}=2.0V	3	-6	-	ns
			V_{CC}=4.5V	3	-2	-	ns
			V_{CC}=6.0V	3	-2	-	ns
nCP maximum frequency	f_{max}	see Figure 6	V_{CC}=2.0V	4.8	23	-	MHz
			V_{CC}=4.5V	24	69	-	MHz
			V_{CC}=5.0V;C_L=15pF	-	76	-	MHz
			V_{CC}=6.0V	28	82	-	MHz
power dissipation capacitance	C_{PD}	C_L=50pF;f=1 MHz; V_I= GND to V_{CC}[3]		-	24	-	pF

Testing Circuit

AC Testing Circuit

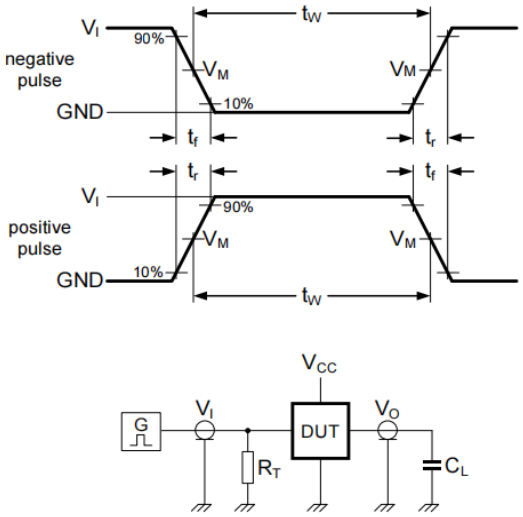


Figure 5. Test circuit for measuring switching times

Definitions for test circuit:

C_L=load capacitance including jig and probe capacitance.

R_T=termination resistance should be equal to the output impedance Z_o of the pulse generator.

AC Testing Waveforms

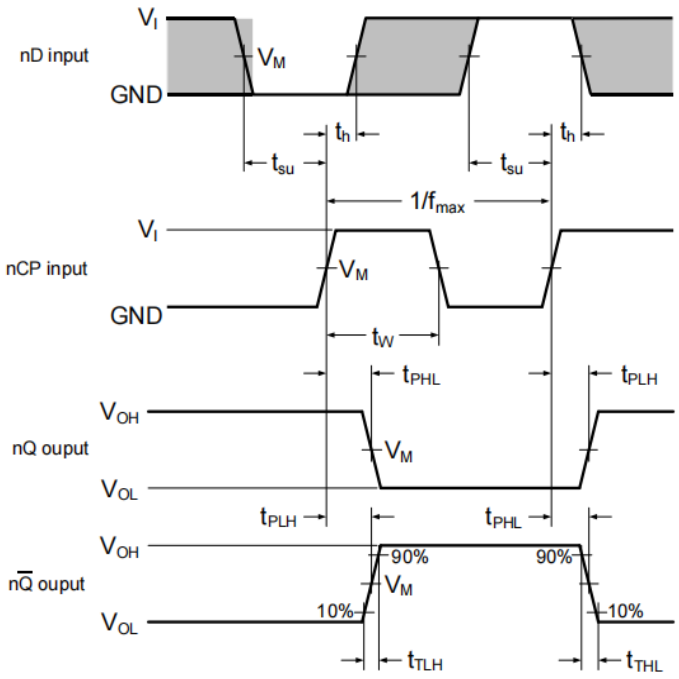


Figure 6. Input to output propagation delays

Measurement Points

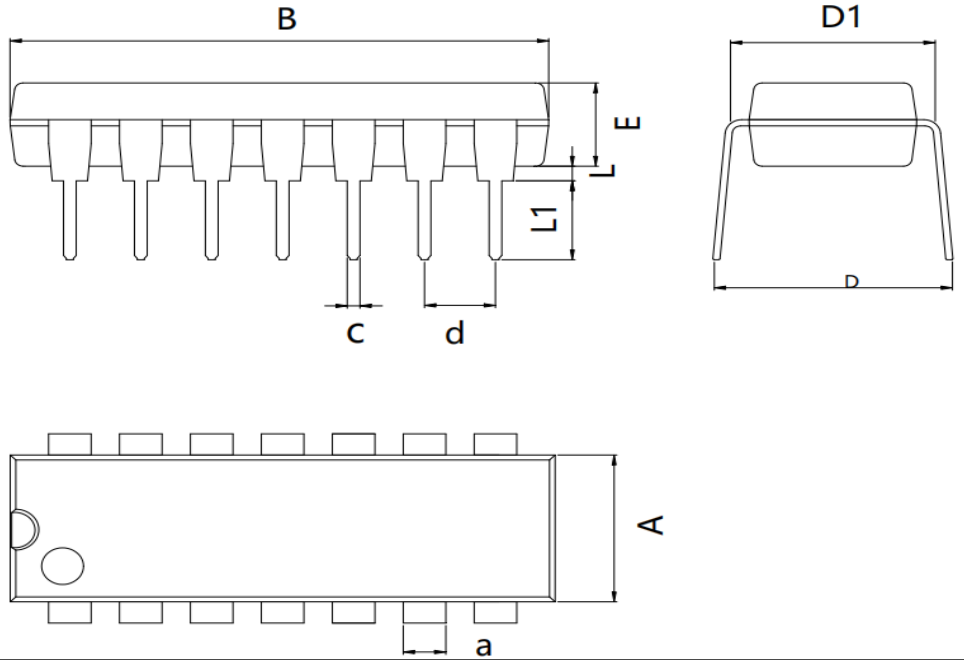
Type	Input	Output
	V_M	V_M
74HC74	$0.5\times V_{CC}$	$0.5\times V_{CC}$

Test Data

Type	Input		Load		Test
	V_I	t_r , t_f	C_L	R_L	
74HC74	V_{CC}	6.0ns	15pF, 50pF	1kΩ	t_{PLH}, t_{PHL}

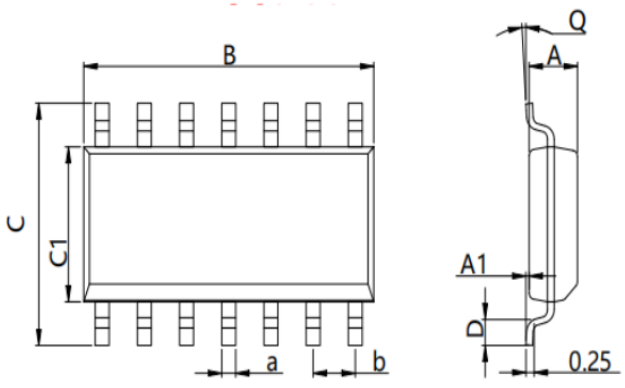
PACKAGE MECHANICAL DATA

DIP14



Dimensions In Millimeters(DIP14)										
Symbol:	A	B	D	D1	E	L	L1	a	C	d
Min:	6.10	18.94	8.40	7.42	3.10	0.50	3.00	1.50	0.40	2.54 BSC
Max:	6.68	19.56	9.00	7.82	3.55	0.70	3.60	1.55	0.50	

SOP14



Dimensions In Millimeters(SOP14)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	8.55	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	8.75	6.20	4.00	0.80	8°	0.45	