Octal D-type transparent latch; 3-state

Description

The 74HC373 is a high-speed Si-gate CMOS device and is pin compatible with

Low-power Schottky TTL. It is specified in compliance with JEDEC standard no. 7A

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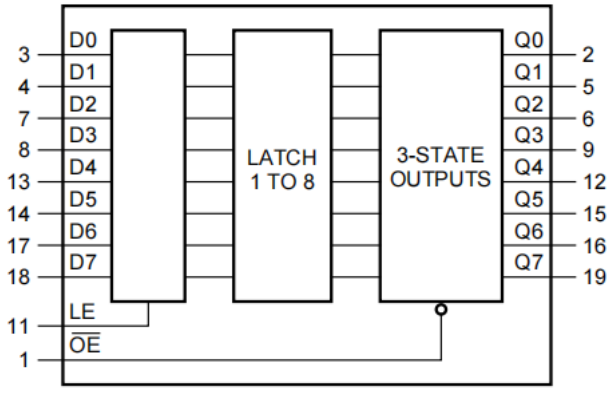
Features

3-state non-inverting outputs for bus oriented applications
Common 3-state output enable input
Functionally identical to 74HC573 ESD protection:

Applications

3-state non-inverting outputs for bus
oriented applications
Common 3-state output enable input
Functionally identical

Functional diagram



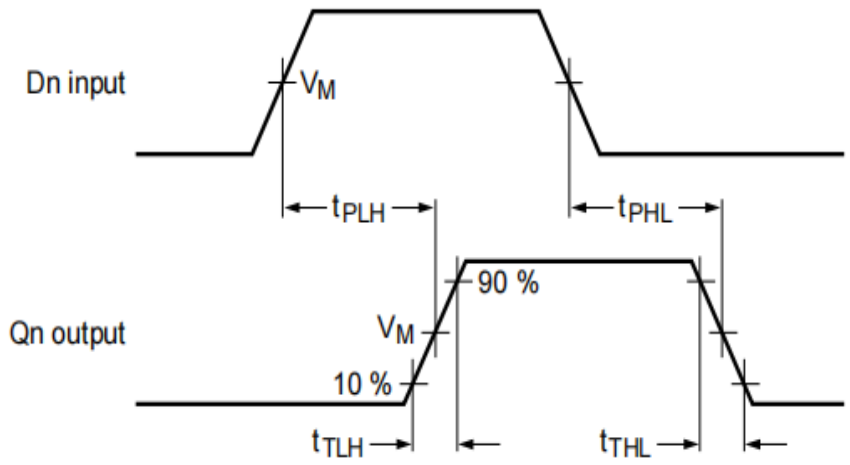
Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)	-	±35	mA
I_{CC}	supply current		-	+70	mA
I_{GND}	ground current		-	−70	mA
T_{stg}	storage temperature		−65	+150	°C
P_{tot}	total power dissipation				

Recommended Operating Conditions

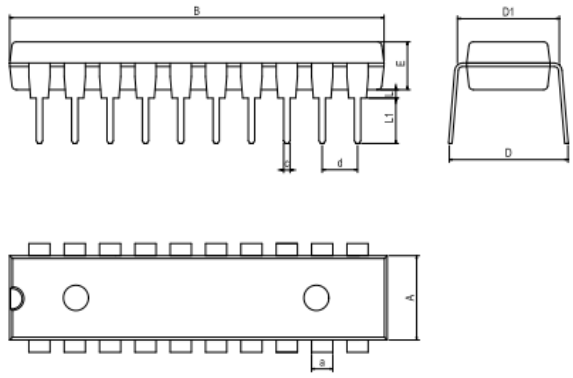
Symbol	Parameter	Conditions	Min	Typ	Max
V_{CC}	supply voltage		2.0	5.0	6.0
V_I	input voltage		0	-	V_{CC}
V_O	output voltage		0	-	V_{CC}
T_{amb}	ambient temperature		−40	+25	+125
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0$ V	-	-	625
		$V_{CC} = 6.0$ V	-	-	83

Waveforms



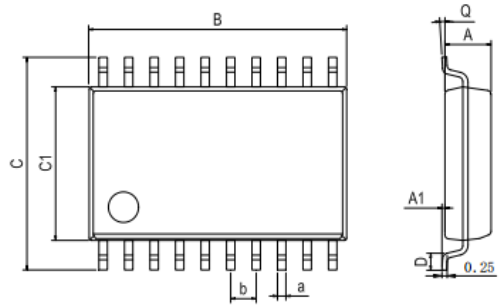
PIN DATA

DIP20



Dimensions In Millimeters(DIP20)										
Symbol:	A	B	D	D1	E	L	L1	a	c	d
Min:	6.10	24.95	8.40	7.42	3.10	0.50	3.00	1.50	0.40	2.54 BSC
Max:	6.68	26.55	9.00	7.82	3.55	0.70	3.60	1.55	0.50	

SOP20



Dimensions In Millimeters(SOP20L)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	2.10	0.05	12.50	10.21	7.40	0.45	0	0.35	1.27 BSC
Max:	2.50	0.25	13.00	10.61	7.60	1.25	8	0.45	