100V_{IN} Micropower Isolated Flyback Converter with 150V/450mA Switch

FEATURES

- **5.5V to 100V Input Voltage Range**
- **450mA, 150V Internal DMOS Power Switch**
- **Up to 5W of Output Power**
- **Low Quiescent Current:**
  - **70µA in Sleep Mode**
  - **280µA in Active Mode**
- **Boundary Mode Operation at Heavy Load**
- **Low Ripple Burst Mode® Operation at Light Load**
- **Minimum Load <0.5% (Typ) of Full Output**
- **V_{OUT} Set with a Single External Resistor**
- No Transformer Third Winding or Opto-Isolator Required for Regulation
- Accurate EN/UVLO Threshold and Hysteresis
- Internal Compensation and Soft-Start
- 5-Lead TSOT-23 Package

APPLICATIONS

- Isolated Telecom, Datacom, Automotive, Industrial, and Medical Power Supplies
- Isolated Auxiliary/Housekeeping Power Supplies

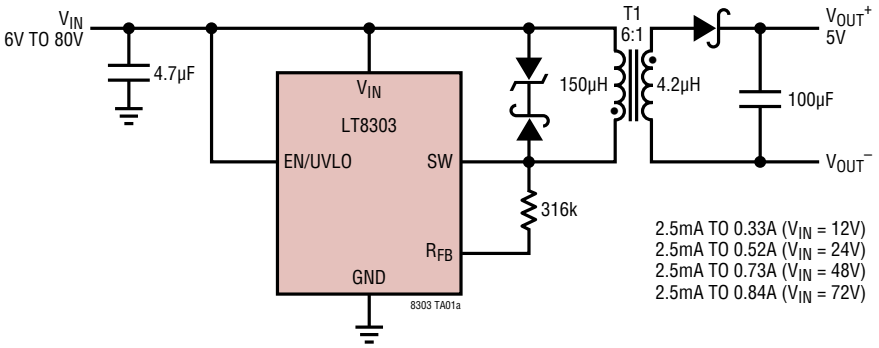
DESCRIPTION

The LT®8303 is a micropower high voltage isolated flyback converter. By sampling the isolated output voltage directly from the primary-side flyback waveform, the part requires no third winding or opto-isolator for regulation. The output voltage is programmed with a single external resistor. Internal compensation and soft-start further reduce external component count. Boundary mode operation provides a small magnetic solution with excellent load regulation. Low ripple Burst Mode operation maintains high efficiency at light load while minimizing the output voltage ripple. A 450mA, 150V DMOS power switch is integrated along with all high voltage circuitry and control logic into a 5-lead ThinSOT™ package.

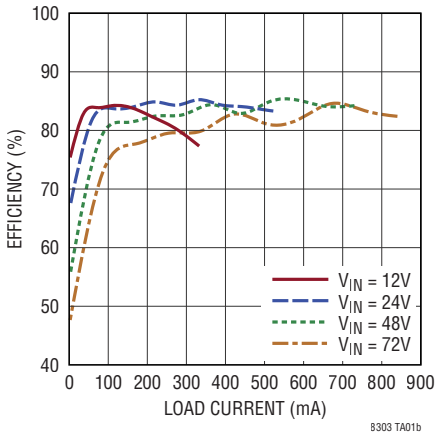
The LT8303 operates from an input voltages range of 5.5V to 100V and can deliver up to 5W of isolated output power. The high level of integration and the use of boundary mode and low ripple Burst Mode operations result in a simple to use, low component count, and high efficiency application solution for isolated power delivery.

TYPICAL APPLICATION

6V to 80V_{IN}, 5V_{OUT} Isolated Flyback Converter



Efficiency vs Load Current

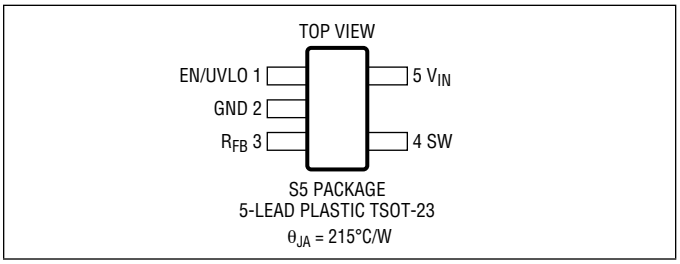


ABSOLUTE MAXIMUM RATINGS

(Note 1)

SW (Note 2) 150V
V_{IN} 100V
EN/UVLO..... V_{IN}
R_{FB}..... V_{IN} – 0.5V to V_{IN}
Current into R_{FB} 200µA
Operating Junction Temperature Range (Notes 3, 4)
LT8303E, LT8303I ..... –40°C to 125°C
LT8303H..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



ORDER INFORMATION

http://www.linear.com/product/LT8303#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8303ES5#PBF	LT8303ES5#TRPBF	LTGXH	5-Lead Plastic TSOT-23	–40°C to 125°C
LT8303IS5#PBF	LT8303IS5#TRPBF	LTGXH	5-Lead Plastic TSOT-23	–40°C to 125°C
LT8303HS5#PBF	LT8303HS5#TRPBF	LTGXH	5-Lead Plastic TSOT-23	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 24V, $V_{EN/UVLO}$ = V_{IN} unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range			5.5		100	V
	V_{IN} UVLO Threshold	Rising Falling			5.3 3.2	5.5	V V
I_Q	V_{IN} Quiescent Current	$V_{EN/UVLO}$ = 0.3V $V_{EN/UVLO}$ = 1.1V Sleep Mode (Switch Off) Active Mode (Switch On)			1.5 200 70 280	2.5	µA µA µA µA
	EN/UVLO Shutdown Threshold	For Lowest Off I_Q	●	0.3	0.75		V
	EN/UVLO Enable Threshold	Falling Hysteresis	●	1.186	1.223 0.016	1.284	V V
I_{HYS}	EN/UVLO Hysteresis Current	$V_{EN/UVLO}$ = 0.3V $V_{EN/UVLO}$ = 1.1V $V_{EN/UVLO}$ = 1.3V		–0.1 2.1 –0.1	0 2.5 0	0.1 2.9 0.1	µA µA µA
f_{MAX}	Maximum Switching Frequency			320	350	380	kHz
f_{MIN}	Minimum Switching Frequency			5	7	9	kHz
$t_{ON(MIN)}$	Minimum Switch-On Time				160		ns
$t_{OFF(MIN)}$	Minimum Switch-Off Time	V_{IN} = $V_{EN/UVLO}$ = 12V			350		ns
$t_{OFF(MAX)}$	Maximum Switch-Off Time	Backup Timer			200		µs
$I_{SW(MAX)}$	Maximum SW Current Limit			450	535	620	mA
$I_{SW(MIN)}$	Minimum SW Current Limit			70	105	140	mA
	SW Over Current Limit	To Initiate Soft-Start			1		A
$R_{DS(ON)}$	Switch On-Resistance	I_{SW} = 100mA			3.2		Ω
I_{LKG}	Switch Leakage Current	V_{IN} = 100V, V_{SW} = 150V			0.1	0.5	µA
I_{RFB}	R_{FB} Regulation Current		●	97.5	100	102.5	µA
	R_{FB} Regulation Current Line Regulation	5.5V ≤ V_{IN} ≤ 100V			0.001	0.01	%/V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

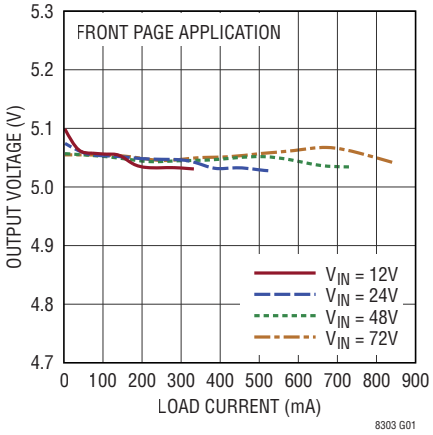
Note 2: The SW pin is rated to 150V for transients. Depending on the leakage inductance voltage spike, operating waveforms of the SW pin should be derated to keep the flyback voltage spike below 150V as shown in Figure 5.

Note 3: The LT8303E is guaranteed to meet performance specifications from 0°C to 125°C operating junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8303I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT8303H is guaranteed over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

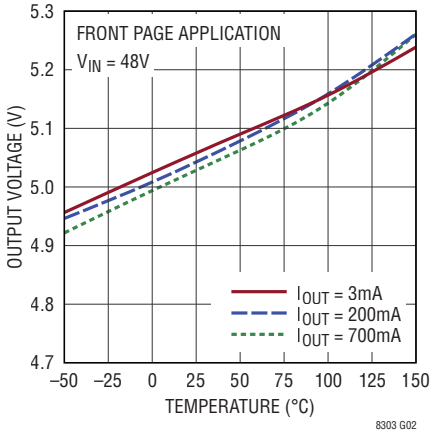
Note 4: The LT8303 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

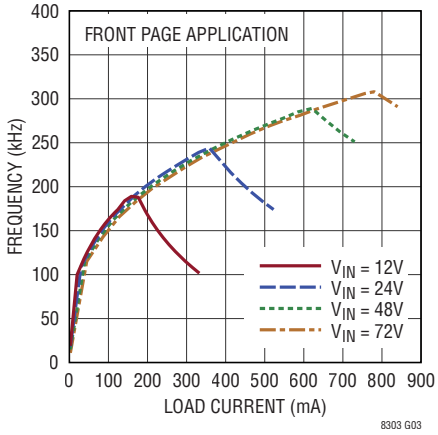
Output Load and Line Regulation



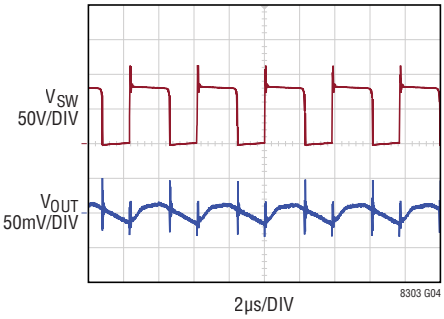
Output Temperature Variation



Switching Frequency vs Load Current



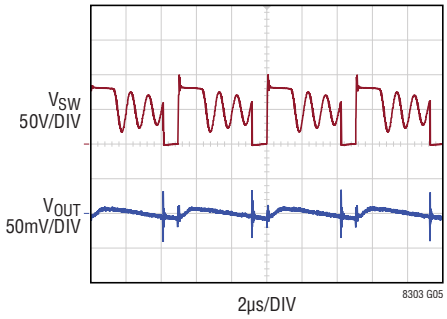
Boundary Mode Waveforms



FRONT PAGE APPLICATION

V_{IN} = 48V, I_{OUT} = 700mA

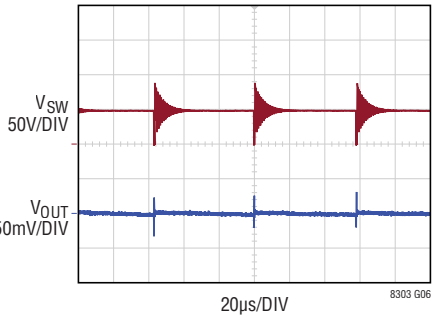
Discontinuous Mode Waveforms



FRONT PAGE APPLICATION

V_{IN} = 48V, I_{OUT} = 200mA

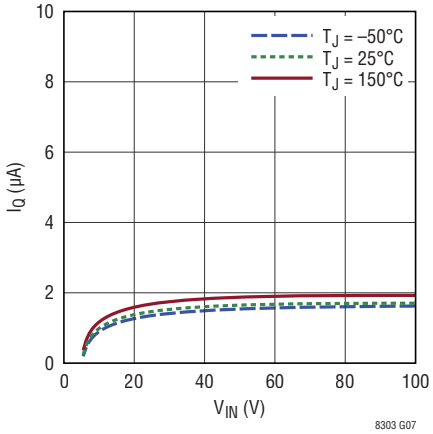
Burst Mode Waveforms



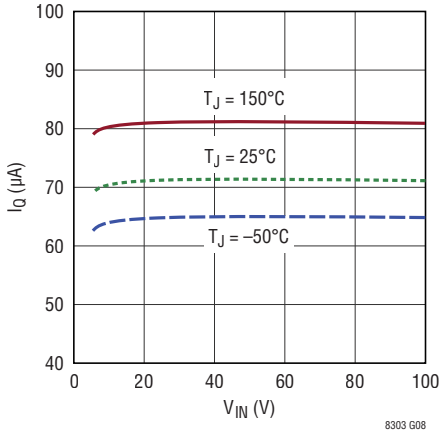
FRONT PAGE APPLICATION

V_{IN} = 48V, I_{OUT} = 3mA

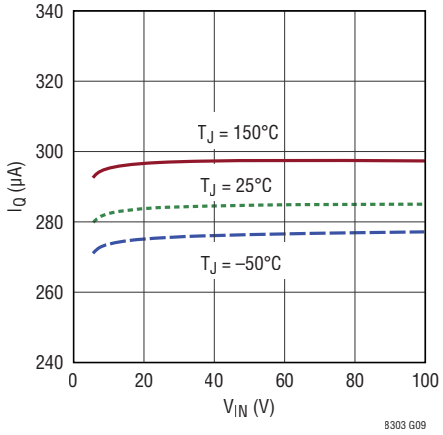
V_{IN} Shutdown Current



V_{IN} Quiescent Current, Sleep Mode

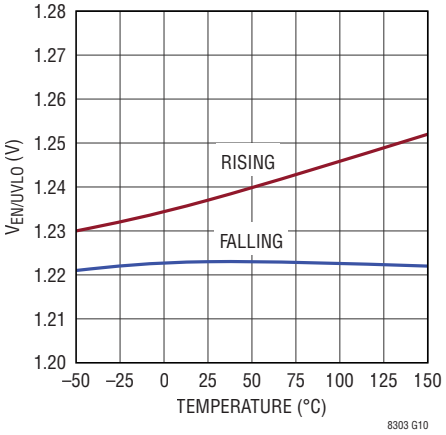


V_{IN} Quiescent Current, Active Mode

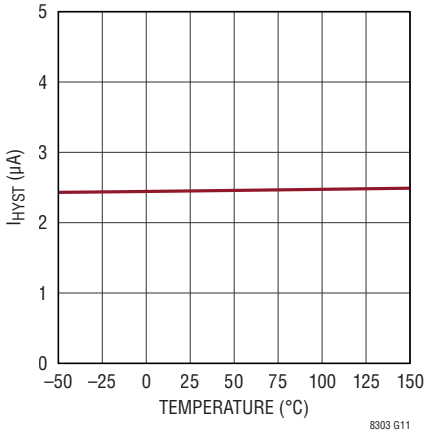


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

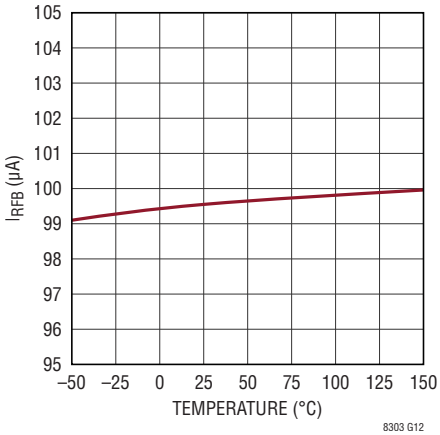
EN/UVLO Enable Threshold



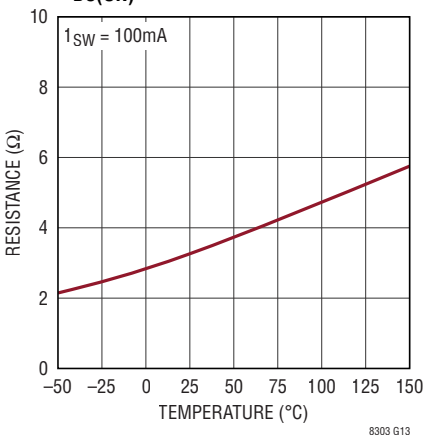
EN/UVLO Hysteresis Current



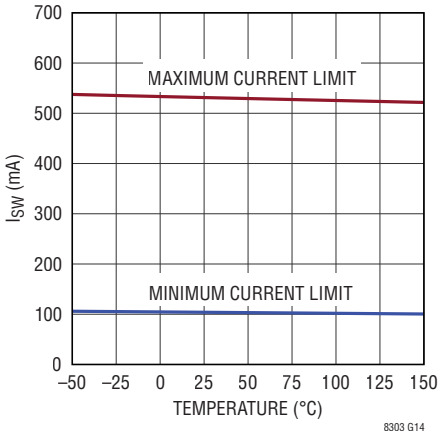
R_{FB} Regulation Current



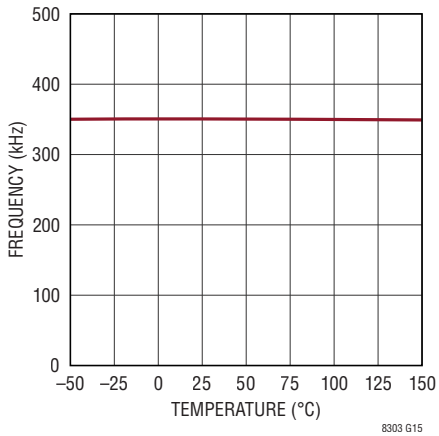
$R_{DS(ON)}$



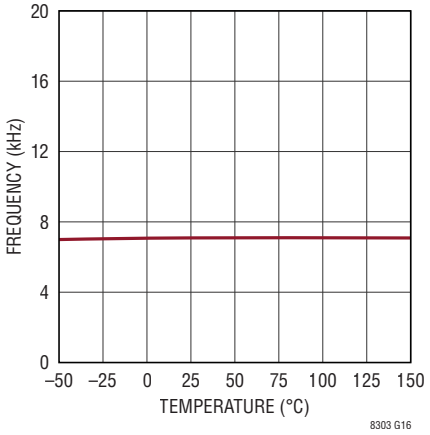
Switch Current Limit



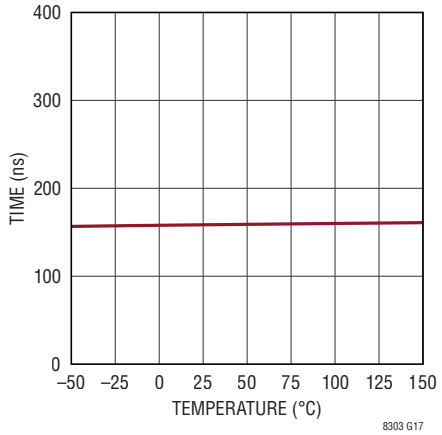
Maximum Switching Frequency



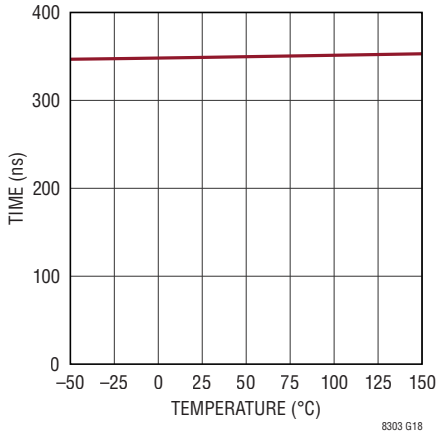
Minimum Switching Frequency



Minimum Switch-On Time



Minimum Switch-Off Time



PIN FUNCTIONS

EN/UVLO (Pin 1): Enable/Undervoltage Lockout. The EN/UVLO pin is used to enable the LT8303. Pull the pin below 0.3V to shut down the LT8303. This pin has an accurate 1.223V threshold and can be used to program a V_{IN} undervoltage lockout (UVLO) threshold using a resistor divider from V_{IN} to ground. A 2.5µA current hysteresis allows the programming of V_{IN} UVLO hysteresis. If neither function is used, tie this pin directly to V_{IN}.

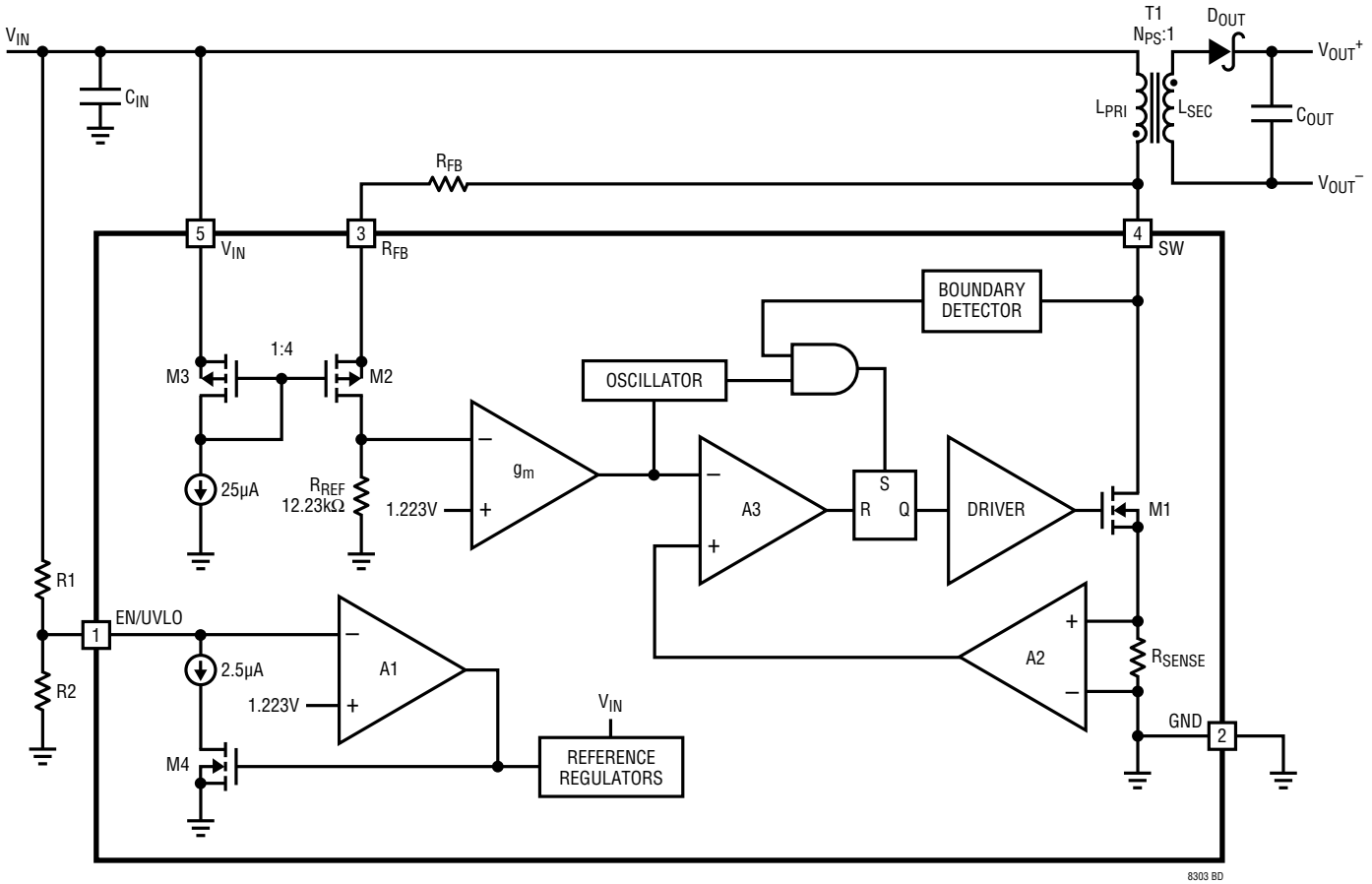
GND (Pin 2): Ground. Tie this pin directly to local ground plane.

R_{FB} (Pin 3): Input Pin for External Feedback Resistor. Connect a resistor from this pin to the transformer primary SW pin. The ratio of the R_{FB} resistor to the internal trimmed 12.23k resistor, times the internal bandgap reference, determines the output voltage (plus the effect of any non-unity transformer turns ratio). Minimize trace area at this pin.

SW (Pin 4): Drain of the 150V Internal DMOS Power Switch. Minimize trace area at this pin to reduce EMI and voltage spikes.

V_{IN} (Pin 5): Input Supply. The V_{IN} pin supplies current to internal circuitry and serves as a reference voltage for the feedback circuitry connected to the R_{FB} pin. Locally bypass this pin to ground with a capacitor.

BLOCK DIAGRAM



OPERATION

The LT8303 is a current mode switching regulator IC designed specially for the isolated flyback topology. The key problem in isolated topologies is how to communicate the output voltage information from the isolated secondary side of the transformer to the primary side for regulation. Historically, opto-isolators or extra transformer windings communicate this information across the isolation boundary. Opto-isolator circuits waste output power, and the extra components increase the cost and physical size of the power supply. Opto-isolators can also cause system issues due to limited dynamic response, nonlinearity, unit-to-unit variation and aging over lifetime. Circuits employing extra transformer windings also exhibit deficiencies, as using an extra winding adds to the transformer's physical size and cost, and dynamic response is often mediocre.

The LT8303 samples the isolated output voltage through the primary-side flyback pulse waveform. In this manner, neither opto-isolator nor extra transformer winding is required for regulation. Since the LT8303 operates in either boundary conduction mode or discontinuous conduction mode, the output voltage is always sampled on the SW pin when the secondary current is zero. This method improves load regulation without the need of external load compensation components.

The LT8303 is a simple to use micropower isolated flyback converter housed in a 5-lead TSOT-23 package. The output voltage is programmed with a single external resistor. By integrating the loop compensation and soft-start inside, the part further reduces the number of external components. As shown in the Block Diagram, many of the blocks are similar to those found in traditional switching regulators including reference, regulators, oscillator, logic, current amplifier, current comparator, driver, and power switch. The novel sections include a flyback pulse sense circuit, a sample-and-hold error amplifier, and a boundary mode detector, as well as the additional logic for boundary conduction mode, discontinuous conduction mode, and low ripple Burst Mode operation.

Boundary Conduction Mode Operation

The LT8303 features boundary conduction mode operation at heavy load, where the chip turns on the primary power switch when the secondary current is zero. Boundary conduction mode is a variable frequency, variable peak-current switching scheme. The power switch turns on and the transformer primary current increases until an internally controlled peak current limit. After the power switch turns off, the voltage on the SW pin rises to the output voltage multiplied by the primary-to-secondary transformer turns ratio plus the input voltage. When the secondary current through the output diode falls to zero, the SW pin voltage collapses and rings around V_{IN}. A boundary mode detector senses this event and turns the power switch back on.

Boundary conduction mode returns the secondary current to zero every cycle, so parasitic resistive voltage drops do not cause load regulation errors. Boundary conduction mode also allows the use of smaller transformers compared to continuous conduction mode and does not exhibit sub-harmonic oscillation.

Discontinuous Conduction Mode Operation

As the load gets lighter, boundary conduction mode increases the switching frequency and decreases the switch peak current at the same ratio. Running at a higher switching frequency up to several MHz increases switching and gate charge losses. To avoid this scenario, the LT8303 has an additional internal oscillator, which clamps the maximum switching frequency to be less than 350kHz (typical). Once the switching frequency hits the internal frequency clamp, the part starts to delay the switch turn-on and operates in discontinuous conduction mode.

Low Ripple Burst Mode Operation

Unlike traditional flyback converters, the LT8303 has to turn on and off at least for a minimum amount of time and with a minimum frequency to allow accurate sampling of the output voltage. The inherent minimum switch current limit and minimum switch-off time are necessary to guarantee the correct operation of specific applications.

As the load gets very light, the LT8303 starts to fold back the switching frequency while keeping the minimum switch current limit. So the load current is able to decrease while still allowing minimum switch-off time for the sample-and-hold error amplifier. Meanwhile, the part switches between sleep mode and active mode, thereby reducing the effec-

OPERATION

tive quiescent current to improve light load efficiency. In this condition, the LT8303 operates in low ripple Burst Mode. The typical 7kHz minimum switching frequency determines how often the output voltage is sampled and also the minimum load requirement.

APPLICATIONS INFORMATION

Output Voltage

The R_{FB} resistor as depicted in the Block Diagram is the only external resistor used to program the output voltage. The LT8303 operates similar to traditional current mode switchers, except in the use of a unique flyback pulse sense circuit and a sample-and-hold error amplifier, which sample and therefore regulate the isolated output voltage from the flyback pulse.

Operation is as follows: when the power switch M1 turns off, the SW pin voltage rises above the V_{IN} supply. The amplitude of the flyback pulse, i.e., the difference between the SW pin voltage and V_{IN} supply, is given as:

$V_{FLBK} = (V_{OUT} + V_F + I_{SEC} \bullet ESR) \bullet N_{PS}$

V_F = Output diode forward voltage

I_{SEC} = Transformer secondary current

ESR = Total impedance of secondary circuit

N_{PS} = Transformer effective primary-to-secondary turns ratio

The flyback voltage is then converted to a current I_{RFB} by the flyback pulse sense circuit (M2 and M3). This current I_{RFB} also flows through the internal trimmed 12.23k R_{REF} resistor to generate a ground-referred voltage. The resulting voltage feeds to the inverting input of the sample-and-hold error amplifier. Since the sample-and-hold error amplifier samples the voltage when the secondary current is zero, the (I_{SEC} • ESR) term in the V_{FLBK} equation can be assumed to be zero.

The bandgap reference voltage V_{BG}, 1.223V, feeds to the non-inverting input of the sample-and-hold error amplifier. The relatively high gain in the overall loop causes the voltage across R_{REF} resistor to be nearly equal to the bandgap reference voltage V_{BG}. The resulting relationship between V_{FLBK} and V_{BG} can be expressed as:

$$\left(\frac{V_{FLBK}}{R_{FB}}\right) \bullet R_{REF} = V_{BG}$$

or

$$V_{FLBK} = \left(\frac{V_{BG}}{R_{REF}}\right) \bullet R_{FB} = I_{RFB} \bullet R_{FB}$$

V_{BG} = Bandgap reference voltage

I_{RFB} = R_{FB} regulation current = 100µA

Combination with the previous V_{FLBK} equation yields an equation for V_{OUT}, in terms of the R_{FB} resistor, transformer turns ratio, and diode forward voltage:

$$V_{OUT} = 100\mu A \bullet \left(\frac{R_{FB}}{N_{PS}}\right) - V_F$$

Output Temperature Coefficient

The first term in the V_{OUT} equation does not have temperature dependence, but the output diode forward voltage V_F has a significant negative temperature coefficient (–1mV/°C to –2mV/°C). Such a negative temperature coefficient produces approximately 200mV to 300mV voltage variation on the output voltage across temperature.

For higher voltage outputs, such as 12V and 24V, the output diode temperature coefficient has a negligible effect on the output voltage regulation. For lower voltage outputs, such as 3.3V and 5V, however, the output diode temperature coefficient does count for an extra 2% to 5% output voltage regulation. For customers requiring tight output voltage regulation across temperature, please refer to other LTC parts with integrated temperature compensation features.

APPLICATIONS INFORMATION

Selecting Actual R_{FB} Resistor Value

The LT8303 uses a unique sampling scheme to regulate the isolated output voltage. Due to the sampling nature, the scheme contains repeatable delays and error sources, which will affect the output voltage and force a re-evaluation of the R_{FB} resistor value. Therefore, a simple two-step process is required to choose feedback resistor R_{FB}.

Rearrangement of the expression for V_{OUT} in the Output Voltage section yields the starting value for R_{FB}:

$$R_{FB} = \frac{N_{PS} \bullet \left(V_{OUT} + V_F\right)}{100\mu A}$$

V_{OUT} = Output voltage

V_F = Output diode forward voltage = ~0.3V

N_{PS} = Transformer effective primary-to-secondary turns ratio

Power up the application with the starting R_{FB} value and other components connected, and measure the regulated output voltage, $V_{OUT(MEAS)}$. The final R_{FB} value can be adjusted to:

$$R_{FB(FINAL)} = \frac{V_{OUT}}{V_{OUT(MEAS)}} \bullet R_{FB}$$

Once the final R_{FB} value is selected, the regulation accuracy from board to board for a given application will be very consistent, typically under ±5% when including device variation of all the components in the system (assuming resistor tolerances and transformer windings matching within ±1%). However, if the transformer or the output diode is changed, or the layout is dramatically altered, there may be some change in V_{OUT}.

Output Power

A flyback converter has a complicated relationship between the input and output currents compared to a buck or a boost converter. A boost converter has a relatively constant maximum input current regardless of input voltage and a buck converter has a relatively constant maximum output current regardless of input voltage. This is due to the continuous non-switching behavior of the two currents. A flyback converter has both discontinuous input and output currents which make it similar to a non-isolated buck-boost converter. The duty cycle will affect the input and output currents, making it hard to predict output power. In addition, the winding ratio can be changed to multiply the output current at the expense of a higher switch voltage.

The graphs in Figures 1 to 4 show the typical maximum output power possible for the output voltages 3.3V, 5V, 12V, and 24V. The maximum output power curve is the calculated output power if the switch voltage is 120V during the switch-off time. 30V of margin is left for leakage inductance voltage spike. To achieve this power level at a given input, a winding ratio value must be calculated to stress the switch to 120V, resulting in some odd ratio values. The curves below the maximum output power curve are examples of common winding ratio values and the amount of output power at given input voltages.

One design example would be a 5V output converter with a minimum input voltage of 30V and a maximum input voltage of 80V. A six-to-one winding ratio fits this design example perfectly and outputs equal to 4.35W at 80V but lowers to 2.95W at 30V.

The following equations calculate output power:

$$P_{OUT} = \eta \bullet V_{IN} \bullet D \bullet I_{SW(MAX)} \bullet 0.5$$

η = Efficiency = ~85%

$$D = \text{Duty Cycle} = \frac{\left(V_{OUT} + V_F\right) \bullet N_{PS}}{\left(V_{OUT} + V_F\right) \bullet N_{PS} + V_{IN}}$$

$I_{SW(MAX)}$ = Maximum switch current limit = 450mA

APPLICATIONS INFORMATION

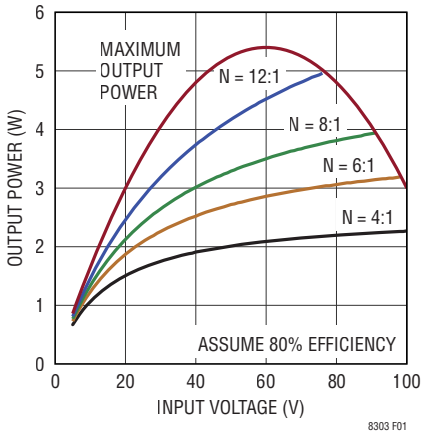


Figure 1. Output Power for 3.3V Output

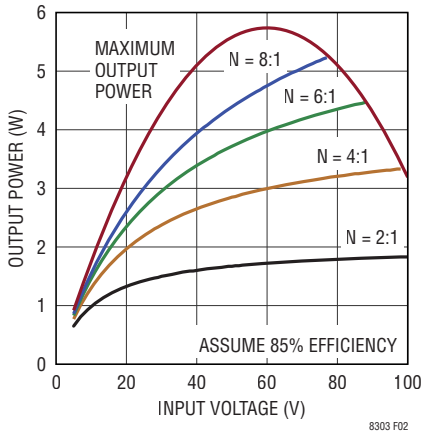


Figure 2. Output Power for 5V Output

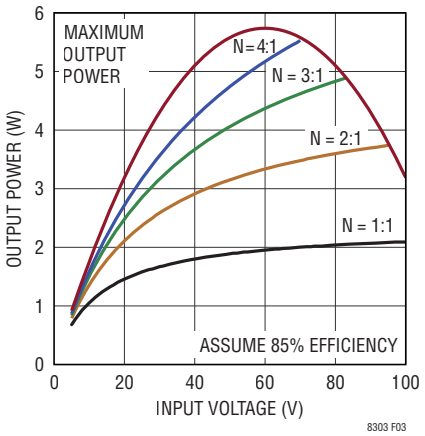


Figure 3. Output Power for 12V Output

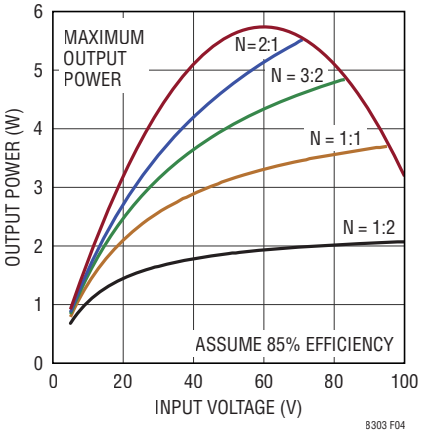


Figure 4. Output Power for 24V Output

Primary Inductance Requirement

The LT8303 obtains output voltage information from the reflected output voltage on the SW pin. The conduction of secondary current reflects the output voltage on the primary SW pin. The sample-and-hold error amplifier needs a minimum 350ns to settle and sample the reflected output voltage. In order to ensure proper sampling, the secondary winding needs to conduct current for a minimum of 350ns. The following equation gives the minimum value for primary-side magnetizing inductance:

$$L_{PRI} \geq \frac{t_{OFF(MIN)} \bullet N_{PS} \bullet \left(V_{OUT} + V_F\right)}{I_{SW(MIN)}}$$

$t_{OFF(MIN)}$ = Minimum switch-off time = 350ns

$I_{SW(MIN)}$ = Minimum switch current limit = 105mA

In addition to the primary inductance requirement for the minimum switch-off time, the LT8303 has minimum switch-on time that prevents the chip from turning on the power switch shorter than approximately 160ns. This minimum switch-on time is mainly for leading-edge blanking the initial switch turn-on current spike. If the inductor current exceeds the desired current limit during that time, oscillation may occur at the output as the current control loop will lose its ability to regulate. Therefore, the following equation relating to maximum input voltage must also be followed in selecting primary-side magnetizing inductance:

$$L_{PRI} \geq \frac{t_{ON(MIN)} \bullet V_{IN(MAX)}}{I_{SW(MIN)}}$$

$t_{ON(MIN)}$ = Minimum Switch-On Time = 160ns

APPLICATIONS INFORMATION

In general, choose a transformer with its primary magnetizing inductance about 40% to 60% larger than the minimum values calculated above. A transformer with much larger inductance will have a bigger physical size and may cause instability at light load.

Selecting a Transformer

Transformer specification and design is perhaps the most critical part of successfully applying the LT8303. In addition to the usual list of guidelines dealing with high frequency isolated power supply transformer design, the following information should be carefully considered.

Linear Technology has worked with several leading magnetic component manufacturers to produce pre-designed flyback transformers for use with the LT8303. Table 1 shows the details of these transformers.

Turns Ratio

Note that when choosing the R_{FB} resistor to set output voltage, the user has relative freedom in selecting a transformer turns ratio to suit a given application. In contrast, the use of simple ratios of small integers, e.g., 4:1, 2:1, 1:1, provides more freedom in settling total turns and mutual inductance.

Table 1. Predesigned Transformers – Typical Specifications

TRANSFORMER PART NUMBER	DIMENSION (W × L × H) (mm)	L_{PRI}, µH TYP	L_{LKG}, µH TYP (MAX)	N_P: N_S	VENDOR	TARGET APPLICATION		
						V_{IN} (V)	V_{OUT} (V)	I_{OUT} (A)
750315825	13.36 × 10.16 × 8.64	150	3 (6)	8:1	Wurth Elektronik	36 to 75	3.3	0.9
750315826	13.36 × 10.16 × 8.64	150	2 (4)	6:1	Wurth Elektronik	36 to 75	5	0.65
750315827	13.36 × 10.16 × 8.65	150	1.8 (3.6)	4:1	Wurth Elektronik	36 to 75	5	0.5
750315828	13.36 × 10.16 × 8.66	150	1.6 (3.2)	2:1	Wurth Elektronik	36 to 75	12	0.25
750315829	13.36 × 10.16 × 8.67	150	1.5 (3)	1:1	Wurth Elektronik	36 to 75	24	0.12
750315830	13.36 × 10.16 × 8.68	150	1.9 (3.8)	1:2	Wurth Elektronik	36 to 75	48	0.06
750315833	13.36 × 10.16 × 8.71	150	1.5 (3)	2:1:1	Wurth Elektronik	36 to 75	12/12	0.12/0.12
750315834	13.36 × 10.16 × 8.72	150	2.6 (5.2)	6:1:1	Wurth Elektronik	36 to 75	5/5	0.32/0.32
PS15-108	14 × 10 × 9.2	150	(5)	8:1	Sumida	36 to 75	3.3	0.9
PS15-109	14 × 10 × 9.2	150	(5)	6:1	Sumida	36 to 75	5	0.65
PS15-110	14 × 10 × 9.2	150	(5)	4:1	Sumida	36 to 75	5	0.5
PS15-111	14 × 10 × 9.2	150	(5)	2:1	Sumida	36 to 75	12	0.25
PS15-112	14 × 10 × 9.2	150	(5)	1:1	Sumida	36 to 75	24	0.12
PS15-113	14 × 10 × 9.2	150	(5)	1:2	Sumida	36 to 75	48	0.06

APPLICATIONS INFORMATION

Typically, choose the transformer turns ratio to maximize available output power. For low output voltages (3.3V or 5V), a larger N:1 turns ratio can be used with multiple primary windings relative to the secondary to maximize the transformer's current gain (and output power). However, remember that the SW pin sees a voltage that is equal to the maximum input supply voltage plus the output voltage multiplied by the turns ratio. In addition, leakage inductance will cause a voltage spike ($V_{LEAKAGE}$) on top of this reflected voltage. This total quantity needs to remain below the 150V absolute maximum rating of the SW pin to prevent breakdown of the internal power switch. Together these conditions place an upper limit on the turns ratio, N_{PS}, for a given application. Choose a turns ratio low enough to ensure:

$$N_{PS} < \frac{150V - V_{IN(MAX)} - V_{LEAKAGE}}{V_{OUT} + V_F}$$

For lower output power levels, choose a smaller N:1 turns ratio to alleviate the SW pin voltage stress. Although a 1:N turns ratio makes it possible to have very high output voltages without exceeding the breakdown voltage of the internal power switch, the multiplied parasitic capacitance through turns ratio coupled with the relatively resistive 150V internal power switch may cause the switch turn-on current spike ringing beyond 160ns leading-edge blanking, thereby producing light load instability in certain applications. So any 1:N turns ratio should be fully evaluated before its use with the LT8303.

The turns ratio is an important element in the isolated feedback scheme, and directly affects the output voltage accuracy. Make sure the transformer manufacturer specifies turns ratio accuracy within ±1%.

Saturation Current

The current in the transformer windings should not exceed its rated saturation current. Energy injected once the core is saturated will not be transferred to the secondary and will instead be dissipated in the core. When designing custom transformers to be used with the LT8303, the saturation current should always be specified by the transformer manufacturers.

Winding Resistance

Resistance in either the primary or secondary windings will reduce overall power efficiency. Good output voltage regulation will be maintained independent of winding resistance due to the boundary/discontinuous conduction mode operation of the LT8303.

Leakage Inductance and Snubbers

Transformer leakage inductance on either the primary or secondary causes a voltage spike to appear on the primary after the power switch turns off. This spike is increasingly prominent at higher load currents where more stored energy must be dissipated. It is very important to minimize transformer leakage inductance.

When designing an application, adequate margin should be kept for the worst-case leakage voltage spikes even under overload conditions. In most cases shown in Figure 5, the reflected output voltage on the primary plus V_{IN} should be kept below 120V. This leaves at least 30V margin for the leakage spike across line and load conditions. A larger voltage margin will be required for poorly wound transformers or for excessive leakage inductance.

In addition to the voltage spikes, the leakage inductance also causes the SW pin ringing for a while after the power switch turns off. To prevent the voltage ringing falsely trigger boundary mode detector, the LT8303 internally blanks the boundary mode detector for approximately 250ns. Any remaining voltage ringing after 250ns may turn the power switch back on again before the secondary current falls to zero. So the leakage inductance spike ringing should be limited to less than 250ns.

APPLICATIONS INFORMATION

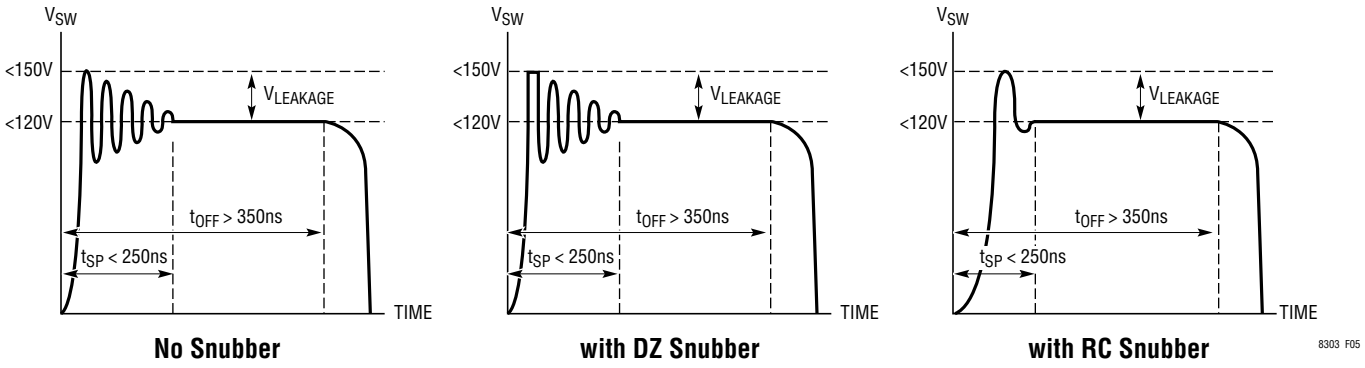


Figure 5. Maximum Voltages for SW Pin Flyback Waveform

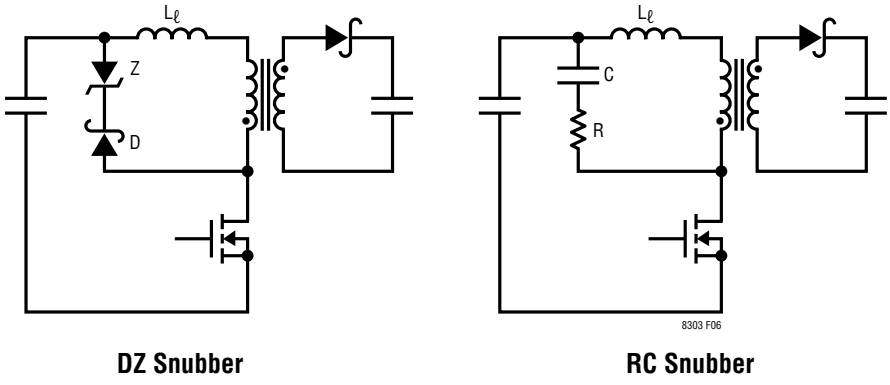


Figure 6. Snubber Circuits

A snubber circuit is recommended for most applications. Two types of snubber circuits shown in Figure 6 that can protect the internal power switch include the DZ (diode-Zener) snubber and the RC (resistor-capacitor) snubber. The DZ snubber ensures well defined and consistent clamping voltage and has slightly higher power efficiency, while the RC snubber quickly damps the voltage spike ringing and provides better load regulation and EMI performance. Figure 5 shows the flyback waveforms with the DZ and RC snubbers.

For the DZ snubber, proper care must be taken when choosing both the diode and the Zener diode. Schottky diodes are typically the best choice, but some PN diodes can be used if they turn on fast enough to limit the leakage inductance spike. Choose a diode that has a reverse-voltage rating higher than the maximum SW pin voltage.

The Zener diode breakdown voltage should be chosen to balance power loss and switch voltage protection. The best compromise is to choose the largest voltage breakdown. Use the following equation to make the proper choice:

$$V_{ZENER(MAX)} \leq 150V - V_{IN(MAX)}$$

For an application with a maximum input voltage of 80V, choose a 62V Zener diode, the $V_{ZENER(MAX)}$ of which is around 65V and below the 70V maximum.

The power loss in the clamp will determine the power rating of the Zener diode. Power loss in the clamp is highest at maximum load and minimum input voltage. The switch current is highest at this point along with the energy stored in the leakage inductance. A 0.5W Zener will satisfy most applications when the highest V_{ZENER} is chosen.

APPLICATIONS INFORMATION

Tables 2 and 3 show some recommended diodes and Zener diodes.

Table 2. Recommended Zener Diodes

PART	V_{ZENER} (V)	POWER (W)	CASE	VENDOR
MMSZ5266BT1G	68	0.5	SOD-123	On Semi
MMSZ5270BT1G	91	0.5	SOD-123	
CMHZ5266B	68	0.5	SOD-123	Central Semiconductor
CMHZ5267B	75	0.5	SOD-123	
BZX84J-68	68	0.5	SOD323F	NXP
BZX100A	100	0.5	SOD323F	

Table 3. Recommended Diodes

PART	I (A)	$V_{REVERSE}$ (V)	CASE	VENDOR
BAV21W	0.625	200	SOD-123	Diodes Inc.
BAV20W	0.625	150	SOD-123	

The recommended approach for designing an RC snubber is to measure the period of the ringing on the SW pin when the power switch turns off without the snubber and then add capacitance (starting with 100pF) until the period of the ringing is 1.5 to 2 times longer. The change in period will determine the value of the parasitic capacitance, from which the parasitic inductance can be determined from the initial period, as well. Once the value of the SW node capacitance and inductance is known, a series resistor can be added to the snubber capacitance to dissipate power and critically dampen the ringing. The equation for deriving the optimal series resistance using the observed periods (t_{PERIOD} and $t_{PERIOD(SNUBBED)}$) and snubber capacitance ($C_{SNUBBER}$) is:

$$C_{PAR} = \frac{C_{SNUBBER}}{\left(\frac{t_{PERIOD(SNUBBED)}}{t_{PERIOD}}\right)^2 - 1}$$

$$L_{PAR} = \frac{t_{PERIOD}^2}{C_{PAR} \bullet 4\pi^2}$$

$$R_{SNUBBER} = \sqrt{\frac{L_{PAR}}{C_{PAR}}}$$

Note that energy absorbed by the RC snubber will be converted to heat and will not be delivered to the load. In high voltage or high current applications, the snubber may need to be sized for thermal dissipation.

Undervoltage Lockout (UVLO)

A resistive divider from V_{IN} to the EN/UVLO pin implements undervoltage lockout (UVLO). The EN/UVLO pin falling threshold is set at 1.223V with 16mV hysteresis. In addition, the EN/UVLO pin sinks 2.5µA when the voltage at the pin is below 1.223V. This current provides user programmable hysteresis based on the value of R1. The programmable UVLO thresholds are:

$$V_{IN(UVLO+)} = \frac{1.239V \bullet (R1 + R2)}{R2} + 2.5\mu A \bullet R1$$

$$V_{IN(UVLO-)} = \frac{1.223V \bullet (R1 + R2)}{R2}$$

Figure 7 shows the implementation of external shutdown control while still using the UVLO function. The NMOS grounds the EN/UVLO pin when turned on, and puts the LT8303 in shutdown with quiescent current less than 2.5µA.

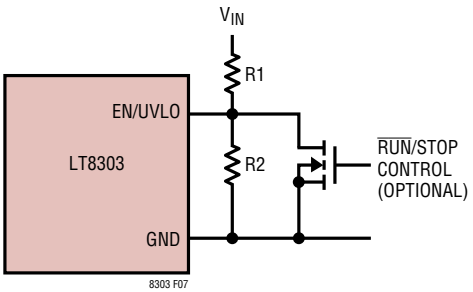


Figure 7. Undervoltage Lockout (UVLO)

APPLICATIONS INFORMATION

Minimum Load Requirement

The LT8303 samples the isolated output voltage from the primary-side flyback pulse waveform. The flyback pulse occurs once the primary switch turns off and the secondary winding conducts current. In order to sample the output voltage, the LT8303 has to turn on and off at least for a minimum amount of time and with a minimum frequency. The LT8303 delivers a minimum amount of energy even during light load conditions to ensure accurate output voltage information. The minimum energy delivery creates a minimum load requirement, which can be approximately estimated as:

$$I_{LOAD(MIN)} = \frac{L_{PRI} \bullet I_{SW(MIN)}^2 \bullet f_{MIN}}{2 \bullet V_{OUT}}$$

L_{PRI} = Transformer primary inductance

$I_{SW(MIN)}$ = Minimum switch current limit = 140mA (Max)

f_{MIN} = Minimum switching frequency = 9kHz (Max)

The LT8303 typically needs less than 0.5% of its full output power as minimum load. Alternatively, a Zener diode with its breakdown of 20% higher than the output voltage can serve as a minimum load if pre-loading is not acceptable. For a 5V output, use a 6V Zener with cathode connected to the output.

Output Short Protection

When the output is heavily overloaded or shorted, the reflected SW pin waveform rings longer than the internal blanking time. After the 350ns minimum switch-off time, the excessive ring falsely trigger the boundary mode detector and turn the power switch back on again before the secondary current falls to zero. Under this condition, the LT8303 runs into continuous conduction mode at 350kHz maximum switching frequency. Depending on the V_{IN} supply voltage, the switch current may run away and exceed 450mA maximum current limit. Once the switch current hits 1A over current limit, a soft-start cycle initiates and throttles back both switch current limit and switch frequency. This output short protection prevents the switch current from running away and limits the average output diode current.

Design Example

Use the following design example as a guide to design applications for the LT8303. The design example involves designing a 12V output with a 200mA load current and an input range from 30V to 80V.

$V_{IN(MIN)}$ = 30V, $V_{IN(NOM)}$ = 48V, $V_{IN(MAX)}$ = 80V, V_{OUT} = 12V, I_{OUT} = 200mA

Step 1: Select the Transformer Turns Ratio.

$$N_{PS} < \frac{150V - V_{IN(MAX)} - V_{LEAKAGE}}{V_{OUT} + V_F}$$

$V_{LEAKAGE}$ = Margin for transformer leakage spike = 30V

V_F = Output diode forward voltage = ~0.3V

Example:

$$N_{PS} < \frac{150V - 80V - 30V}{12V + 0.3V} = 3.3$$

The choice of transformer turns ratio is critical in determining output current capability of the converter. Table 4 shows the switch voltage stress and output current capability at different transformer turns ratio.

Table 4. Switch Voltage Stress and Output Current Capability vs Turns Ratio

N_{PS}	$V_{SW(MAX)}$ at $V_{IN(MAX)}$ (V)	$I_{OUT(MAX)}$ at $V_{IN(MIN)}$ (mA)	DUTY CYCLE (%)
1:1	92.3	139	13 to 29
2:1	104.6	215	24 to 45
3:1	116.9	264	32 to 55

Since both N_{PS} = 2 and N_{PS} = 3 can meet the 200mA output current requirement, N_{PS} = 2 is chosen in this example to allow more margin for transformer leakage inductance voltage spike.

APPLICATIONS INFORMATION

Step 2: Determine the Primary Inductance.

Primary inductance for the transformer must be set above a minimum value to satisfy the minimum switch-off and switch-on time requirements:

$$L_{PRI} \geq \frac{t_{OFF(MIN)} \bullet N_{PS} \bullet \left(V_{OUT} + V_F\right)}{I_{SW(MIN)}}$$

$$L_{PRI} \geq \frac{t_{ON(MIN)} \bullet V_{IN(MAX)}}{I_{SW(MIN)}}$$

$t_{OFF(MIN)}$ = 350ns

$t_{ON(MIN)}$ = 160ns

$I_{SW(MIN)}$ = 105mA

Example:

$$L_{PRI} \geq \frac{350ns \bullet 2 \bullet (12V + 0.3V)}{105mA} = 82\mu H$$

$$L_{PRI} \geq \frac{160ns \bullet 80V}{105mA} = 122\mu H$$

Most transformers specify primary inductance with a tolerance of ±20%. With other component tolerance considered, choose a transformer with its primary inductance 40% to 60% larger than the minimum values calculated above. L_{PRI} = 150µH is then chosen in this example.

The transformer also needs to be rated for the correct saturation current level across line and load conditions. A saturation current rating larger than 620mA is necessary to work with the LT8303. The PS15-111 from Sumida is chosen as the flyback transformer.

Step 3: Choose the Output Diode.

Two main criteria for choosing the output diode include forward current rating and reverse voltage rating. The maximum load requirement is a good first-order guess as the average current requirement for the output diode. A conservative metric is the maximum switch current limit multiplied by the turns ratio,

$$I_{DIODE(MAX)} = I_{SW(MAX)} \bullet N_{PS}$$

Example:

$I_{DIODE(MAX)}$ = 1.07A

Next calculate reverse voltage requirement using maximum V_{IN}:

$$V_{REVERSE} = V_{OUT} + \frac{V_{IN(MAX)}}{N_{PS}}$$

Example:

$$V_{REVERSE} = 12V + \frac{72V}{2} = 48V$$

The DFLS2100 (2A, 100V diode) from Diodes Inc. is chosen.

Step 4: Choose the Output Capacitor.

The output capacitor should be chosen to minimize the output voltage ripple while considering the increase in size and cost of a larger capacitor. Use the equation below to calculate the output capacitance:

$$C_{OUT} = \frac{L_{PRI} \bullet I_{SW}^2}{2 \bullet V_{OUT} \bullet \Delta V_{OUT}}$$

Example:

Design for output voltage ripple less than 1% of V_{OUT}, i.e., 120mV.

$$C_{OUT} = \frac{150\mu H \bullet (0.535A)^2}{2 \bullet 12V \bullet 0.12V} = 14.9\mu F$$

Remember ceramic capacitors lose capacitance with applied voltage. The capacitance can drop to 40% of quoted capacitance at the maximum voltage rating. So a 22µF, 25V rating X5R or X7R ceramic capacitor is chosen.

Step 5: Design Snubber Circuit.

The snubber circuit protects the power switch from leakage inductance voltage spike. A DZ snubber is recommended for this application because of lower leakage inductance and larger voltage margin. The Zener and the diode need to be selected.

APPLICATIONS INFORMATION

The maximum Zener breakdown voltage is set according to the maximum V_{IN}:

$V_{ZENER(MAX)} \leq 150V - V_{IN(MAX)}$

Example:

$V_{ZENER(MAX)} \leq 150V - 80V = 70V$

A 62V Zener with a maximum of 65V will provide optimal protection and minimize power loss. So a 62V, 0.5W Zener from Central Semiconductor (CMHZ5265B) is chosen.

Choose a diode that is fast and has sufficient reverse voltage breakdown:

$V_{REVERSE} > V_{SW(MAX)}$

$V_{SW(MAX)} = V_{IN(MAX)} + V_{ZENER(MAX)}$

Example:

$V_{REVERSE} > 144V$

A 200V, 1A diode from Central Semiconductor (CMMRIU-02) is chosen.

Step 6: Select the R_{FB} Resistor.

Use the following equation to calculate the starting value for R_{FB}:

$$R_{FB} = \frac{N_{PS} \bullet (V_{OUT} + V_F)}{100\mu A}$$

Example:

$$R_{FB} = \frac{2 \bullet (12V + 0.3V)}{100\mu A} = 246k$$

Depending on the tolerance of standard resistor values, the precise resistor value may not exist. For 1% standard values, a 243k resistor in series with a 3.01k resistor should be close enough. As discussed in the Application Information section, the final R_{FB} value should be adjusted on the measured output voltage.

Step 7: Select the EN/UVLO Resistors.

Determine the amount of hysteresis required and calculate R1 resistor value:

$V_{IN(HYS)} = 2.5\mu A \bullet R1$

Example:

Choose 2.5V of hysteresis,

$R1 = 1M$

Determine the UVLO thresholds and calculate R2 resistor value:

$$V_{IN(UVLO+)} = \frac{1.239V \bullet (R1 + R2)}{R2} + 2.5\mu A \bullet R1$$

Example:

Set V_{IN} UVLO rising threshold to 34.5V,

$R2 = 49.9k$

$V_{IN(UVLO+)} = 28.6V$

$V_{IN(UVLO-)} = 25.7V$

Step 8: Ensure minimum load.

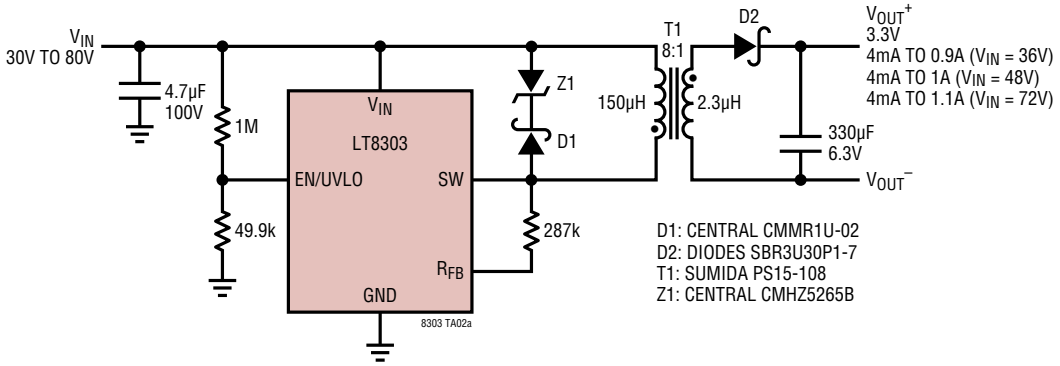
The theoretical minimum load can be approximately estimated as:

$$I_{LOAD(MIN)} = \frac{150\mu H \bullet (140mA)^2 \bullet 9kHz}{2 \bullet 12V} = 1.1mA$$

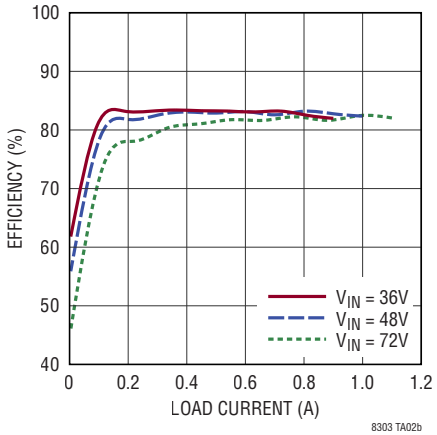
Remember to check the minimum load requirement in real application. The minimum load occurs at the point where the output voltage begins to climb up as the converter delivers more energy than what is consumed at the output. The real minimum load for this application is about 1mA. In this example, a 12.1k resistor is selected as the minimum load.

TYPICAL APPLICATIONS

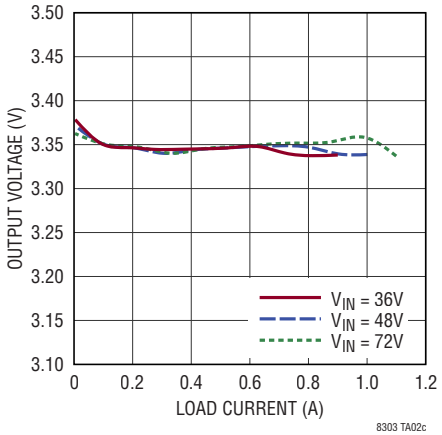
30V to 80V_{IN}, 3.3V_{OUT} Isolated Flyback Converter



Efficiency vs Load Current

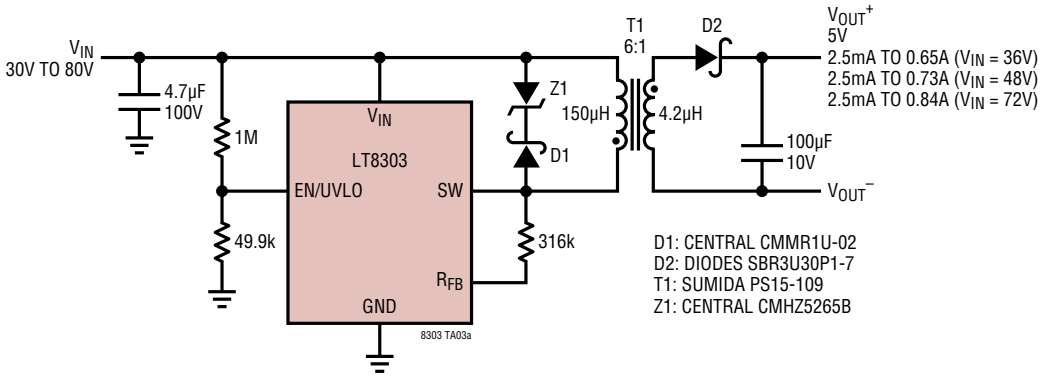


Output Load and Line Regulation

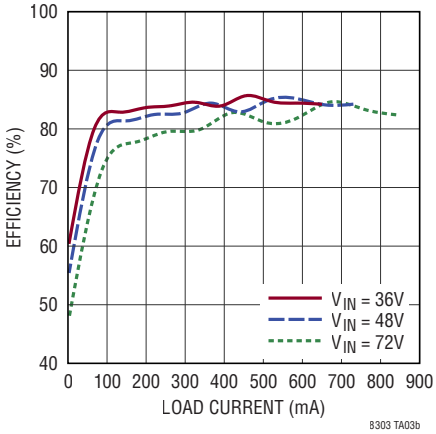


TYPICAL APPLICATIONS

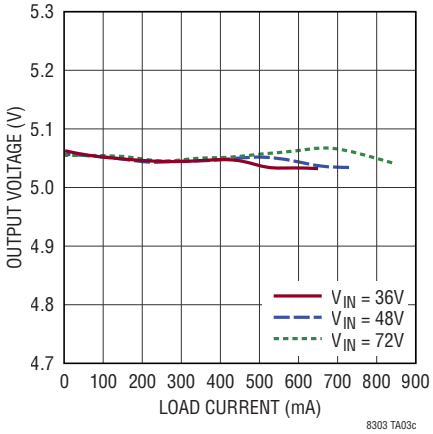
30V to 80V_{IN}, 5V_{OUT} Isolated Flyback Converter



Efficiency vs Load Current

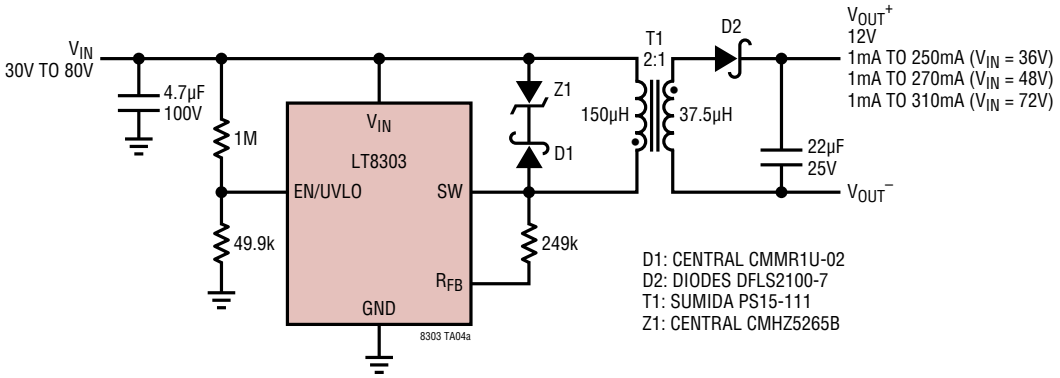


Output Load and Line Regulation

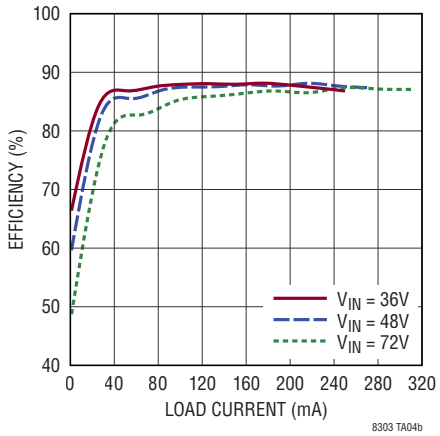


TYPICAL APPLICATIONS

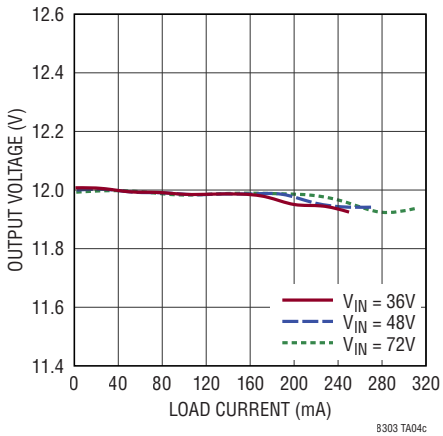
30V to 80V_{IN}, 12V_{OUT} Isolated Flyback Converter



Efficiency vs Load Current

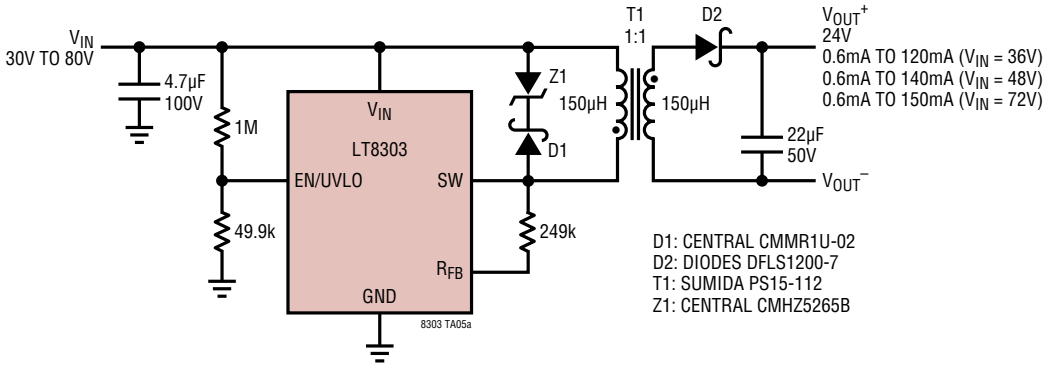


Output Load and Line Regulation



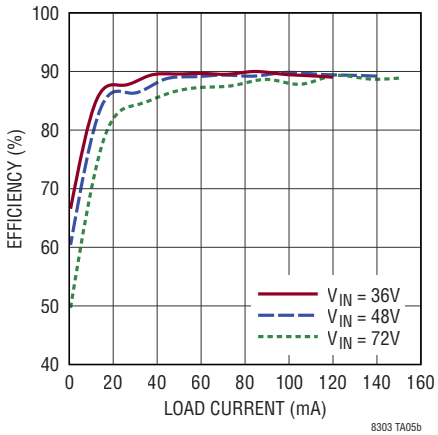
TYPICAL APPLICATIONS

30V to 80V_{IN}, 24V_{OUT} Isolated Flyback Converter

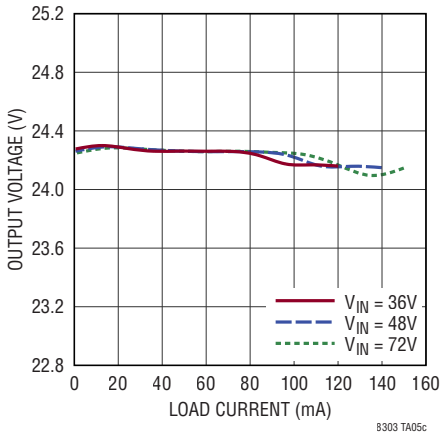


D1: CENTRAL CMMR1U-02
D2: DIODES DFLS1200-7
T1: SUMIDA PS15-112
Z1: CENTRAL CMHZ5265B

Efficiency vs Load Current



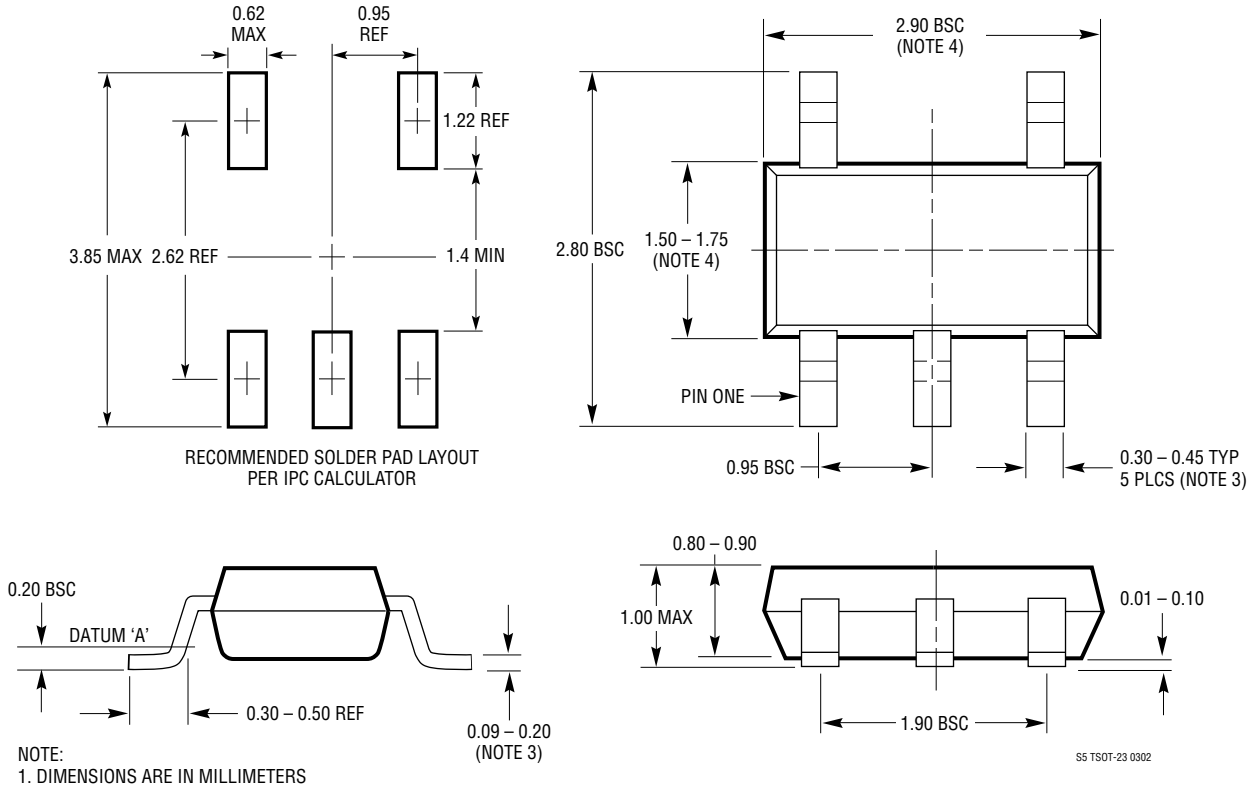
Output Load and Line Regulation



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT8303#packaging for the most recent package drawings.

S5 Package
5-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1635)



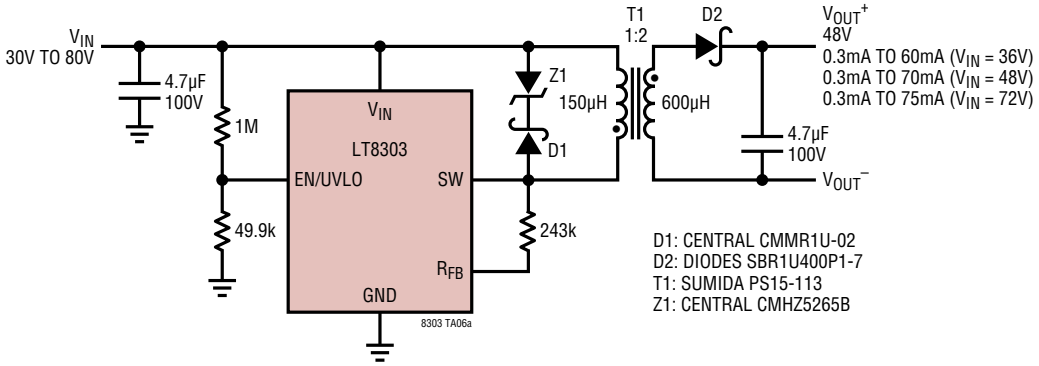
NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

REVISION HISTORY

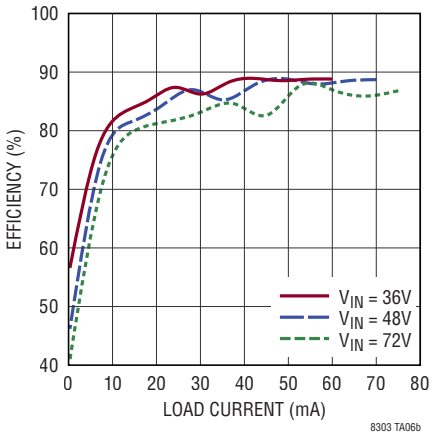
REV	DATE	DESCRIPTION	PAGE NUMBER
A	1/17	Added H-grade version	2, 3

TYPICAL APPLICATION

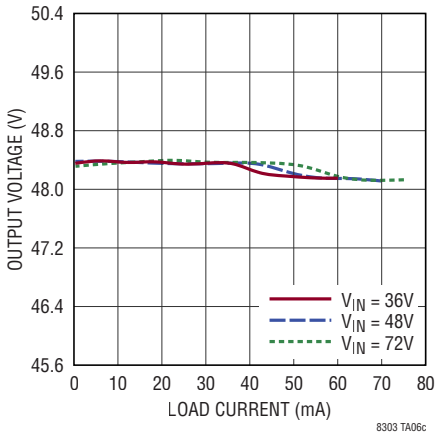
30V to 80V_{IN}, 48V_{OUT} Isolated Flyback Converter



Efficiency vs Load Current



Output Load and Line Regulation



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT8300	100V_{IN} Micropower Isolated Flyback Converter with 150V/260mA Switch	Low I_Q Monolithic No-Opto Flyback, 5-Lead TSOT-23
LT8304	100V_{IN} Micropower Isolated Flyback Converter with 150V/2A Switch	Low I_Q Monolithic No-Opto Flyback, 8-Lead SO-8E
LT8301	42V_{IN} Micropower Isolated Flyback Converter with 65V/1.2A Switch	Low I_Q Monolithic No-Opto Flyback, 5-Lead TSOT-23
LT8302	42V_{IN} Micropower Isolated Flyback Converter with 65V/3.6mA Switch	Low I_Q Monolithic No-Opto Flyback, 8-Lead SO-8E
LT8309	Secondary-Side Synchronous Rectifier Driver	4.5V ≤ V_{CC} ≤ 40V, Fast Turn-On and Turn-Off, 5-Lead TSOT-23
LT3748	100V Isolated Flyback Controller	5V ≤ V_{IN} ≤ 100V, No-Opto Flyback, MSOP-16(12)
LT3798	Off-Line Isolated No-Opto Flyback Controller with Active PFC	V_{IN} and V_{OUT} Limited Only by External Components
LT3757/LT3759/ LT3758	40V/100V Flyback/Boost Controller	Universal Controllers with Small Package and Powerful Gate Drive
LT3957/LT3958	40V/80V Boost/Flyback Converter	Monolithic with Integrated 5A/3.3A Switch
LTC3803/LTC3803-3/ LTC3803-5	200kHz/300kHz Flyback Controller in SOT-23	V_{IN} and V_{OUT} Limited Only by External Components
LTC3805/LTC3805-5	Adjustable Frequency Flyback Controllers	V_{IN} and V_{OUT} Limited Only by External Components