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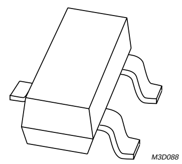


BSH111

N-channel enhancement mode field-effect transistor

Rev. 02 — 26 April 2002 **Product data**

1. Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

Product availability:

BSH111 in SOT23.

2. Features

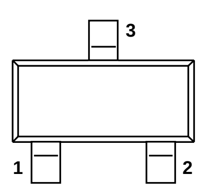
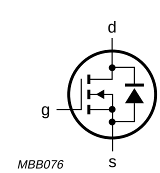
- TrenchMOS™ technology
- Very fast switching
- Low threshold voltage
- Subminiature surface mount package.

3. Applications

- Battery management
- High speed switch
- Logic level translator.

4. Pinning information

Table 1: Pinning - SOT23, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	 **SOT23**	
2	source (s)		
3	drain (d)		

5. Quick reference data

Table 2: Quick reference data

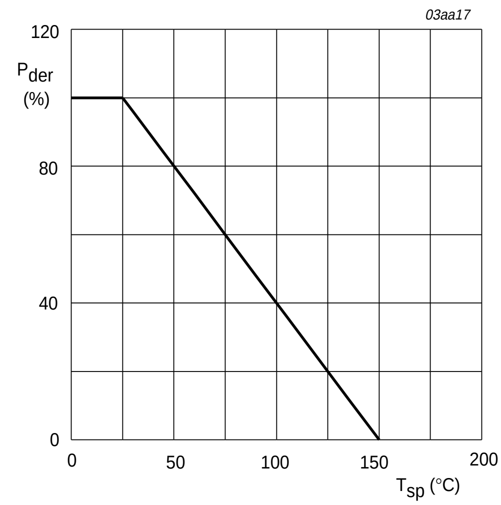
Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	25 °C ≤ T_j ≤ 150 °C	-	55	V
I_D	drain current (DC)	T_{sp} = 25 °C; V_{GS} = 4.5 V	-	335	mA
P_{tot}	total power dissipation	T_{sp} = 25 °C	-	0.83	W
T_j	junction temperature		-	150	°C
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 500 mA	2.3	4.0	Ω
		V_{GS} = 2.5 V; I_D = 75 mA	2.4	5.0	Ω
		V_{GS} = 1.8 V; I_D = 75 mA	3.1	8.0	Ω

6. Limiting values

Table 3: Limiting values

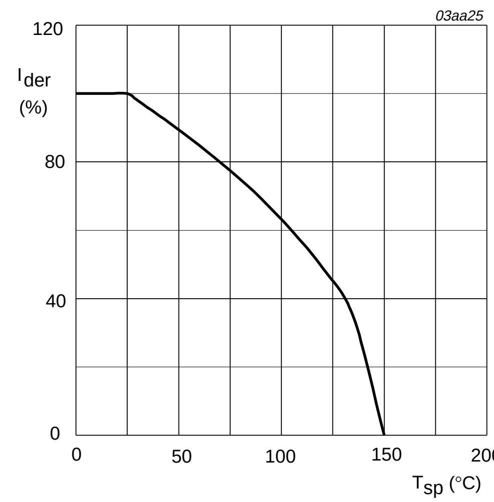
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	25 °C ≤ T_j ≤ 150 °C	-	55	V
V_{DGR}	drain-gate voltage (DC)	25 °C ≤ T_j ≤ 150 °C; R_{GS} = 20 kΩ	-	55	V
V_{GS}	gate-source voltage		-	±10	V
I_D	drain current (DC)	T_{sp} = 25 °C; V_{GS} = 4.5 V; Figure 2 and 3	-	335	mA
		T_{sp} = 100 °C; V_{GS} = 4.5 V; Figure 2	-	212	mA
I_{DM}	peak drain current	T_{sp} = 25 °C; pulsed; t_p ≤ 10 µs; Figure 3	-	1.3	A
P_{tot}	total power dissipation	T_{sp} = 25 °C; Figure 1	-	0.83	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–65	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	T_{sp} = 25 °C	-	335	mA
I_{SM}	peak source (diode forward) current	T_{sp} = 25 °C; pulsed; t_p ≤ 10 µs	-	1.3	A



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

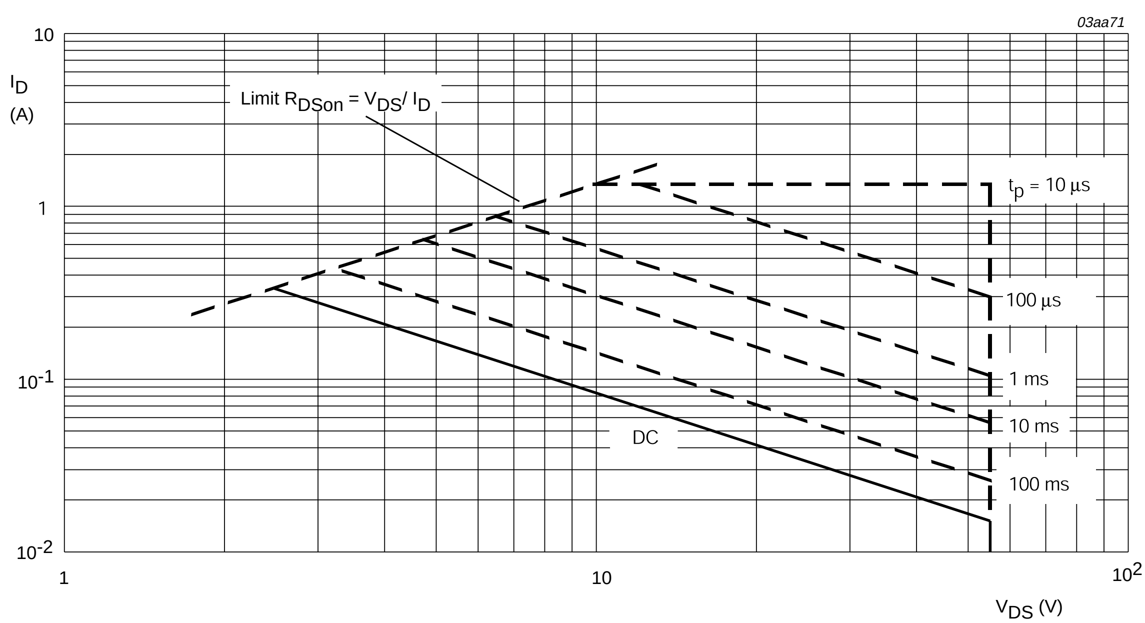
Fig 1. Normalized total power dissipation as a function of solder point temperature.



$V_{GS} \geq 4.5$ V

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



T_{sp} = 25 °C; I_{DM} is single pulse.

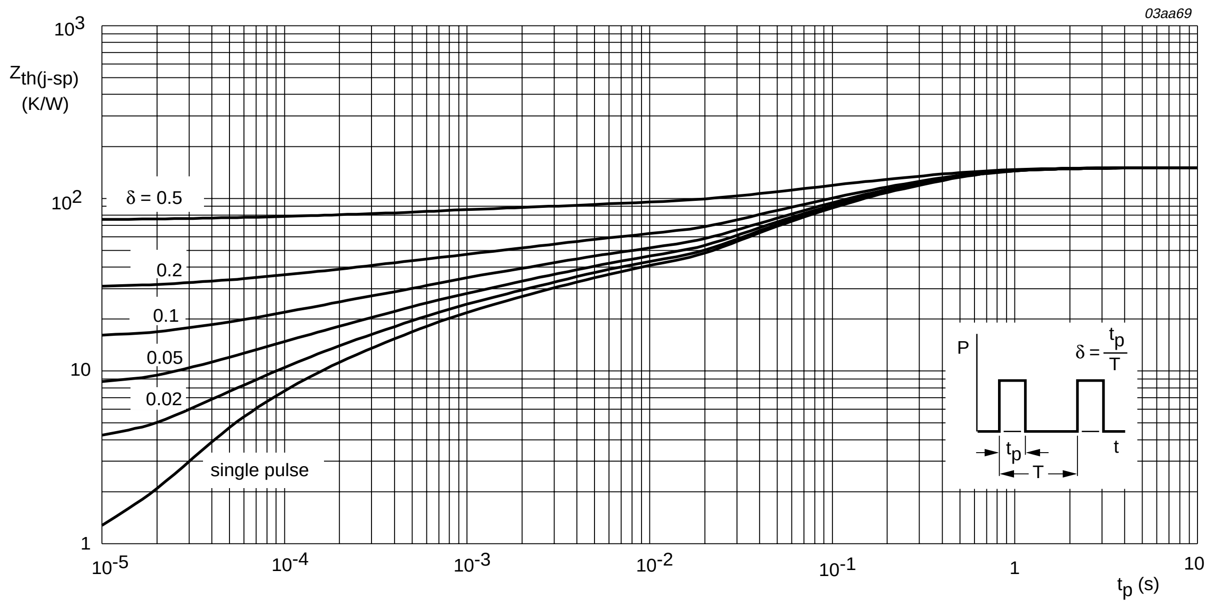
Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	mounted on metal clad substrate; Figure 4	-	-	150	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on printed circuit board	-	350	-	K/W

7.1 Transient thermal impedance



Mounted on metal clad substrate.

Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration.

8. Characteristics

Table 5: Characteristics

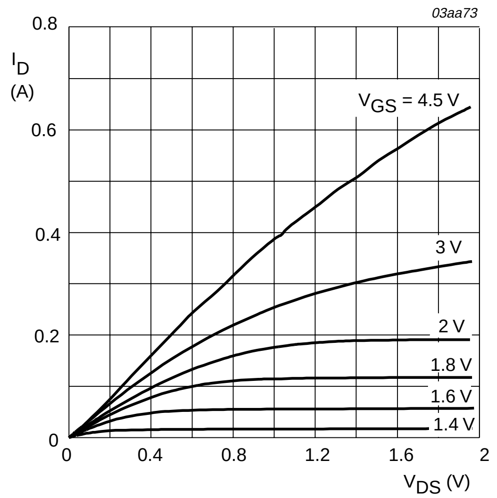
T_j = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 µA; V_{GS} = 0 V				
		T_j = 25 °C	55	75	-	V
		T_j = –55 °C	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 9				
		T_j = 25 °C	0.4	1.0	1.3	V
		T_j = 150 °C	0.3	-	-	V
		T_j = –55 °C	-	-	2.5	V
I_{DSS}	drain-source leakage current	V_{DS} = 44 V; V_{GS} = 0 V				
		T_j = 25 °C	-	0.01	1.0	µA
		T_j = 150 °C	-	-	10	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±8 V; V_{DS} = 0 V	-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 2.5 V; I_D = 75 mA; Figure 7 and 8				
		T_j = 25 °C	-	2.4	5	Ω
		T_j = 150 °C	-	-	7.4	Ω
		V_{GS} = 4.5 V; I_D = 500 mA; Figure 7 and 8				
		T_j = 25 °C	-	2.3	4	Ω
		V_{GS} = 1.8 V; I_D = 75 mA; Figure 7 and 8				
		T_j = 25 °C	-	3.1	8	Ω
Dynamic characteristics						
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 200 mA; Figure 11	100	380	-	mS
$Q_{g(tot)}$	total gate charge	I_D = 0.5 A; V_{DS} = 44 V; V_{GS} = 8 V; Figure 14	-	1.0	-	nC
Q_{gs}	gate-source charge		-	0.05	-	nC
Q_{gd}	gate-drain (Miller) charge		-	0.5	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 10 V; f = 1 MHz; Figure 12	-	17	40	pF
C_{oss}	output capacitance		-	7	30	pF
C_{rss}	reverse transfer capacitance		-	4	10	pF
t_{on}	turn-on time	V_{DD} = 50 V; R_D = 250 Ω; V_{GS} = 10 V; R_G = 50 Ω; R_{GS} = 50 Ω	-	4	10	ns
t_{off}	turn-off time		-	11	15	ns

Table 5: Characteristics...*continued*

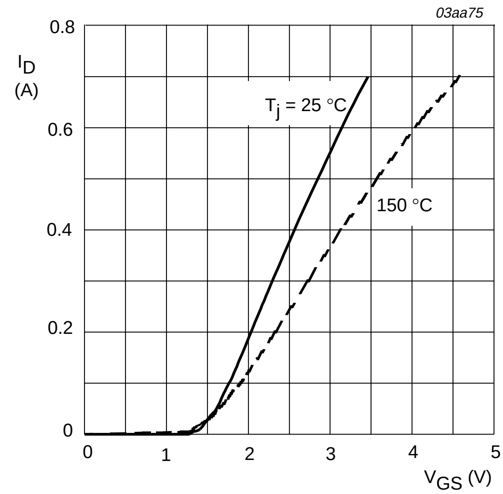
T_j = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 300 mA; V_{GS} = 0 V; Figure 13	-	0.95	1.5	V
t_{rr}	reverse recovery time	I_S = 300 mA; dI_S/dt = –100 A/µs; V_{GS} = 0 V; V_{DS} = 25 V	-	30	-	ns
Q_r	recovered charge		-	30	-	nC



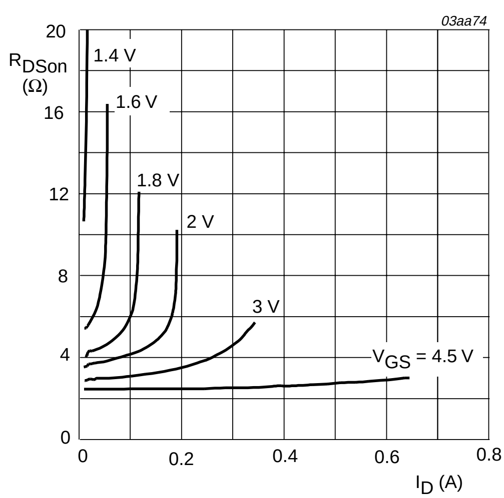
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



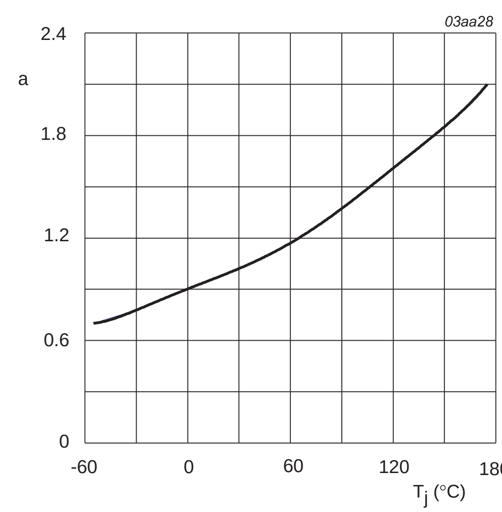
T_j = 25 °C and 150 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



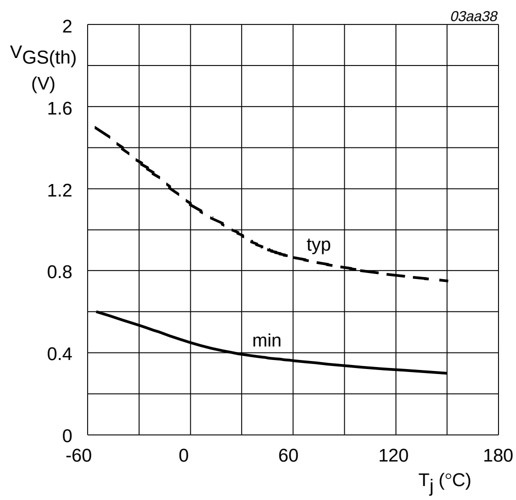
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



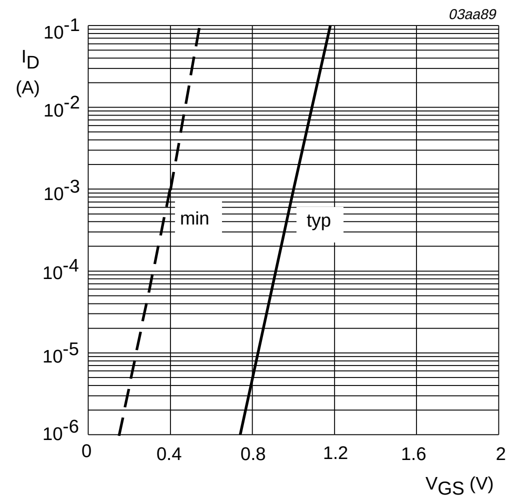
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



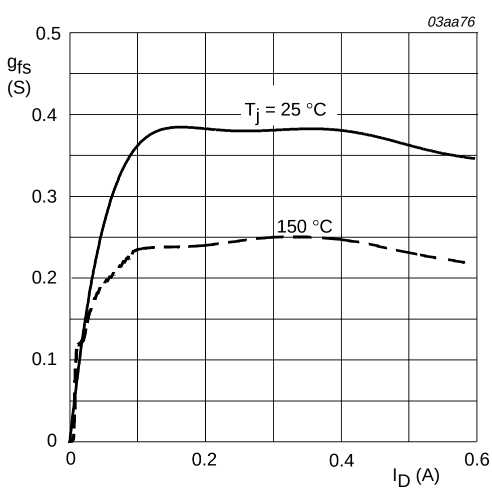
I_D = 1 mA; V_{DS} = V_{GS}

Fig 9. Gate-source threshold voltage as a function of junction temperature.



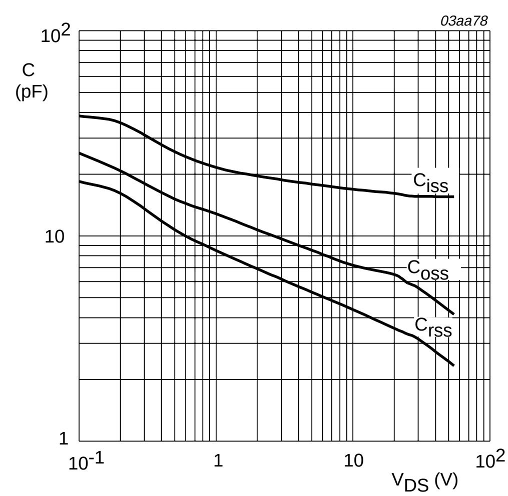
T_j = 25 °C; V_{DS} = 5 V

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



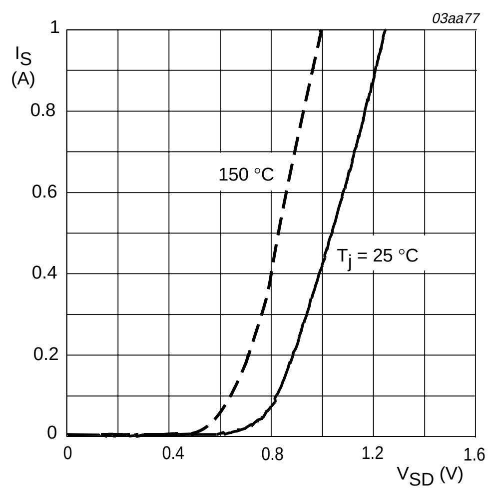
T_j = 25 °C and 150 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 11. Forward transconductance as a function of drain current; typical values.



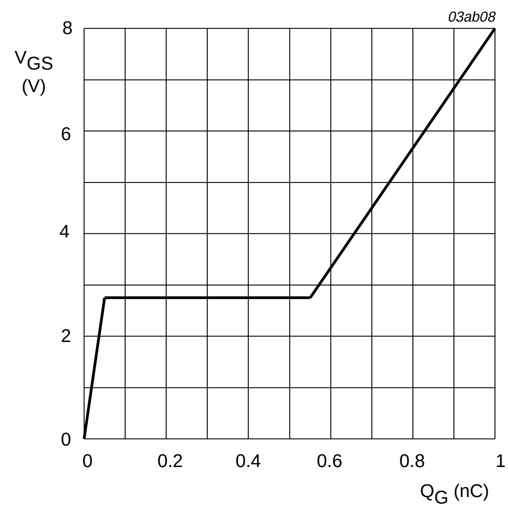
V_{GS} = 0 V; f = 1 MHz

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



T_j = 25 °C and 150 °C; V_{GS} = 0 V

Fig 13. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

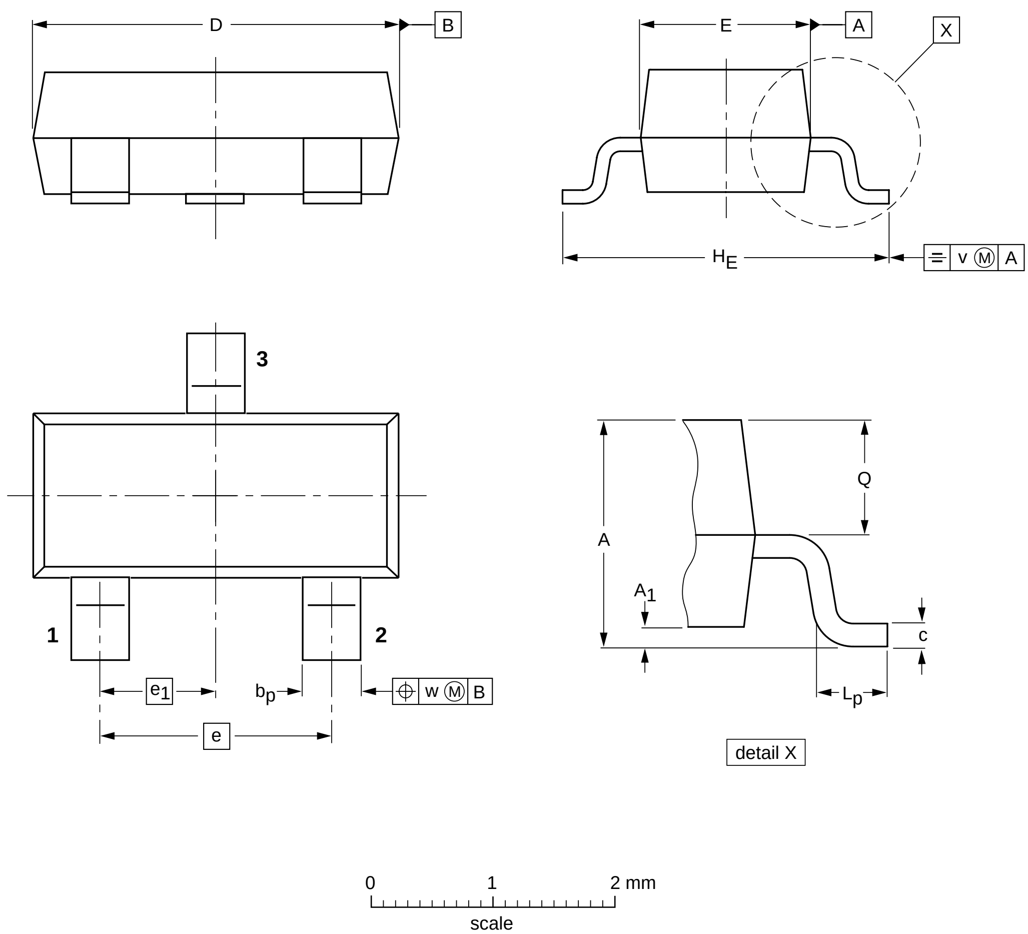


I_D = 0.5 A; V_{DS} = 44 V

Fig 14. Gate-source voltage as a function of gate charge; typical values.

9. Package outline

Plastic surface mounted package; 3 leads **SOT23**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max.	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT23		TO-236AB				~~97-02-28~~ 99-09-13

Fig 15. SOT23.

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
02	**20020426**	**-**	**Product data (9397 750 09629)** Modifications • V_{GS} data updated.
01	**20000807**	**-**	**Product specification; initial version.**

11. Data sheet status

Data sheet status[1]	Product status[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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