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FQS4903

N-Channel QFET® MOSFET

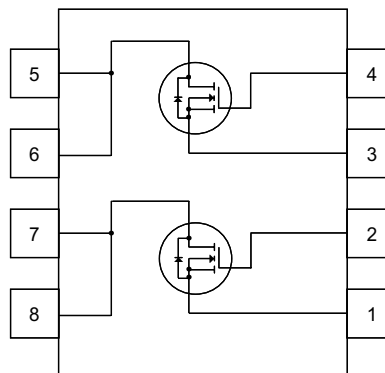
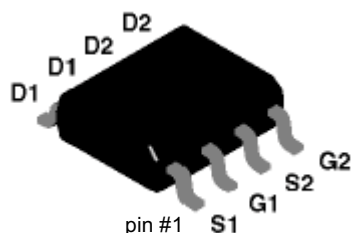
500 V, 0.37 A, 6.2 Ω

Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor®'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 0.37 A, 500 V, $R_{DS(on)}=6.2 \Omega(\text{Max.})@V_{GS}=10 \text{ V}, I_D=0.185 \text{ A}$
- Low Gate Charge (Typ. 6.3 nC)
- Low C_{rss} (Typ. 4.5 pF)
- 100% Avalanche Tested



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | FQS4903 | Unit |
|----------------|---|-------------|------------------|
| V_{DSS} | Drain-Source Voltage | 500 | V |
| I_D | Drain Current - Continuous ($T_A = 25^\circ\text{C}$) | 0.37 | A |
| | | 0.234 | A |
| I_{DM} | Drain Current - Pulsed (Note 1) | 1.48 | A |
| V_{GSS} | Gate-Source Voltage | ± 25 | V |
| dv/dt | Peak Diode Recovery dv/dt (Note 3) | 4.5 | V/ns |
| P_D | Power Dissipation ($T_A = 25^\circ\text{C}$) | 2.0 | W |
| | | 1.3 | W |
| T_J, T_{STG} | Operating and Storage Temperature Range | -55 to +150 | $^\circ\text{C}$ |

Thermal Characteristics

| Symbol | Parameter | Typ | Max | Unit |
|-----------------|---|-----|------|--------------------|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | -- | 62.5 | $^\circ\text{C/W}$ |

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|--------|-----------|-----------------|-----|-----|-----|------|
|--------|-----------|-----------------|-----|-----|-----|------|

Off Characteristics

| | | | | | | |
|--------------------------------------|---|---|-----|------|------|---------------------------|
| BV_{DSS} | Drain-Source Breakdown Voltage | $V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$ | 500 | -- | -- | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D = 250\ \mu\text{A}$, Referenced to 25°C | -- | 0.49 | -- | $\text{V}/^\circ\text{C}$ |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$ | -- | -- | 1 | μA |
| | | $V_{DS} = 400\text{ V}, T_C = 125^\circ\text{C}$ | -- | -- | 10 | μA |
| I_{GSSF} | Gate-Body Leakage Current, Forward | $V_{GS} = 25\text{ V}, V_{DS} = 0\text{ V}$ | -- | -- | 100 | nA |
| I_{GSSR} | Gate-Body Leakage Current, Reverse | $V_{GS} = -25\text{ V}, V_{DS} = 0\text{ V}$ | -- | -- | -100 | nA |

On Characteristics

| | | | | | | |
|--------------|-----------------------------------|---|-----|------|-----|----------|
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$ | 2.0 | -- | 4.0 | V |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS} = 10\text{ V}, I_D = 0.185\text{ A}$ | -- | 4.7 | 6.2 | Ω |
| g_{FS} | Forward Transconductance | $V_{DS} = 35\text{ V}, I_D = 0.185\text{ A}$ (Note 3) | -- | 0.13 | -- | S |

Dynamic Characteristics

| | | | | | | |
|-----------|------------------------------|--|----|-----|-----|----|
| C_{iss} | Input Capacitance | $V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$ | -- | 155 | 200 | pF |
| C_{oss} | Output Capacitance | | -- | 25 | 35 | pF |
| C_{rss} | Reverse Transfer Capacitance | | -- | 4.5 | 6.0 | pF |

Switching Characteristics

| | | | | | | |
|--------------|---------------------|---|------------|------|------|-----|
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD} = 250\text{ V}, I_D = 0.37\text{ A},$ $R_G = 25\ \Omega$ | -- | 5.5 | 20 | ns |
| t_r | Turn-On Rise Time | | -- | 20 | 50 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | -- | 20 | 50 | ns |
| t_f | Turn-Off Fall Time | | (Note 3,4) | -- | 45 | 100 |
| Q_g | Total Gate Charge | $V_{DS} = 400\text{ V}, I_D = 0.37\text{ A},$ $V_{GS} = 10\text{ V}$ | -- | 6.3 | 8.2 | nC |
| Q_{gs} | Gate-Source Charge | | -- | 0.56 | -- | nC |
| Q_{gd} | Gate-Drain Charge | | (Note 3,4) | -- | 3.63 | -- |

Drain-Source Diode Characteristics and Maximum Ratings

| | | | | | | |
|----------|---|---|----------|------|-------|----|
| I_S | Maximum Continuous Drain-Source Diode Forward Current | -- | -- | 0.37 | A | |
| I_{SM} | Maximum Pulsed Drain-Source Diode Forward Current | -- | -- | 1.48 | A | |
| V_{SD} | Drain-Source Diode Forward Voltage | $V_{GS} = 0\text{ V}, I_S = 0.37\text{ A}$ | -- | -- | 1.4 | V |
| t_{rr} | Reverse Recovery Time | $V_{GS} = 0\text{ V}, I_S = 0.37\text{ A},$ $di_F / dt = 100\text{ A}/\mu\text{s}$ | -- | 100 | -- | ns |
| Q_{rr} | Reverse Recovery Charge | | (Note 3) | -- | 0.175 | -- |

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $I_{SD} \leq 0.37\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 0.37\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\ \mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

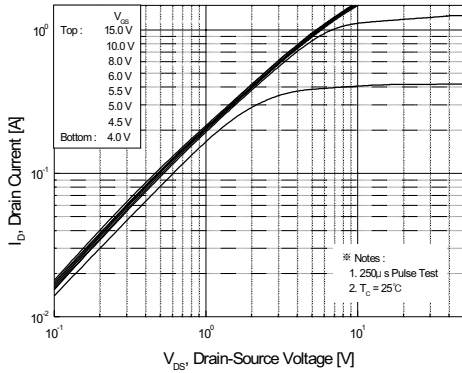


Figure 1. On-Region Characteristics

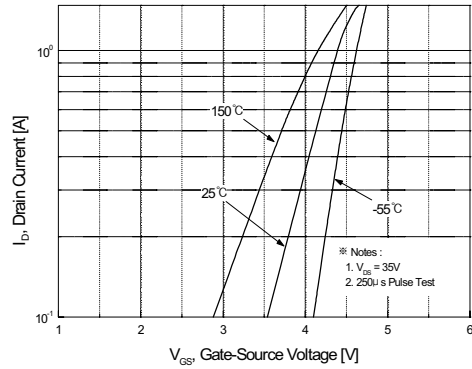


Figure 2. Transfer Characteristics

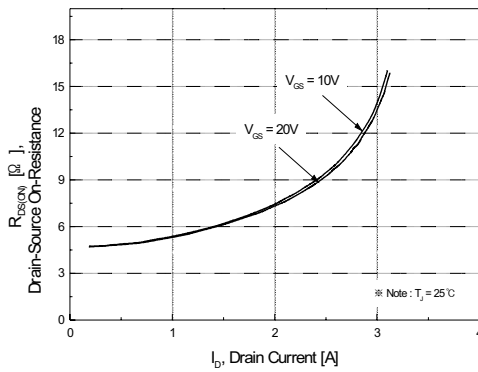


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

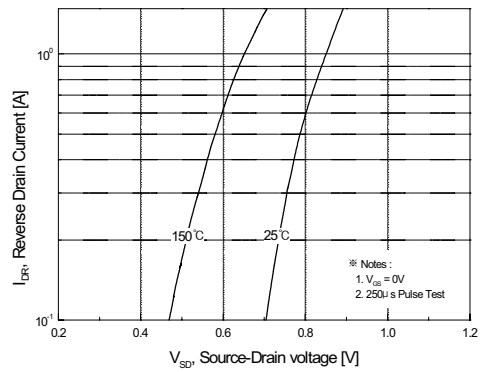


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

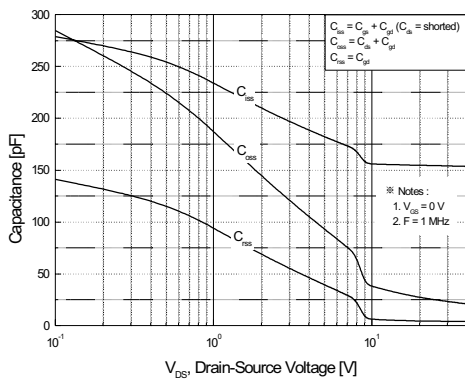


Figure 5. Capacitance Characteristics

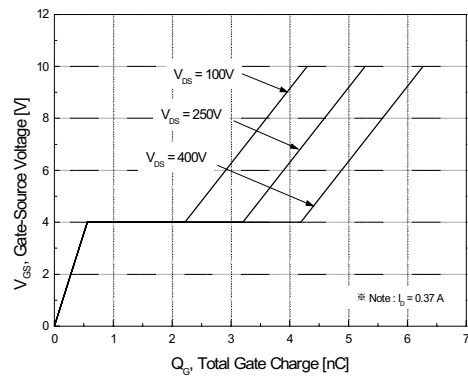


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

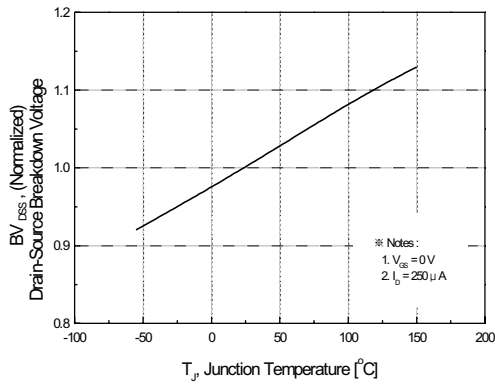


Figure 7. Breakdown Voltage Variation vs. Temperature

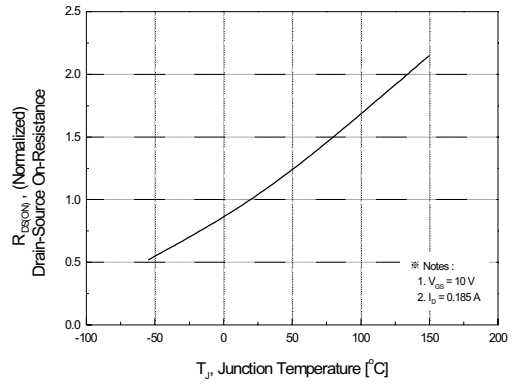


Figure 8. On-Resistance Variation vs. Temperature

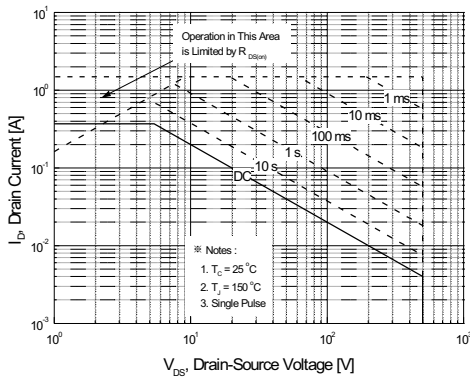


Figure 9. Maximum Safe Operating Area

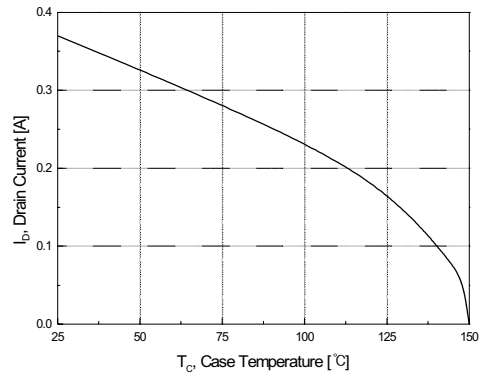


Figure 10. Maximum Drain Current vs. Case Temperature

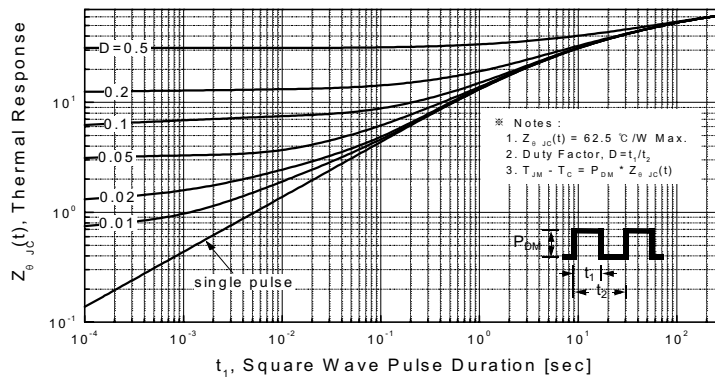
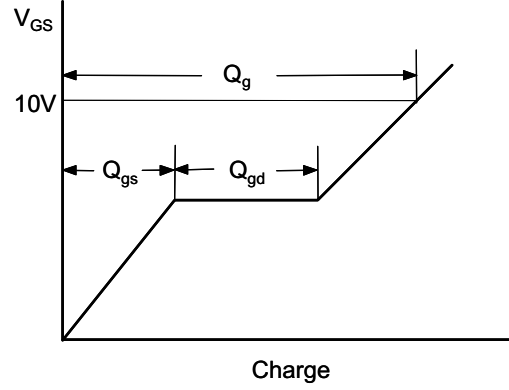
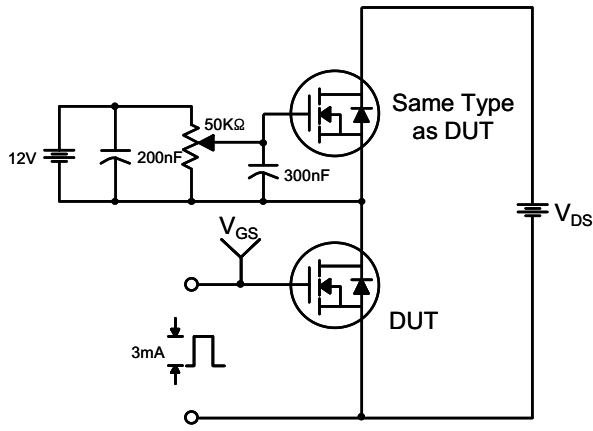
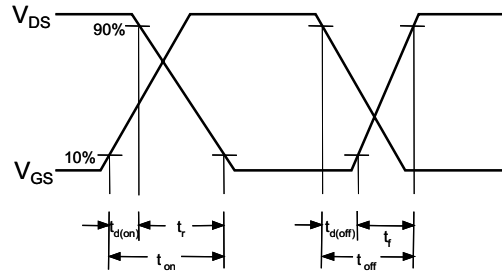
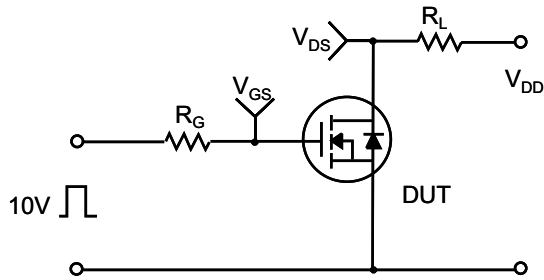


Figure 11. Transient Thermal Response Curve

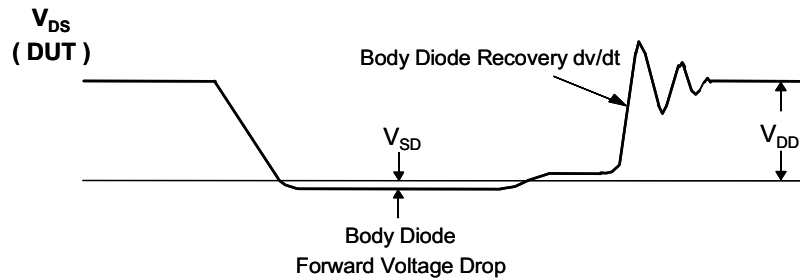
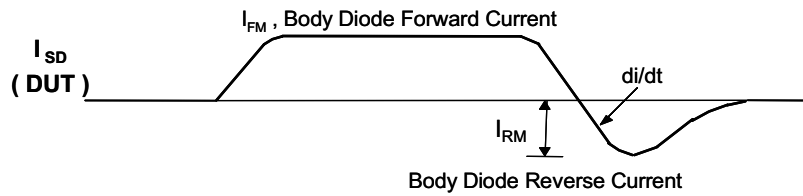
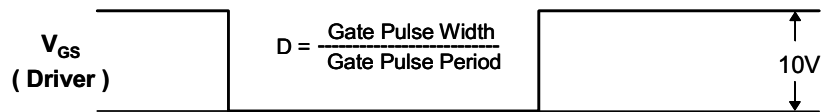
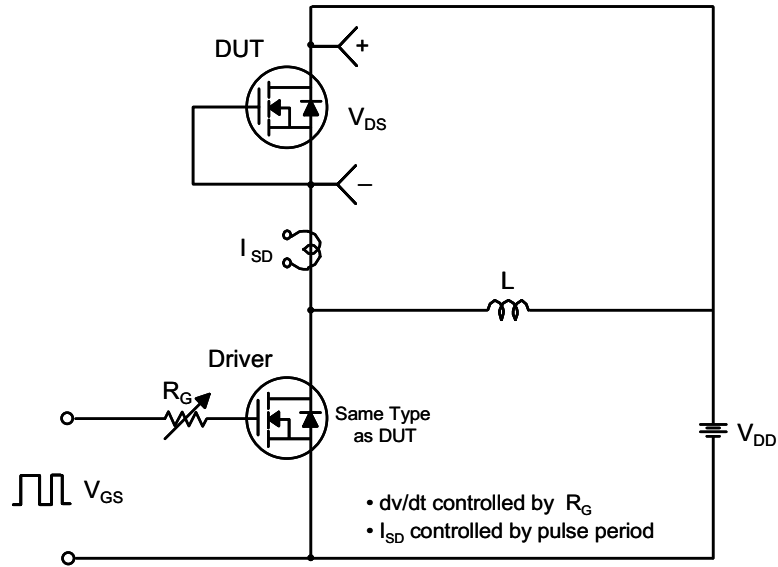
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

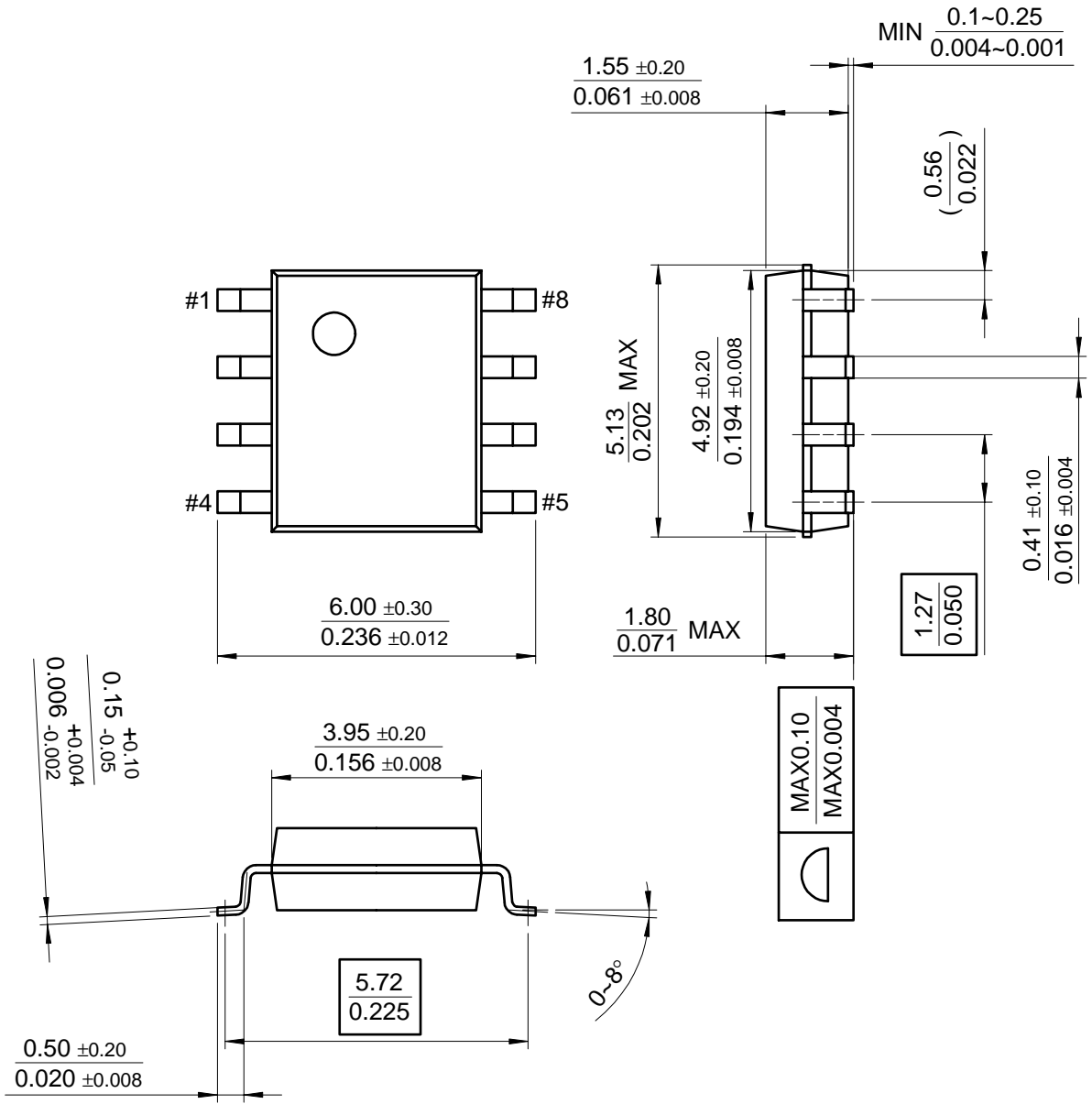


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimensions

8SOP





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