

Automotive-grade N-channel 40 V, 4.3 mΩ typ., 120 A STripFET™ II Power MOSFET in a D²PAK and TO-220

Datasheet - production data

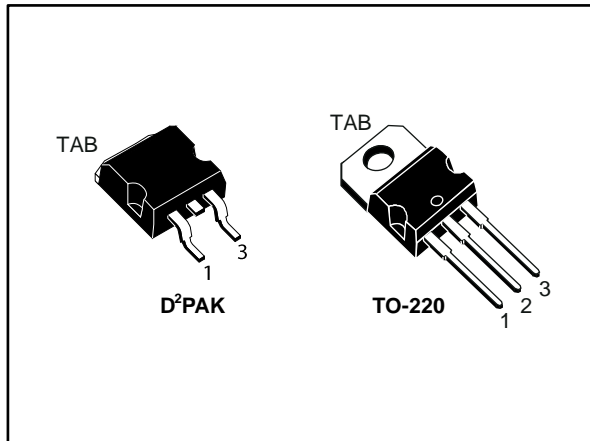
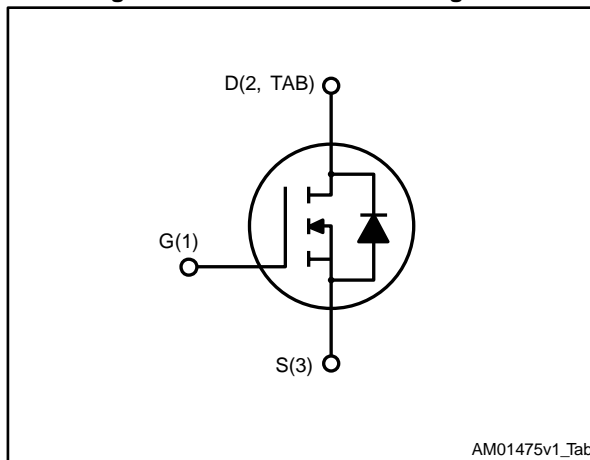


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{tot}
STB100NF04T4	40 V	4.6 mΩ	120 A	300 W
STP100NF04	40 V	4.6 mΩ	120 A	300 W



- AEC-Q101 qualified
- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge

Applications

- Switching applications

Description

These Power MOSFETs have been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the devices suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

Table 1: Device summary

Order code	Marking	Package	Packing
STB100NF04T4	B100NF04	D ² PAK	Tape and reel
STP100NF04	P100NF04	TO-220	Tube

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves).....	6
3	Spice thermal model	10
4	Test circuits	11
5	Package information	12
	5.1 D ² PAK packing information	12
	5.2 D ² PAK packing information	15
	5.3 TO-220 package information.....	17
6	Revision history	19

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate- source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	120	A
$I_D^{(1)}$	Drain current (continuous) at $T_C=100^\circ\text{C}$	120	A
$I_{DM}^{(2)}$	Drain current (pulsed)	480	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	300	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	6	V/ns
$E_{AS}^{(4)}$	Single pulse avalanche energy	1.2	J
T_j	Operating junction temperature range	- 55 to 175	$^\circ\text{C}$
T_{stg}	Storage temperature range		

Notes:

(1)Current limited by package

(2)Pulse width limited by safe operating area.

(3) $I_{SD} \leq 120\text{ A}$, $di/dt \leq 300\text{A}/\mu\text{s}$, $V_{DD} = V_{(BR)DSS}$, $T_j \leq T_{JMAX}$

(4)Starting $T_j = 25^\circ\text{C}$, $I_D = 60\text{ A}$, $V_{DD} = 30\text{ V}$.

Table 3: Thermal data

Symbol	Parameter	Value		Unit
		D ² PAK	TO-220	
$R_{thj-case}$	Thermal resistance junction-case	0.5		$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	35		$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient		62.5	$^\circ\text{C}/\text{W}$

Notes:

(1)When mounted on a 1-inch² FR-4 board, 2oz Cu.

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	40			V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 40\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 40\ \text{V}$, $V_{GS} = 0\ \text{V}$ $T_C = 125\text{ °C}^{(1)}$			10	μA
I_{GSS}	Gate body leakage current	$V_{GS} = \pm 20\ \text{V}$, $V_{DS} = 0\ \text{V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on- resistance	$V_{GS} = 10\ \text{V}$, $I_D = 50\ \text{A}$		4.3	4.6	m Ω

Notes:

⁽¹⁾Defined by design, not subject to production test

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\ \text{V}$, $f = 1\ \text{MHz}$, $V_{GS} = 0\ \text{V}$	-	5100		pF
C_{oss}	Output capacitance		-	1300		pF
C_{riss}	Reverse transfer capacitance		-	160		pF
Q_g	Total gate charge	$V_{DD} = 32\ \text{V}$, $I_D = 120\ \text{A}$, $V_{GS} = 10\ \text{V}$ (see Figure 21: "Test circuit for gate charge behavior")	-	110	150	nC
Q_{gs}	Gate-source charge		-	35		nC
Q_{gd}	Gate-drain charge		-	70		nC
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 20\ \text{V}$, $I_D = 60\ \text{A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\ \text{V}$ (see Figure 20: "Test circuit for resistive load switching times" and Figure 25: "Switching time waveform")	-	35		ns
t_r	Rise time		-	220		ns
$t_{d(off)}$	Turn-off delay time		-	80		ns
t_f	Fall time		-	50		ns

Table 6: Source drain diode

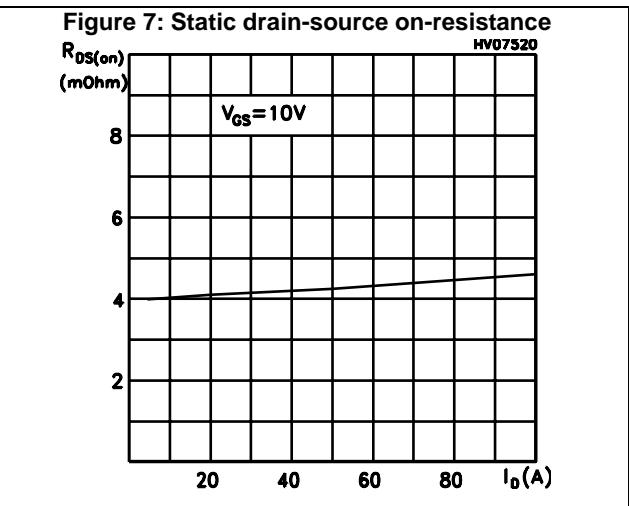
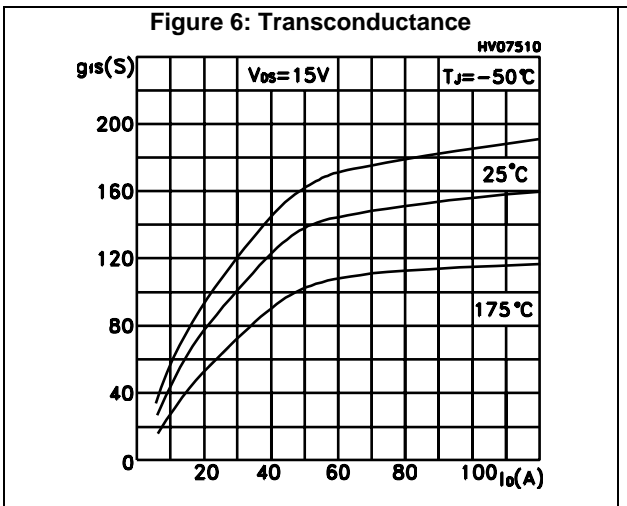
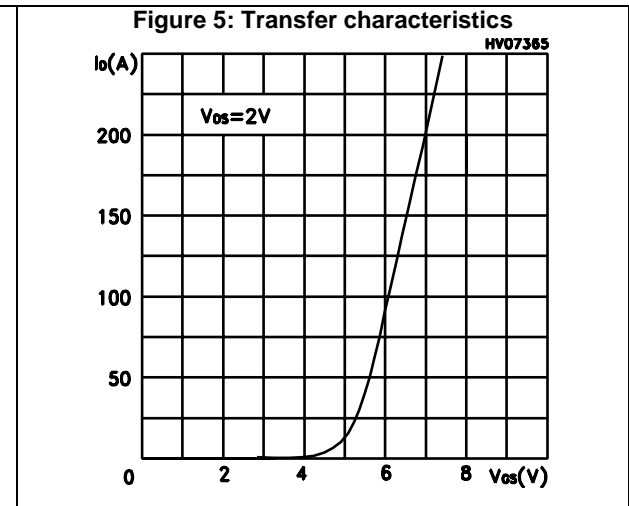
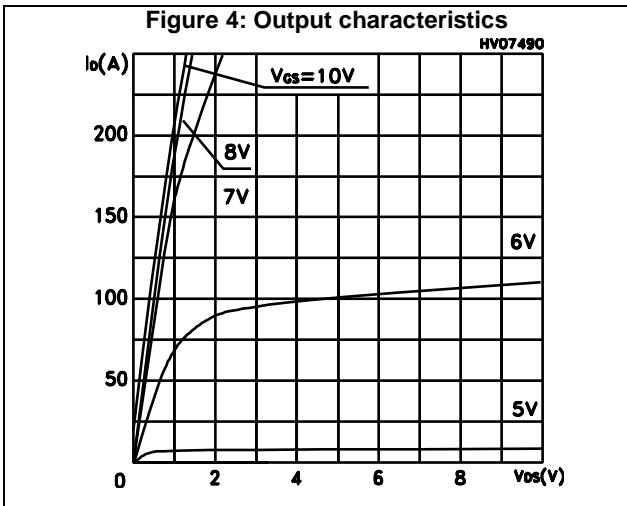
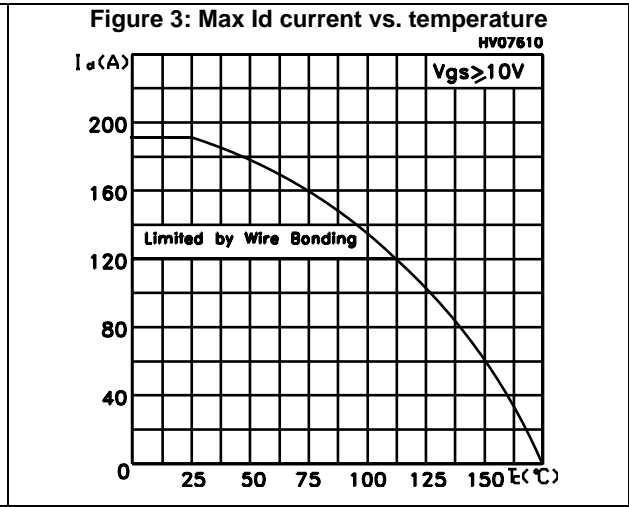
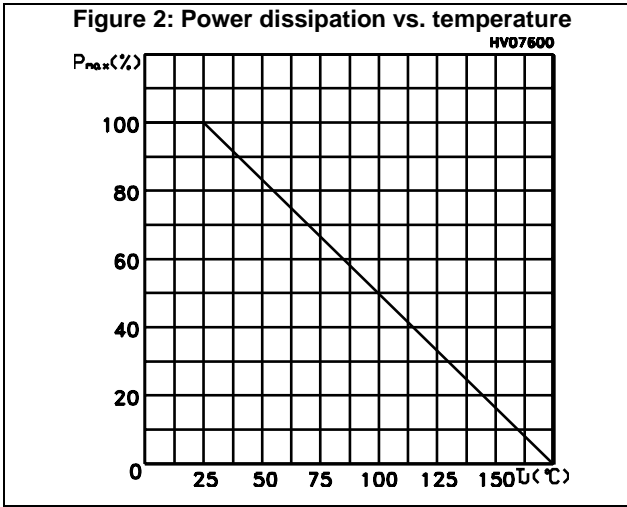
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		120	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		480	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 120 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.3	V
t_r	Reverse recovery time	$I_{SD} = 120 \text{ A}$, $V_{DD} = 20 \text{ V}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 22: "Test circuit for inductive load switching and diode recovery times")	-	75	-	ns
$t_{d(off)}$	Reverse recovery charge		-	185	-	nC
t_{fr}	Reverse recovery current		-	5	-	A

Notes:

(1)Pulse width limited by safe operating area.

(2)Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)



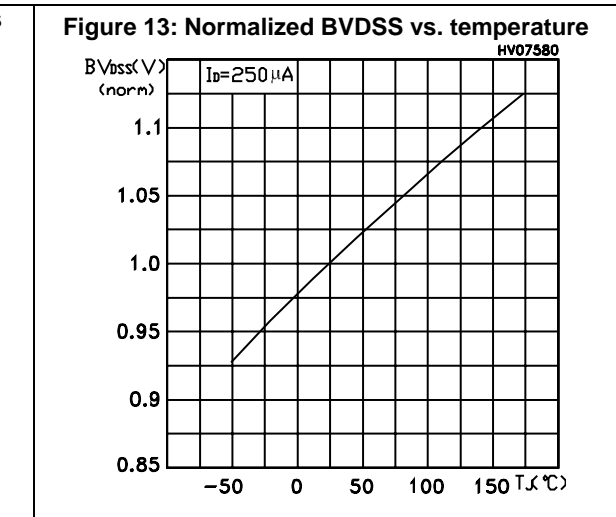
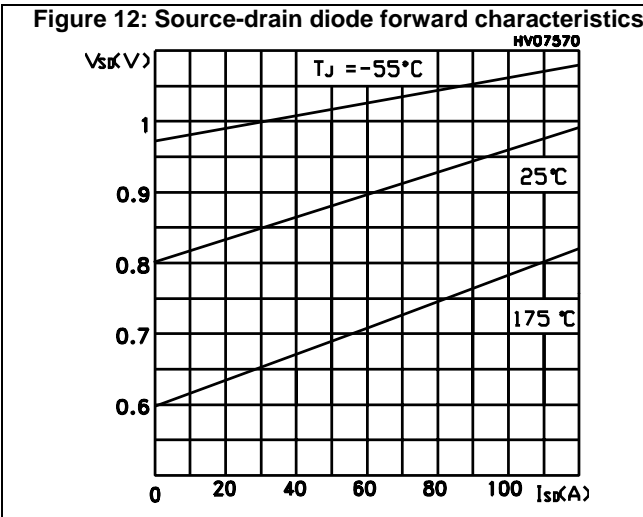
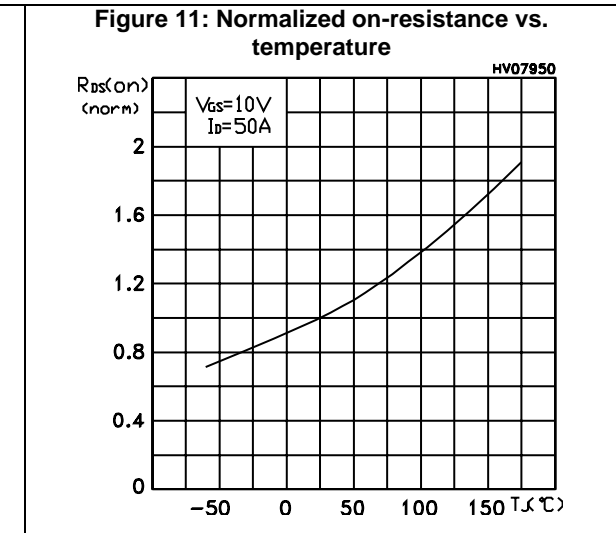
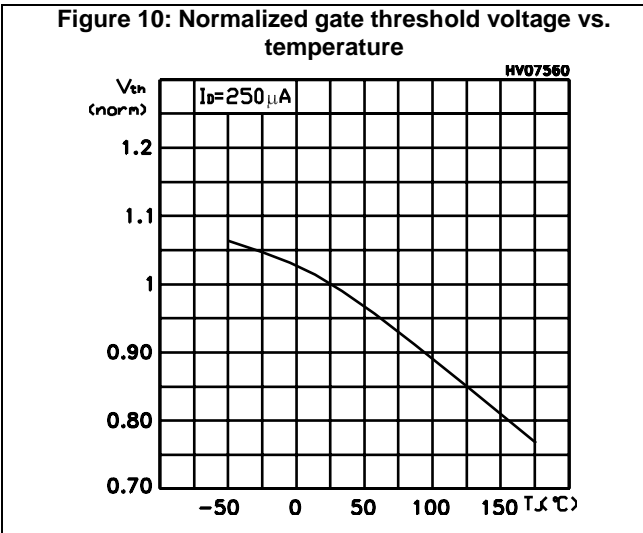
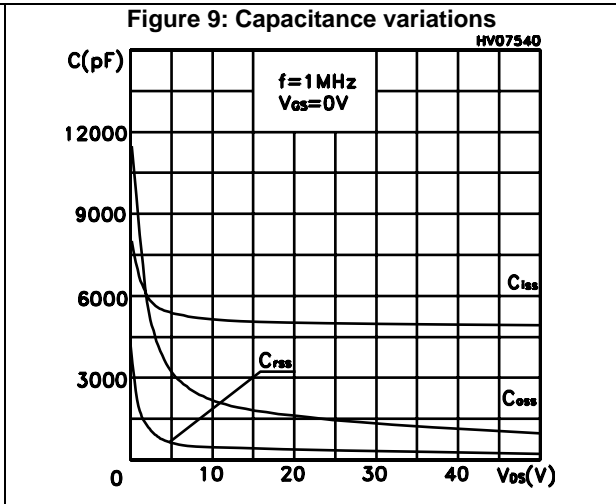
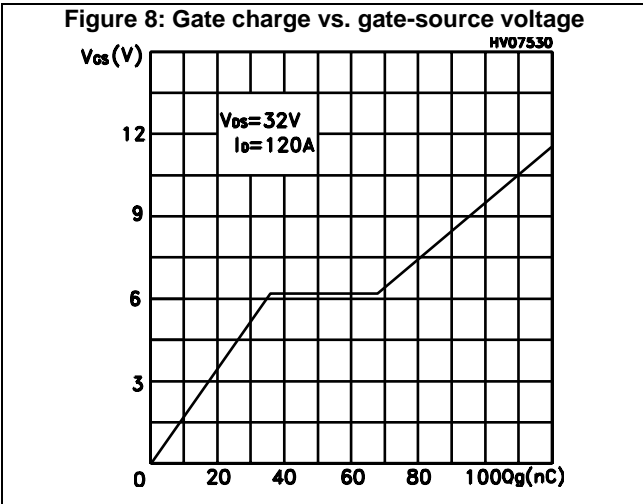


Figure 14: Thermal resistance $R_{thj-pcb}$ vs. PCB copper area

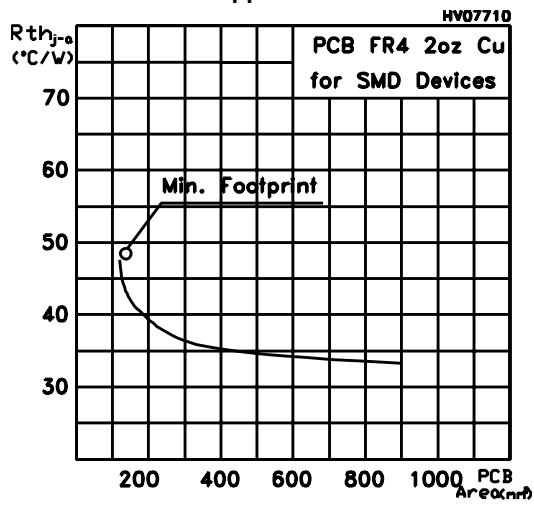


Figure 15: Thermal impedance

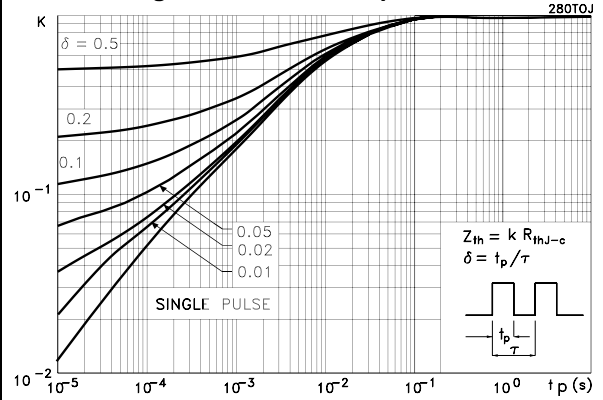


Figure 16: Max power dissipation vs. PCB copper area

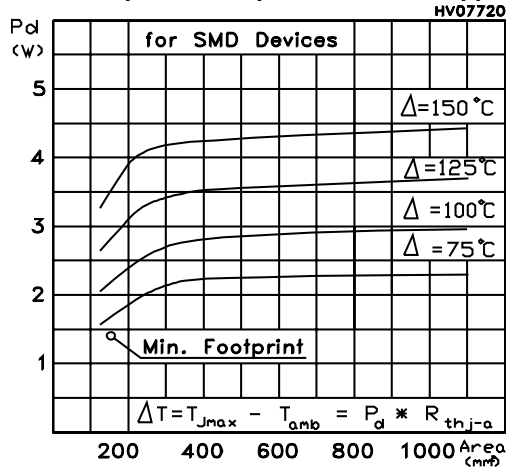
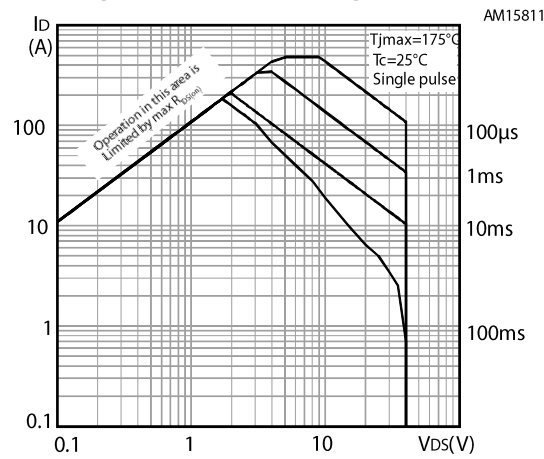
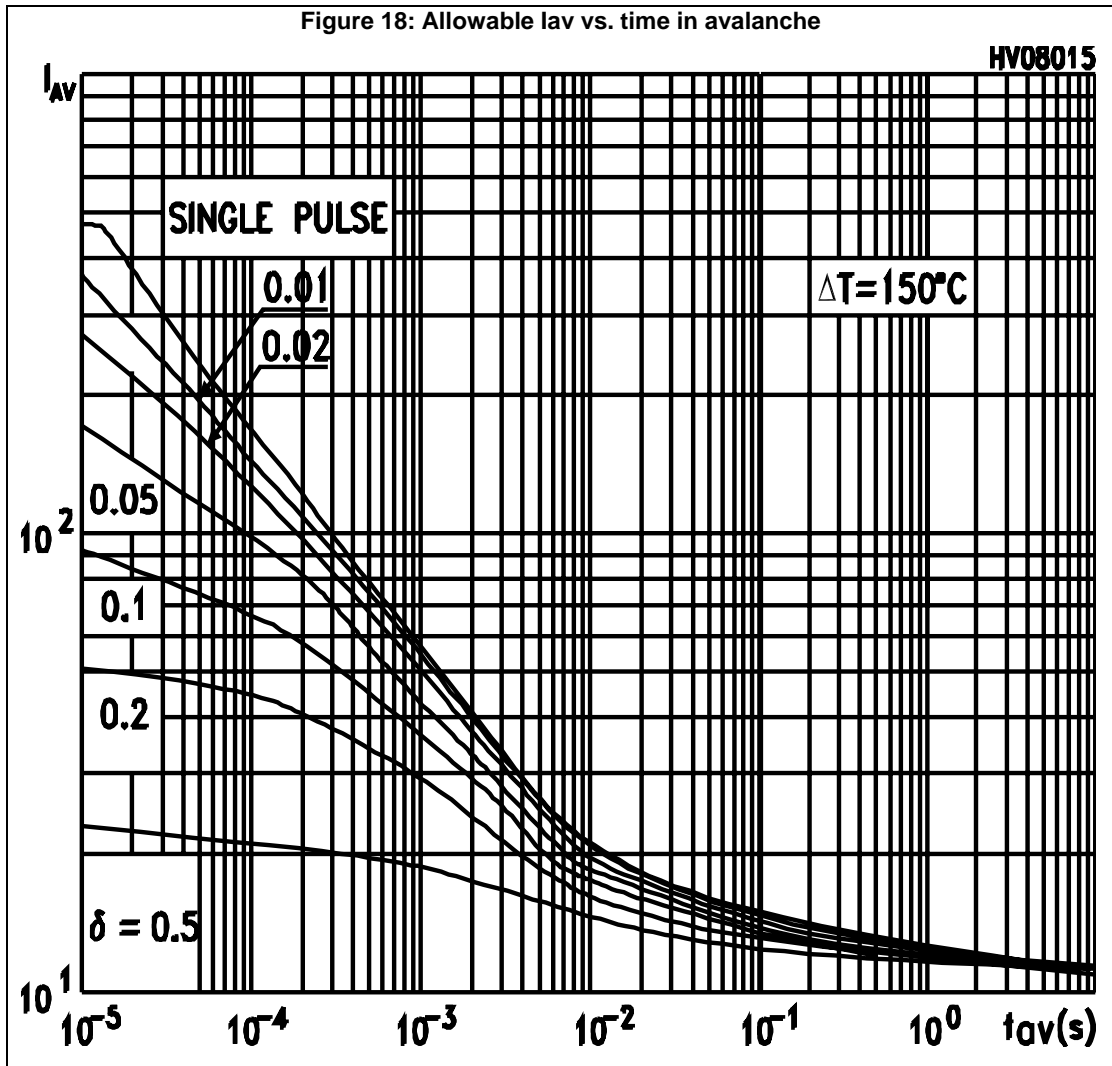


Figure 17: Safe operating area





The previous curve give the safe operating area for unclamped inductive loads, single pulse or repetitive, under the following conditions:

$$P_{D(AVE)} = 0.5 \cdot (1.3 \cdot BV_{DSS} \cdot I_{AV})$$

$$E_{AS(AR)} = P_{D(AVE)} \cdot T_{AV}$$

Where:

I_{AV} is the allowable current in avalanche

P_{D(AVE)} is the average power dissipation in avalanche(single pulse)

t_{AV} is the time in avalanche

To de rate above 25°C, at fixed I_{AV}, the following equation must be applied:

$$I_{AV} = 2 \cdot (T_{jmax} - T_{CASE}) / (1.3 \cdot BV_{DSS} \cdot Z_{th})$$

Where:

Z_{th} = K · R_{th} is the value coming from normalized thermal response at fixed pulse width equal to T_{AV}

3 Spice thermal model

Figure 19: Spice model schematic

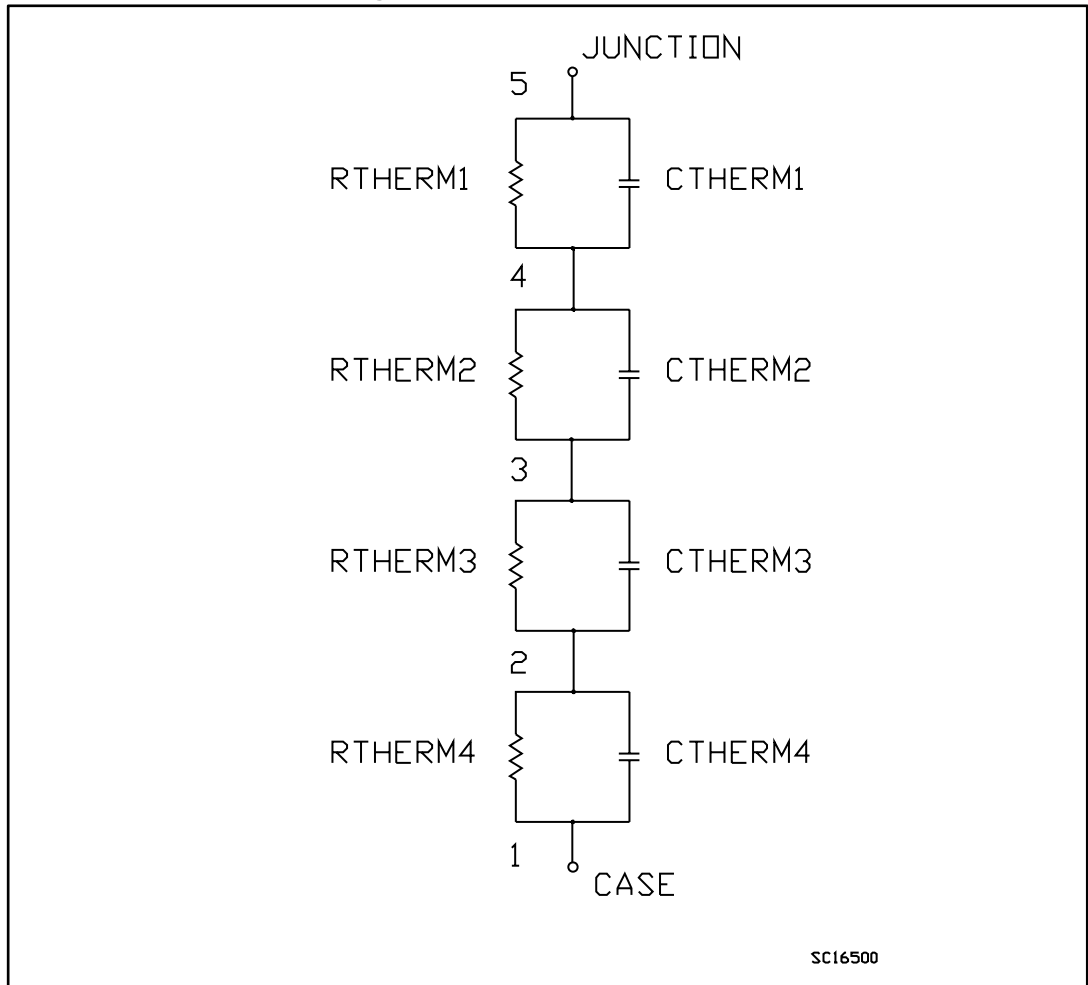
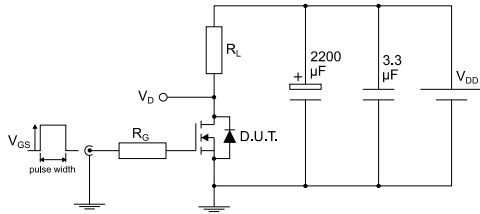


Table 7: Spice parameter

Parameter	Node	Value
C THERM1	5 - 4	0.011
C THERM1	4 - 3	0.0012
C THERM3	3 - 2	0.05
C THERM4	2 - 1	0.1
R THERM1	5 - 4	0.09
R THERM2	4 - 3	0.02
R THERM3	3 - 2	0.11
R THERM4	2 - 1	0.17

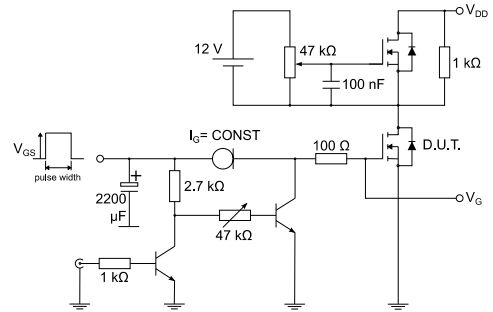
4 Test circuits

Figure 20: Test circuit for resistive load switching times



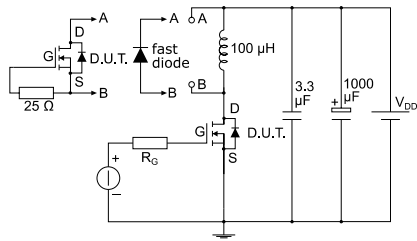
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Figure 21: Test circuit for gate charge behavior



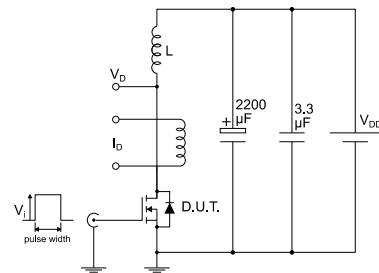
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Figure 22: Test circuit for inductive load switching and diode recovery times



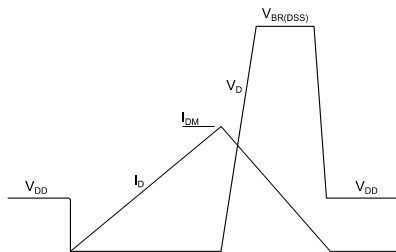
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Figure 23: Unclamped inductive load test circuit



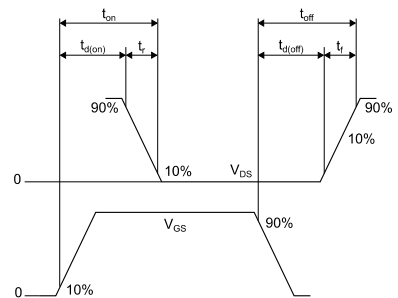
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Figure 24: Unclamped inductive waveform



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Figure 25: Switching time waveform



AM01473v1

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.1 D²PAK packing information

Figure 26: D²PAK (TO-263) type A package outline

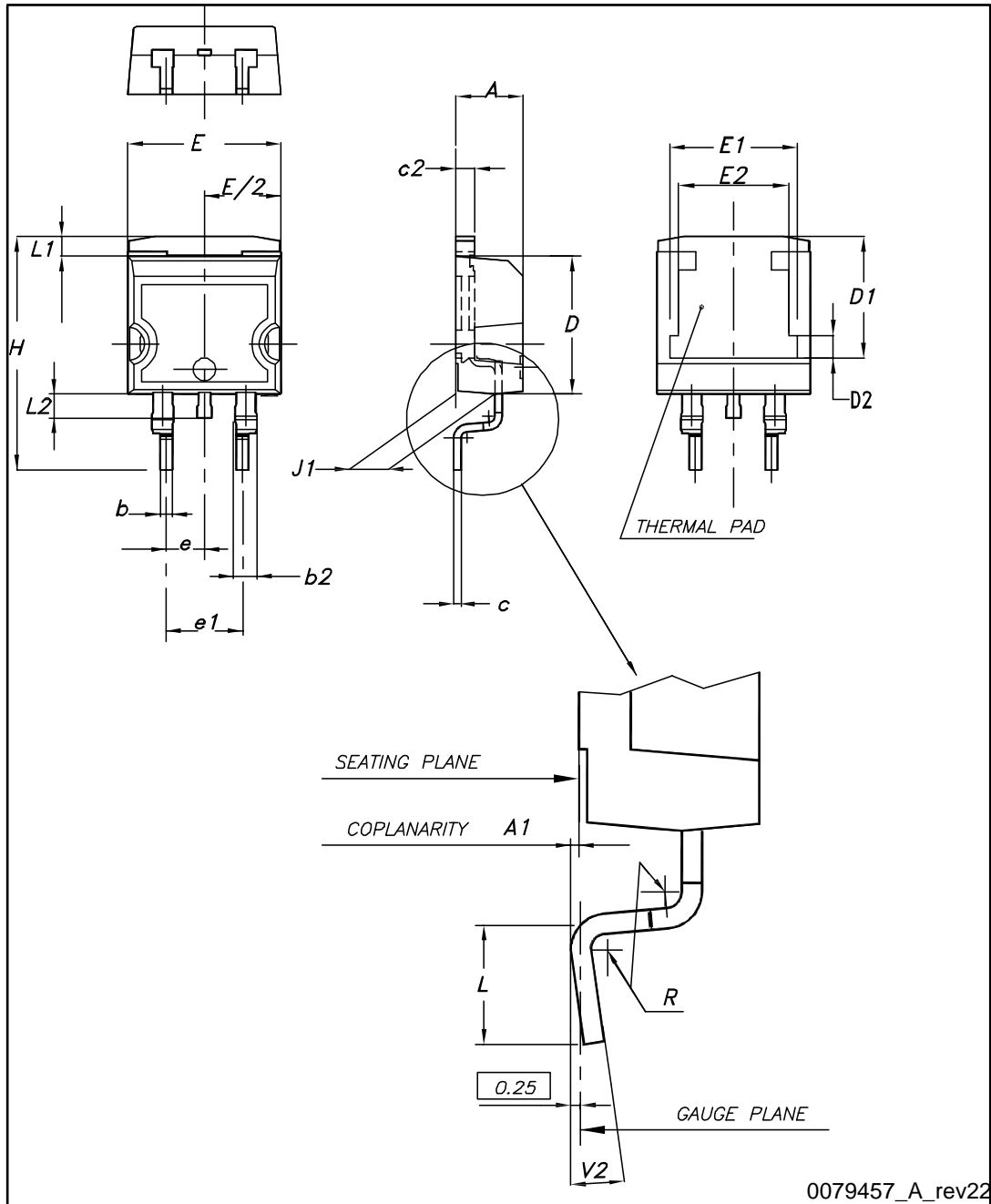
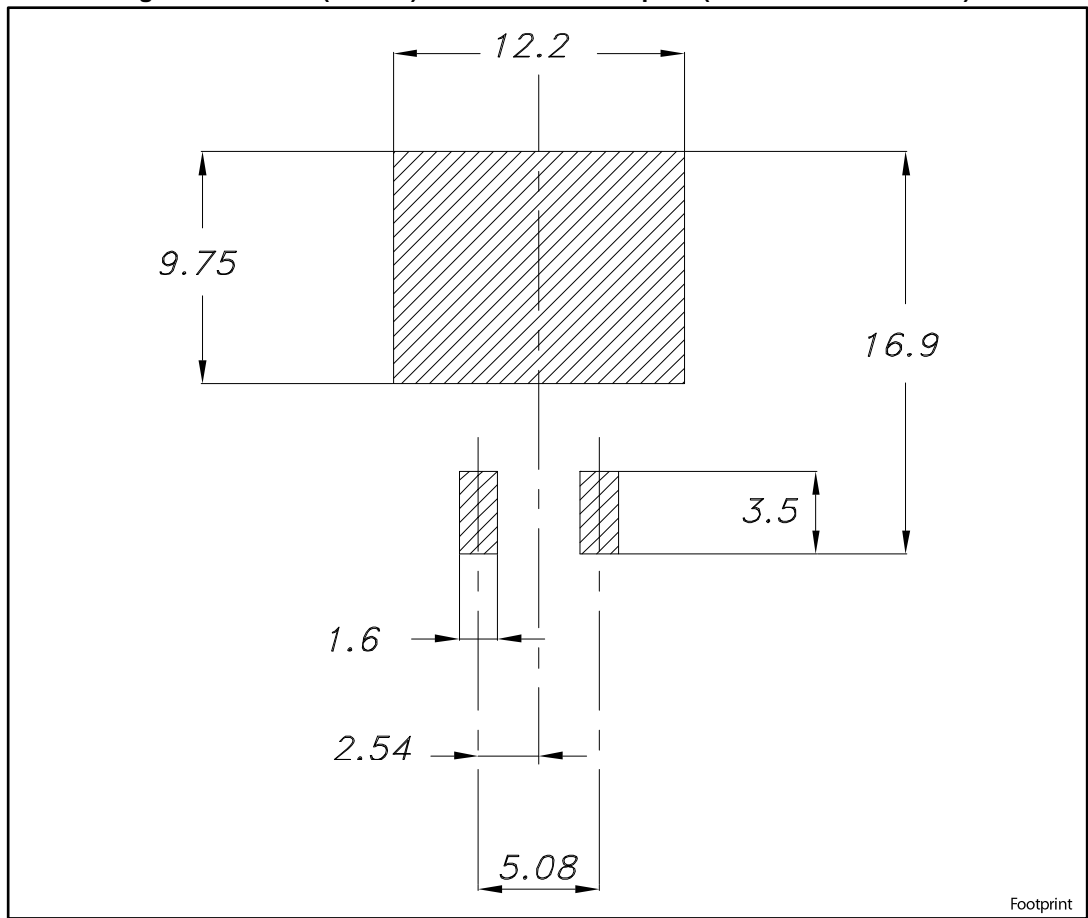


Table 8: D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 27: D²PAK (TO-263) recommended footprint (dimensions are in mm)



5.2 D²PAK packing information

Figure 28: Tape outline

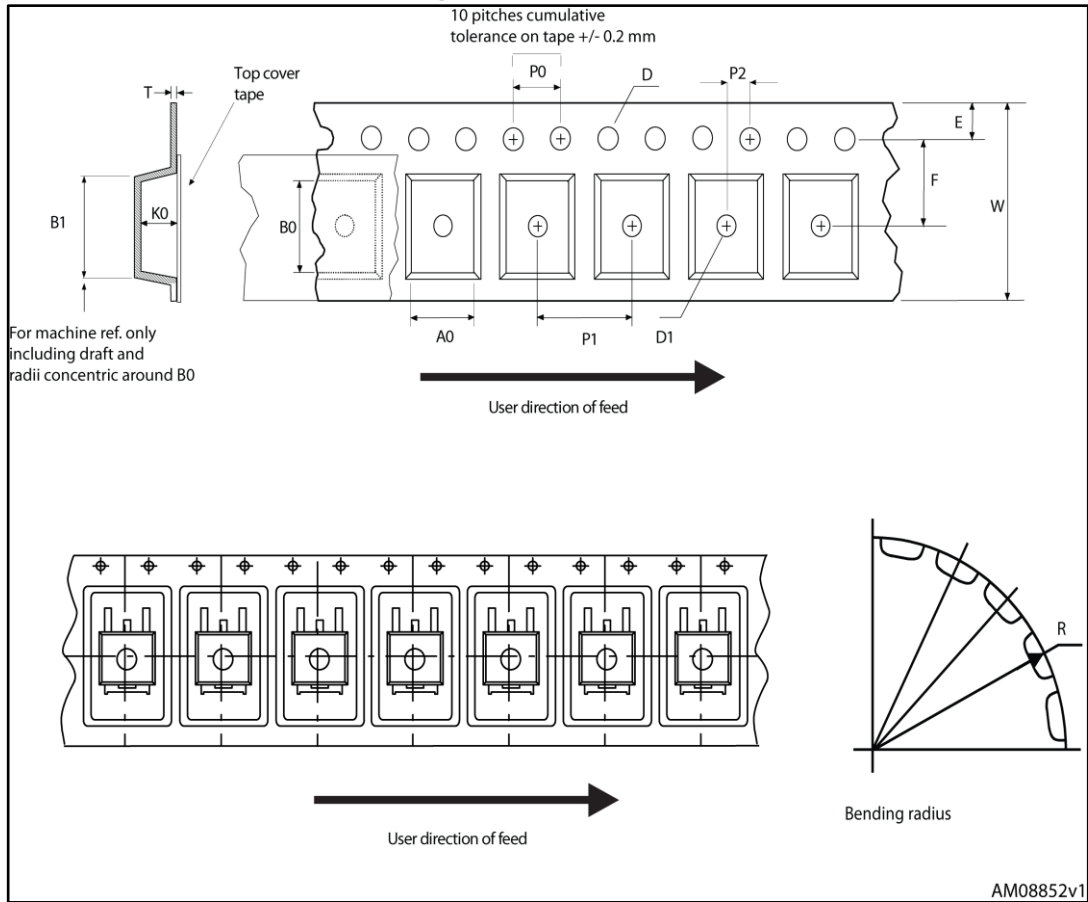
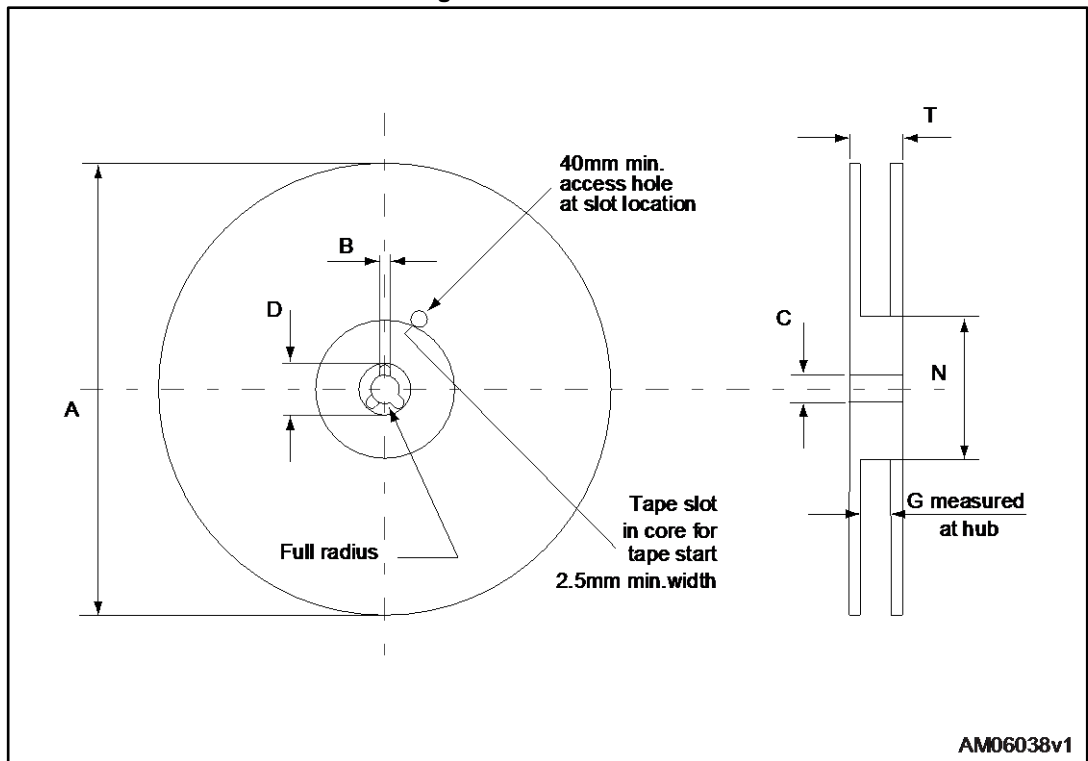


Figure 29: Reel outline



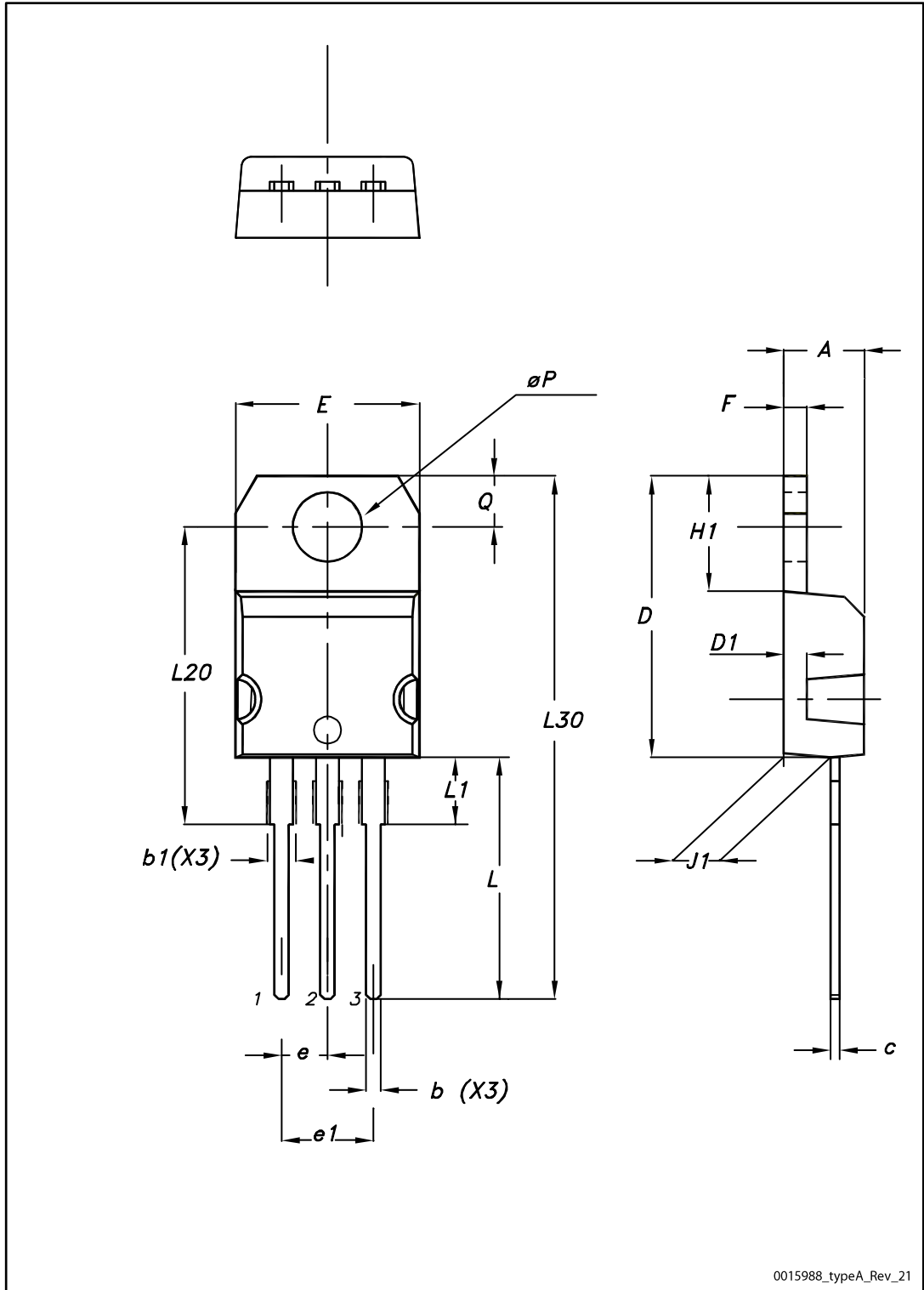
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Table 9: D²PAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

5.3 TO-220 package information

Figure 30: TO-220 type A package outline



0015988_typeA_Rev_21

Table 11: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

6 Revision history

Table 12: Document revision history

Date	Revision	Changes
23-Mar-2005	2	New template
01-Mar-2006	3	Removed I ² PAK and inserted D ² PAK.
04-Sep-2006	4	New template, no content change
20-Feb-2007	5	Typo mistake on page 1
16-Mar-2013	6	Minor text changes – Modified: <i>Figure 17</i> – Updated: Section 4: <i>Package mechanical data</i> and Section 5: <i>Packaging mechanical data</i>
21-Nov-2016	7	Updated title in cover page. Updated Section 2: "Electrical characteristics" . Minor text changes.

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