



# STD9NM60N STF9NM60N, STP9NM60N

N-channel 600 V, 0.63  $\Omega$ , 6.5 A TO-220, TO-220FP, DPAK  
MDmesh™ II Power MOSFET

## Features

Order codes	V <sub>DSS</sub> (@T <sub>jmax</sub> )	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STD9NM60N	650 V	< 0.745 $\Omega$	6.5 A
STF9NM60N			
STP9NM60N			

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

## Application

Switching applications

## Description

This series of devices is realized with the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

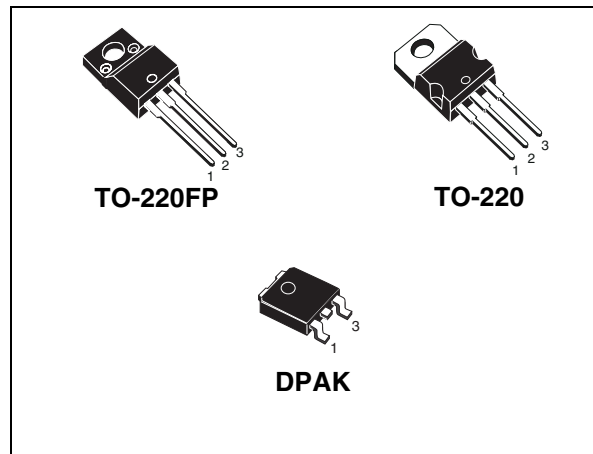


Figure 1. Internal schematic diagram

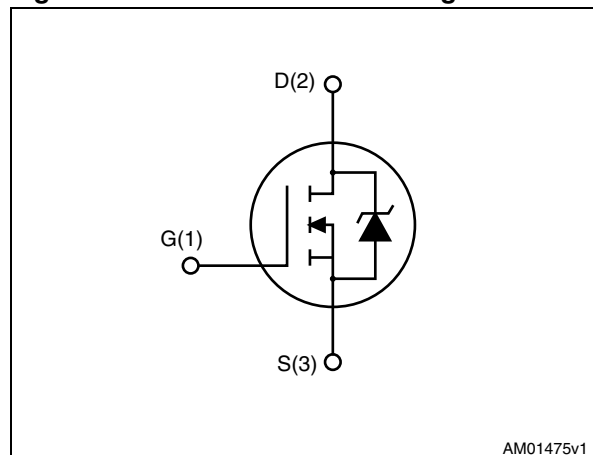


Table 1. Device summary

Order codes	Marking	Packages	Packaging
STD9NM60N	9NM60N	DPAK	Tape and reel
STF9NM60N		TO-220FP	Tube
STP9NM60N		TO-220	

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220, DPAK	TO-220FP	
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	600		V
$V_{GS}$	Gate- source voltage	$\pm 25$		V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	6.5	6.5 <sup>(1)</sup>	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	4	4 <sup>(1)</sup>	A
$I_{DM}^{(2)}$	Drain current (pulsed)	26	26 <sup>(1)</sup>	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	70	25	W
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t=1\text{ s}; T_C=25\text{ }^\circ\text{C}$ )		2500	V
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15		V/ns
$T_{stg}$	Storage temperature	- 55 to 150		$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150		$^\circ\text{C}$

- Limited only by maximum temperature allowed
- Pulse width limited by safe operating area
- $I_{SD} \leq 6.5\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value			Unit
		DPAK	TO-220	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case max	1.79		5	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb minimum footprint	50			$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max		62.5		$^\circ\text{C}/\text{W}$
$T_l$	Maximum lead temperature for soldering purpose		300		$^\circ\text{C}$

- When mounted on 1inch<sup>2</sup> FR-4 board, 2 oz Cu

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ Max)	2.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	115	mJ

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	600			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{max rating}$ $V_{DS} = \text{max rating}$ , @125 °C			1 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 3.25\text{ A}$		0.63	0.745	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	452	-	pF
$C_{oss}$	Output capacitance			30		pF
$C_{rss}$	Reverse transfer capacitance			1.45		pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0$ , $V_{DS} = 0\text{ to }480\text{ V}$	-	79	-	pF
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}$ , $I_D = 6.5\text{ A}$ , $V_{GS} = 10\text{ V}$ , <i>(see Figure 18)</i>	-	17.4	-	nC
$Q_{gs}$	Gate-source charge			3		nC
$Q_{gd}$	Gate-drain charge			9.7		nC
$R_g$	Gate input resistance	f=1 MHz Gate DC Bias=0 Test signal level=20 mV open drain	-	4.8	-	$\Omega$

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V^{DS}$  increases from 0 to 80%  $V_{DS}$ .

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 480\text{ V}$ , $I_D = 6.5\text{ A}$ $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ <i>(see Figure 17)</i>	-	28	-	ns
$t_r$	Rise time		-	23	-	ns
$t_{d(off)}$	Turn-off delay time		-	52.5	-	ns
$t_f$	Fall time		-	26.7	-	ns

**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		6.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				26	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 6.5\text{ A}$ , $V_{GS} = 0$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 6.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ <i>(see Figure 22)</i>	-	264		ns
$Q_{rr}$	Reverse recovery charge				1.9	$\mu\text{C}$
$I_{RRM}$	Reverse recovery current				14.6	A
$t_{rr}$	Reverse recovery time	$I_{SD} = 6.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ <i>(see Figure 22)</i>	-	324		ns
$Q_{rr}$	Reverse recovery charge				2.3	$\mu\text{C}$
$I_{RRM}$	Reverse recovery current				14.2	A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

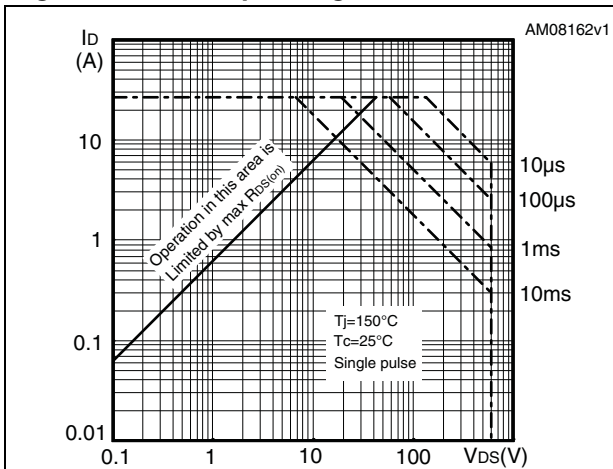


Figure 3. Thermal impedance for TO-220

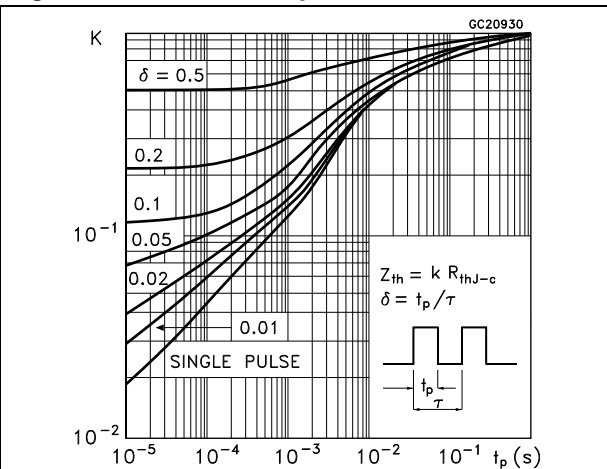


Figure 4. Safe operating area for DPAK

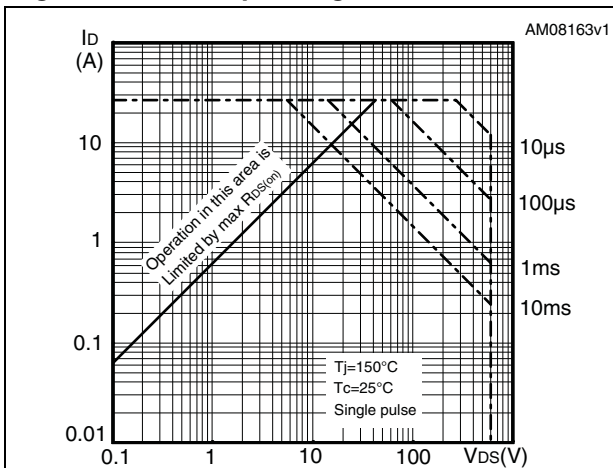


Figure 5. Thermal impedance for DPAK

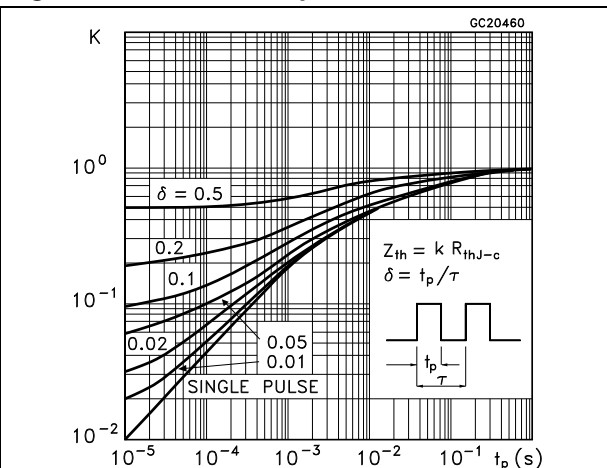


Figure 6. Safe operating area for TO-220FP

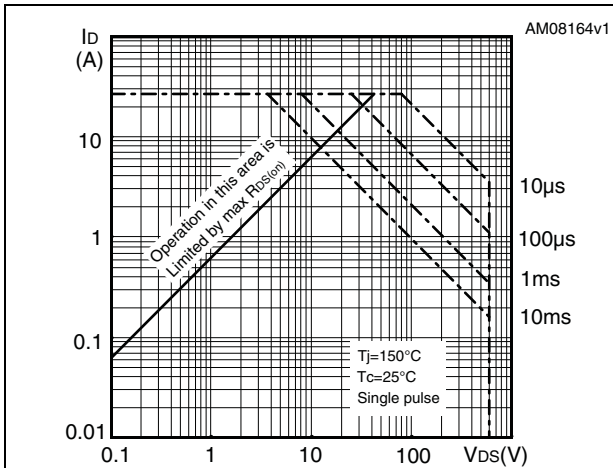


Figure 7. Thermal impedance for TO-220FP

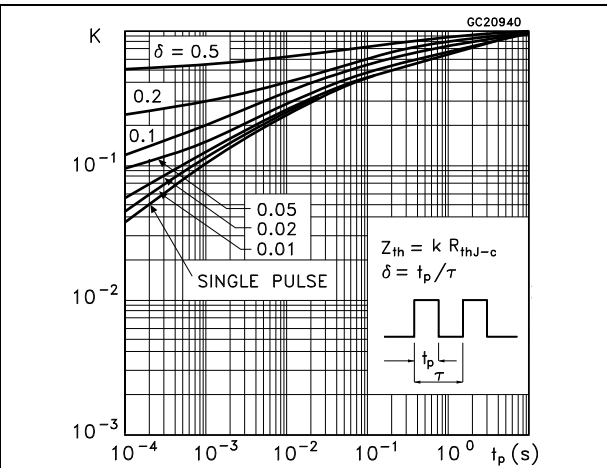


Figure 8. Output characteristics

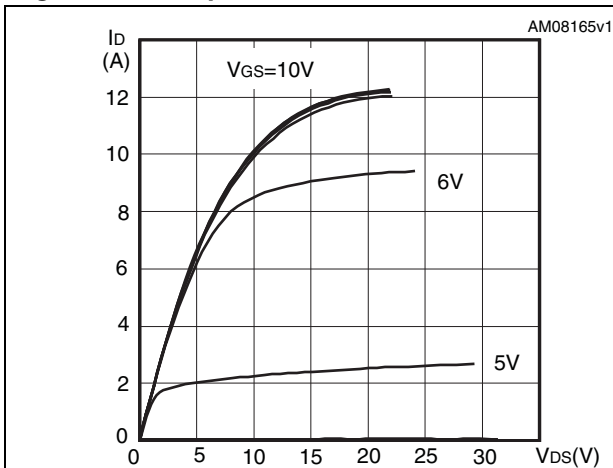


Figure 9. Transfer characteristics

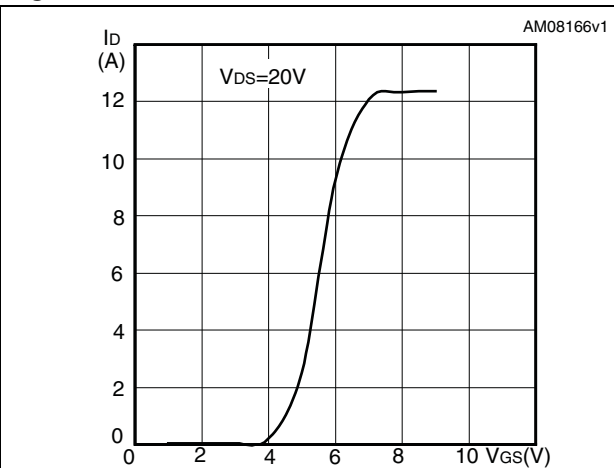


Figure 10. Gate charge vs gate-source voltage

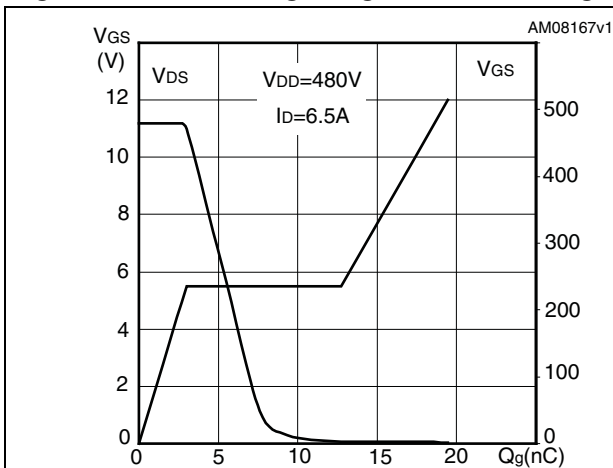


Figure 11. Static drain-source on resistance

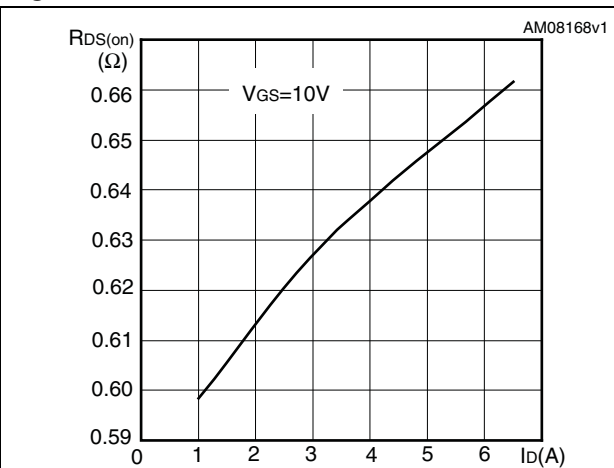


Figure 12. Capacitance variations

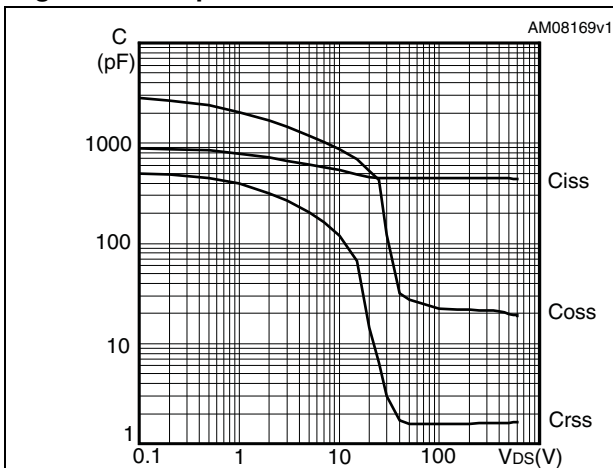


Figure 13. Output capacitance stored energy

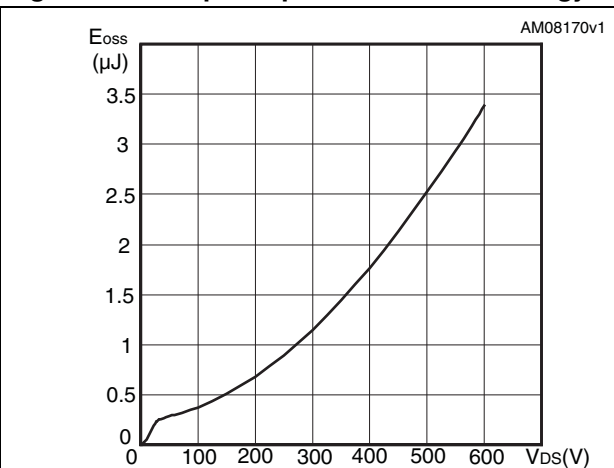


Figure 14. Normalized gate threshold voltage vs temperature

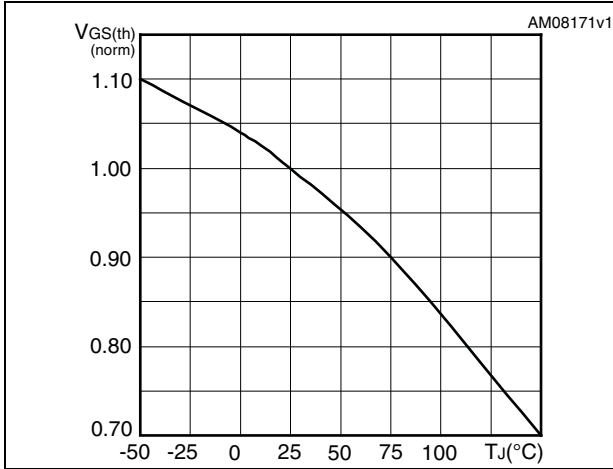


Figure 15. Normalized on resistance vs temperature

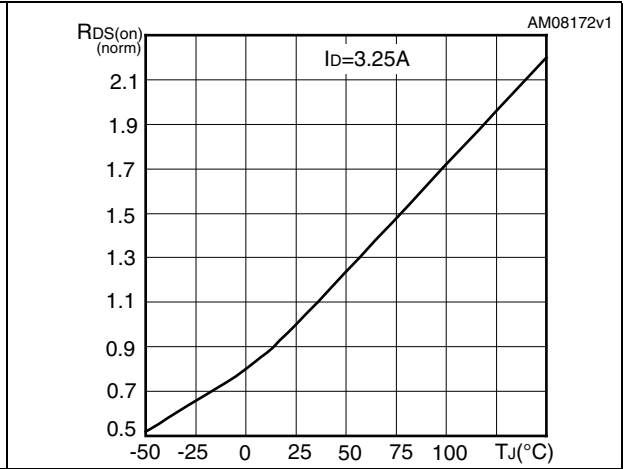
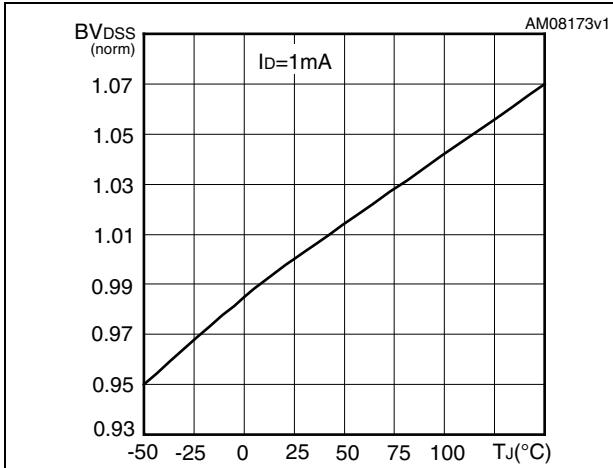


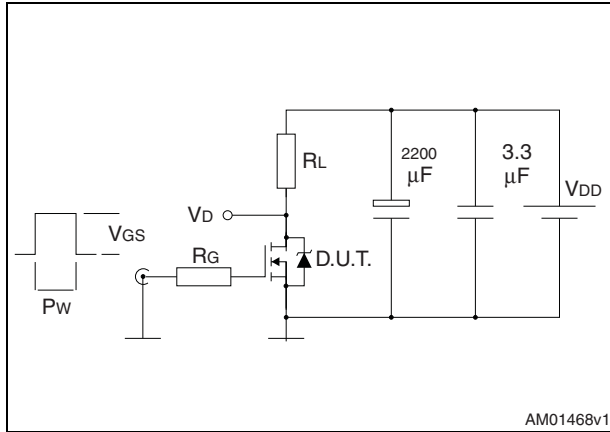
Figure 16. Normalized B<sub>VDSS</sub> vs temperature





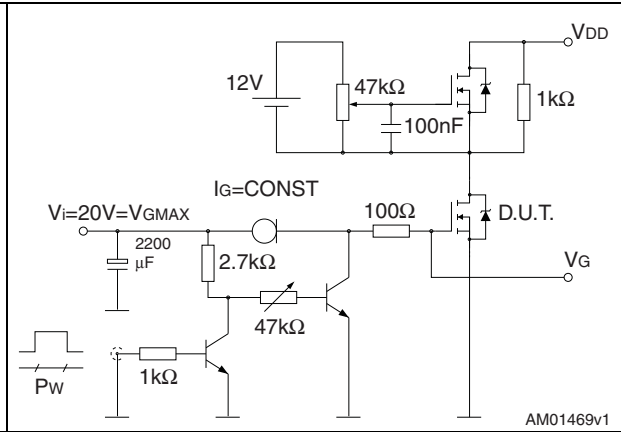
### 3 Test circuits

**Figure 17. Switching times test circuit for resistive load**



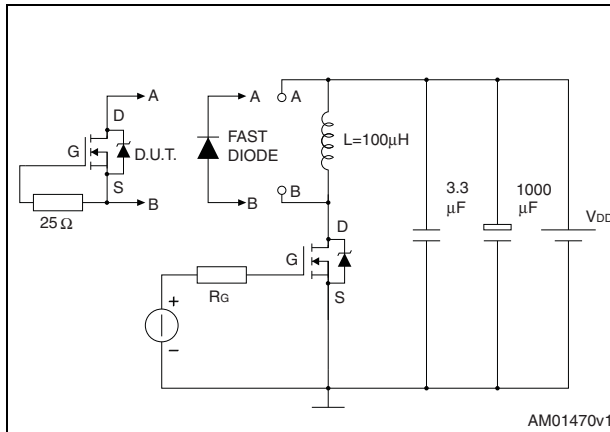
AM01468v1

**Figure 18. Gate charge test circuit**



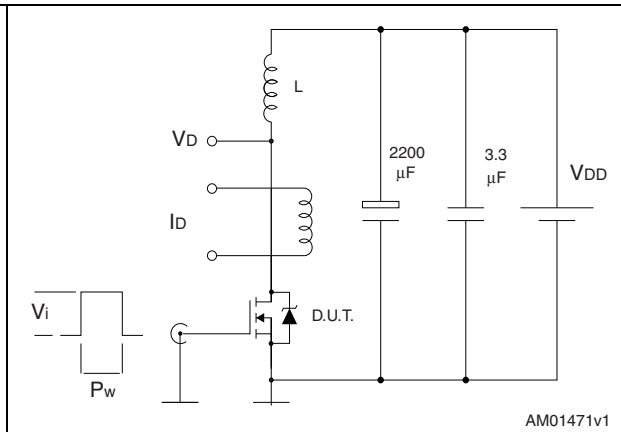
AM01469v1

**Figure 19. Test circuit for inductive load switching and diode recovery times**



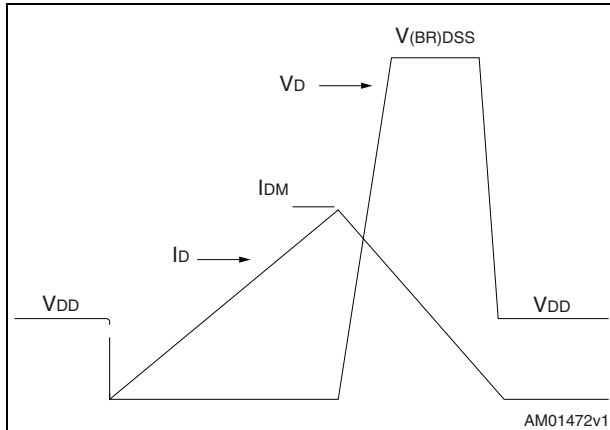
AM01470v1

**Figure 20. Unclamped inductive load test circuit**



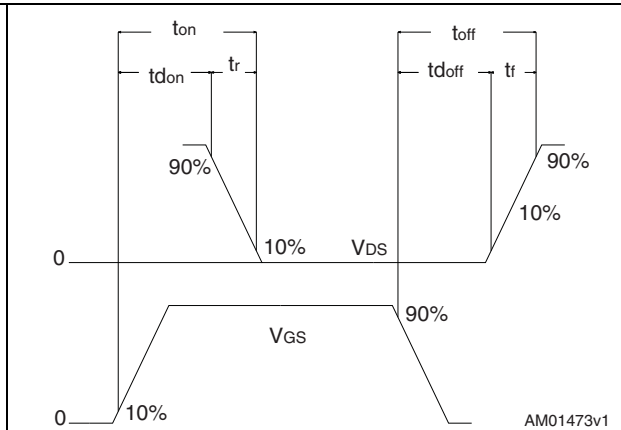
AM01471v1

**Figure 21. Unclamped inductive waveform**



AM01472v1

**Figure 22. Switching time waveform**



AM01473v1

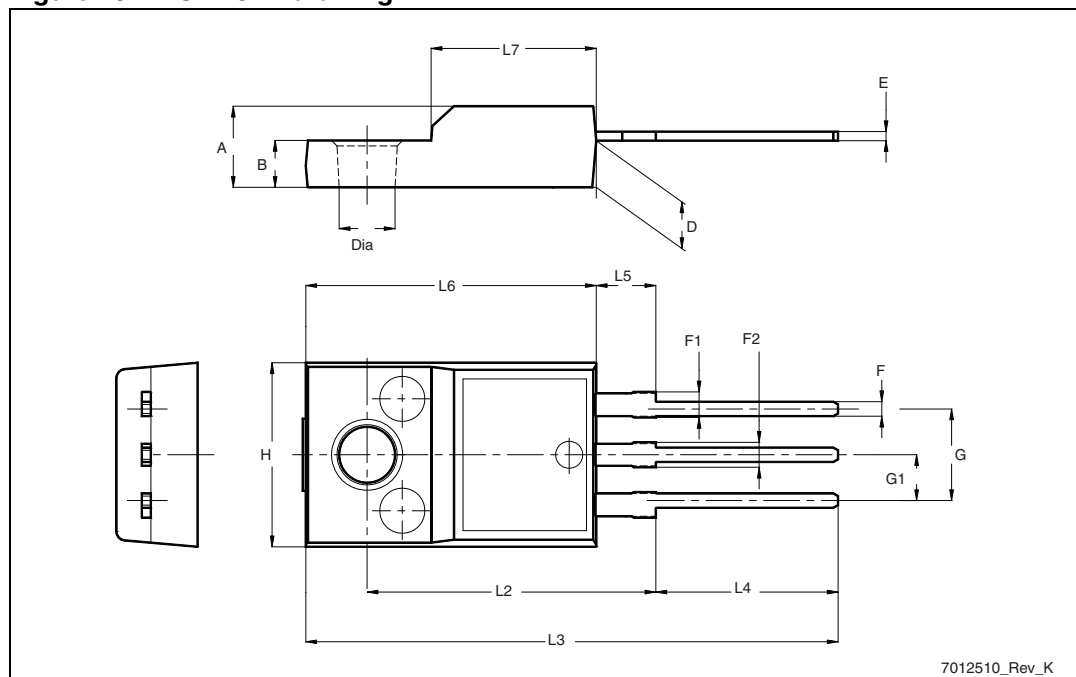
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 9. TO-220FP mechanical data

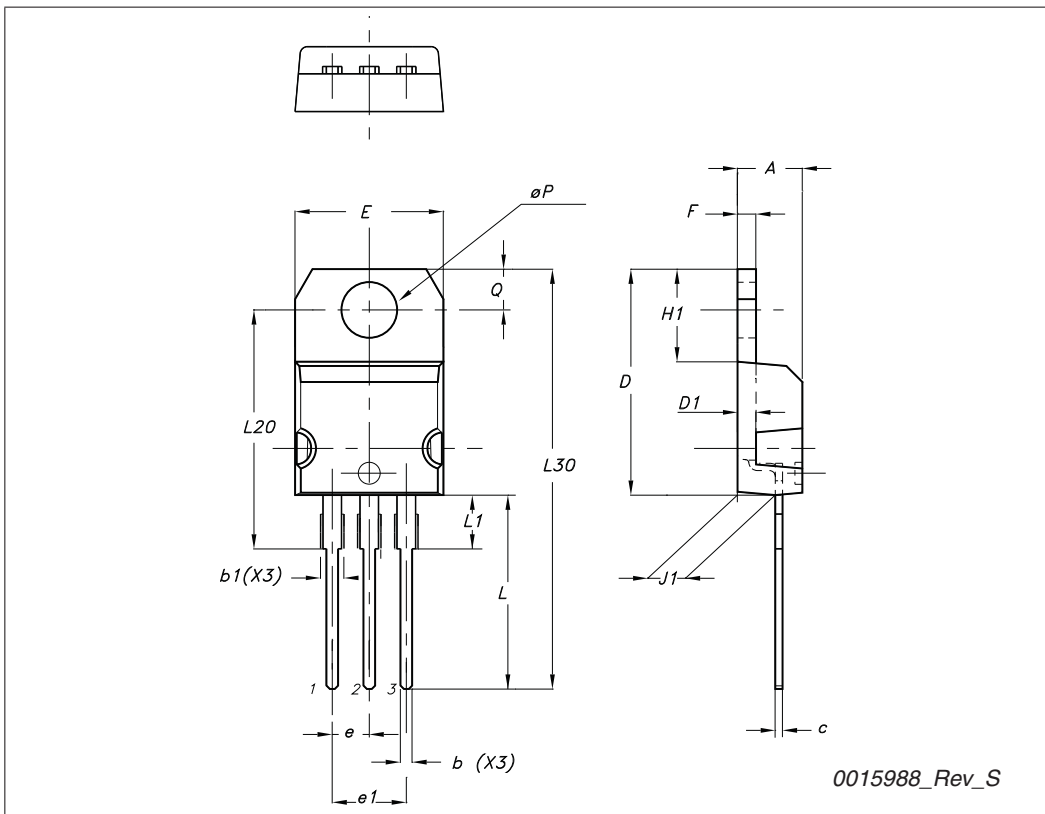
Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 23. TO-220FP drawing



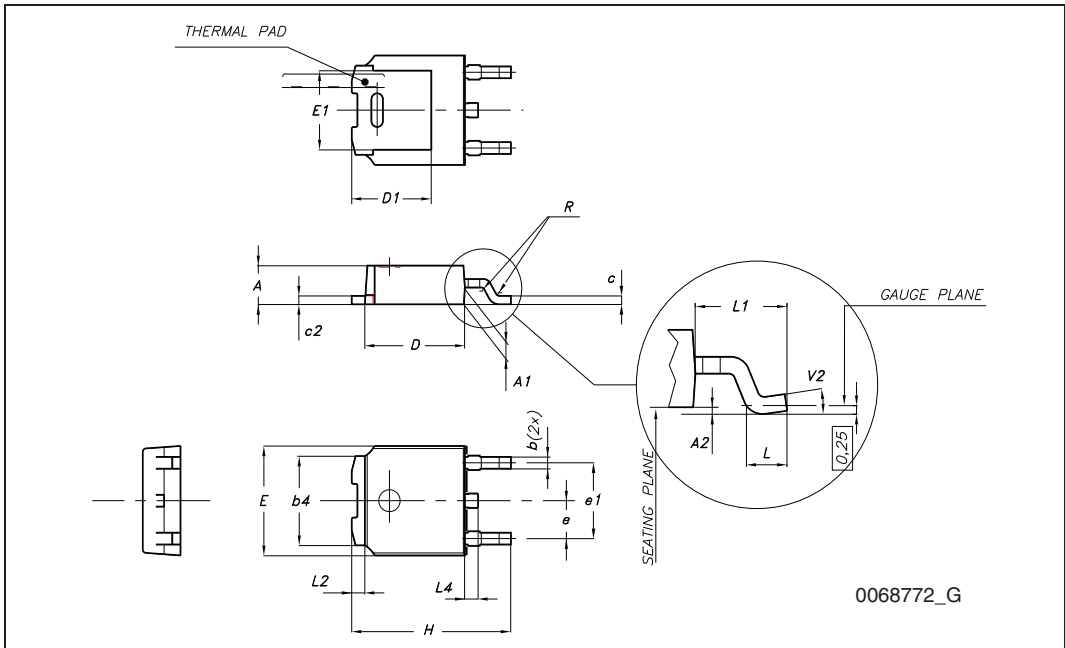
TO-220 type A mechanical data

Dim	mm		
	Min	Typ	Max
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95



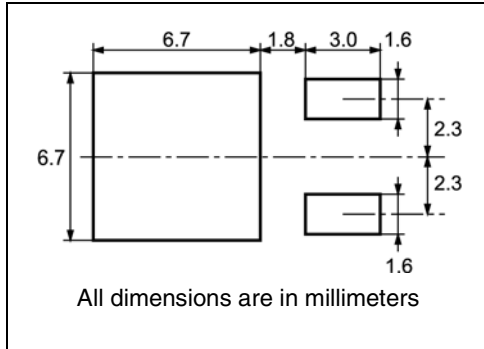
TO-252 (DPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°



# 5 Package mechanical data

## DPAK FOOTPRINT



## TAPE AND REEL SHIPMENT

40 mm min. Access hole at slot location

Full radius

Tape slot in core for tape start 2.5mm min. width

G measured at hub

### REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

### TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

TOP COVER TAPE

User Direction of Feed

Center line of cavity

Bending radius R min.

FEED DIRECTION

TRL

For machine ref. only including draft and radii concentric around B0

10 pitches cumulative tolerance on tape +/- 0.2 mm

## 6 Revision history

Table 10. Document revision history

Date	Revision	Changes
20-Oct-2010	1	First release.

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