

N-Channel Power MOSFET

60V, 300mA, 2Ω

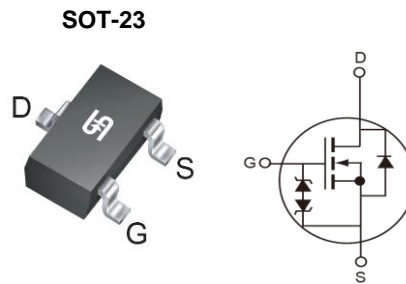
FEATURES

- Low On-Resistance
- ESD Protected 2KV
- High Speed Switching
- Low Voltage Drive

APPLICATION

- Logic Level translators
- DC-DC Converter

KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
V_{DS}	60	V
$R_{DS(on)}$ (max)	$V_{GS} = 10V$	2
	$V_{GS} = 4.5V$	4
Q_g	0.4	nC



Notes: Moisture sensitivity level: level 3. Per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^(Note 1)	I_D	$T_A = 25^\circ\text{C}$	300
		$T_A = 100^\circ\text{C}$	180
Pulsed Drain Current ^(Note 2)	I_{DM}	800	mA
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_{DTOT}	300	mW
Single Pulsed Avalanche Energy ^(Note 3)	E_{AS}	0.2	mJ
Single Pulsed Avalanche Current ^(Note 3)	I_{AS}	2	A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	$^\circ\text{C}$

THERMAL PERFORMANCE			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	350	$^\circ\text{C/W}$

Notes: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB in still air

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 4)						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 10\mu A$	BV_{DSS}	60	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	1.0	1.5	2.5	V
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I_{GSS}	--	--	± 10	μA
Zero Gate Voltage Drain Current	$V_{DS} = 60V, V_{GS} = 0V$	I_{DSS}	--	--	1.0	μA
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 300mA$	$R_{DS(ON)}$	--	1.2	2	Ω
	$V_{GS} = 4.5V, I_D = 200mA$		--	2	4	
Forward Transconductance	$V_{DS} = 10V, I_D = 200mA$	g_{fs}	100	--	--	mS
Diode Forward Voltage	$I_S = 300mA, V_{GS} = 0V$	V_{SD}	--	0.8	1.4	V
Dynamic (Note 5)						
Total Gate Charge	$V_{DS} = 10V, I_D = 250mA,$ $V_{GS} = 4.5V$	Q_g	--	0.4	0.6	nC
Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0MHz$	C_{iss}	--	30	--	μF
Output Capacitance		C_{oss}	--	6	--	
Reverse Transfer Capacitance		C_{rss}	--	2.5	--	
Gate Resistance	$F = 1MHz, \text{open drain}$	R_g	--	70	--	Ω
Switching (Note 6)						
Turn-On Delay Time	$V_{DD} = 30V, R_G = 10\Omega$ $I_D = 200mA, V_{GEN} = 10V,$	$t_{d(on)}$	--	25	--	ns
Turn-Off Delay Time		$t_{d(off)}$	--	35	--	
Source-Drain Diode (Note 4)						
Diode Forward Voltage	$I_S = 300mA, V_{GS} = 0V$	V_{SD}	--	0.8	1.4	
Reverse Recovery Time	$I_S = 0.5A$	t_{rr}	--	40	--	ns
Reverse Recovery Charge	$di_f/dt = 100A/\mu s$	Q_{rr}	--	39	--	nC

Notes:

1. Current limited by package
2. Pulse width limited by the maximum junction temperature
3. $L = 0.1mH, I_{AS} = 2A, V_{DD} = 25V, R_G = 25\Omega, \text{Starting } T_J = 25^\circ\text{C}$
4. Pulse test: $PW \leq 300\mu s, \text{duty cycle} \leq 2\%$
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.

ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM2N7002KCX RFG	SOT-23	3,000pcs / 7" Reel

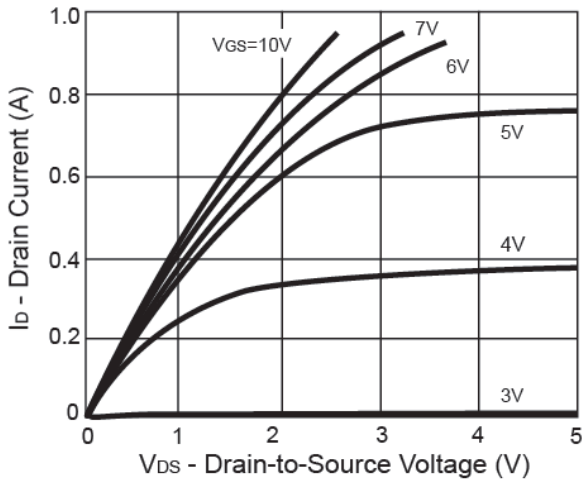
Note:

1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
2. Halogen-free according to IEC 61249-2-21 definition

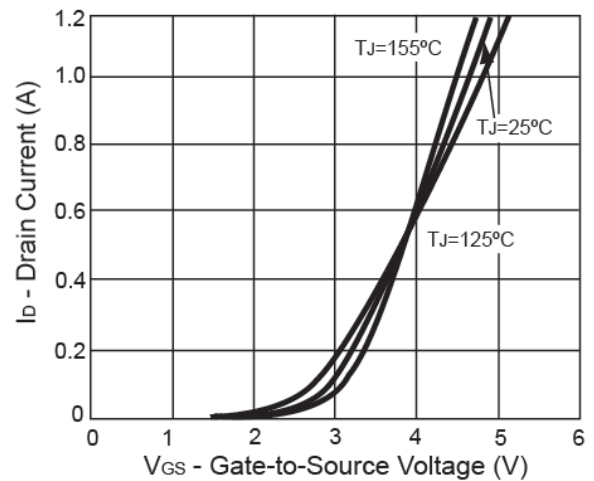
CHARACTERISTICS CURVES

($T_C = 25^\circ\text{C}$ unless otherwise noted)

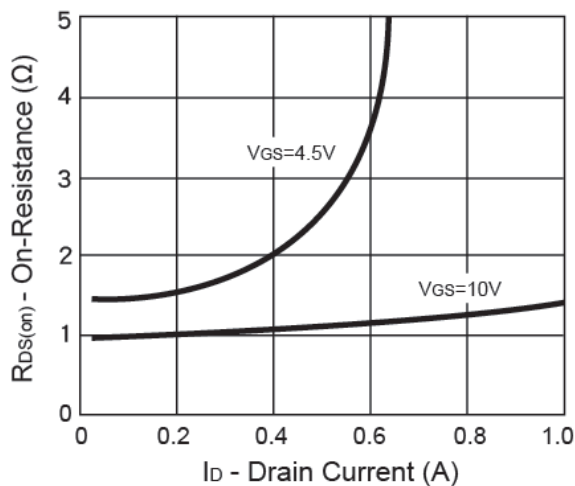
Output Characteristics



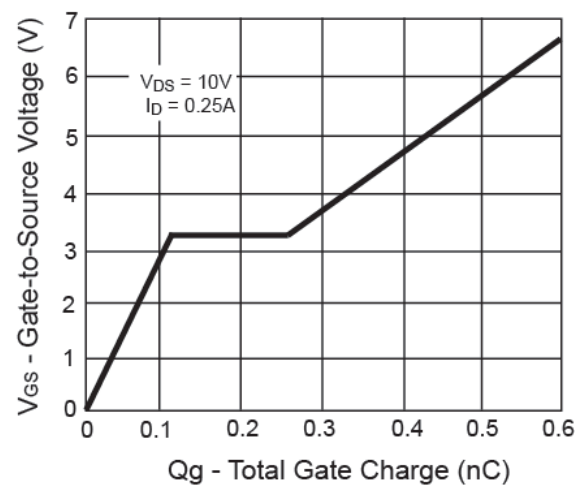
Transfer Characteristics



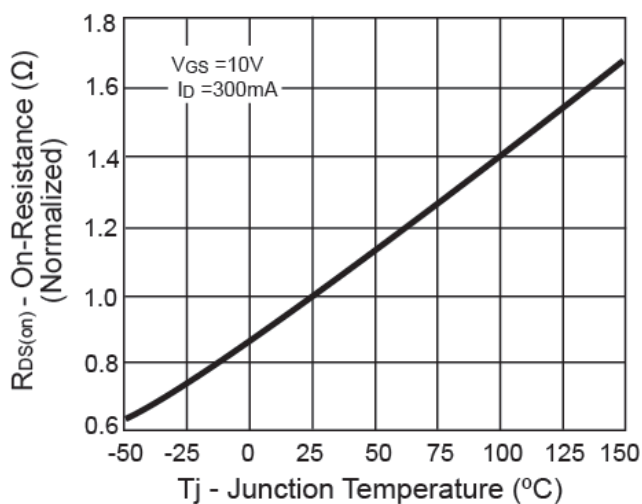
On-Resistance vs. Drain Current



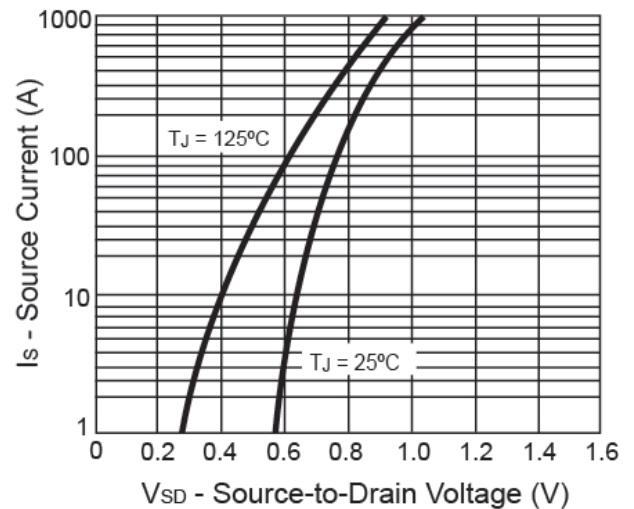
Gate Charge



On-Resistance vs. Junction Temperature



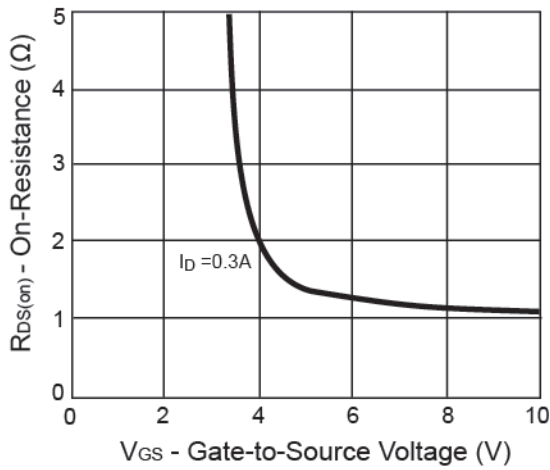
Source-Drain Diode Forward Voltage



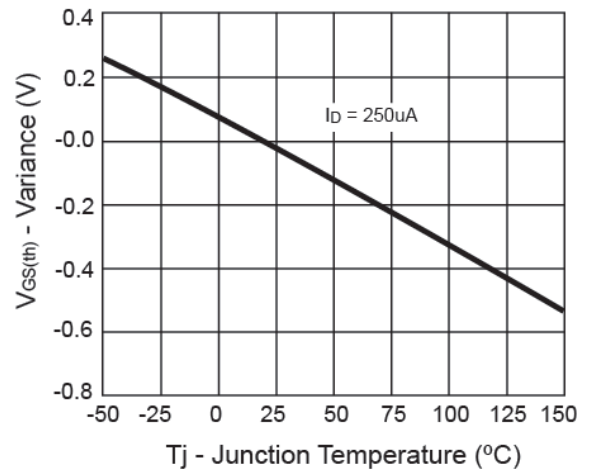
CHARACTERISTICS CURVES

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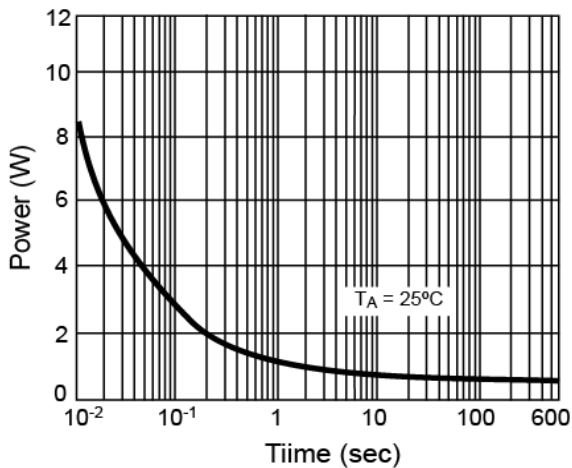
On-Resistance vs. Gate-Source Voltage



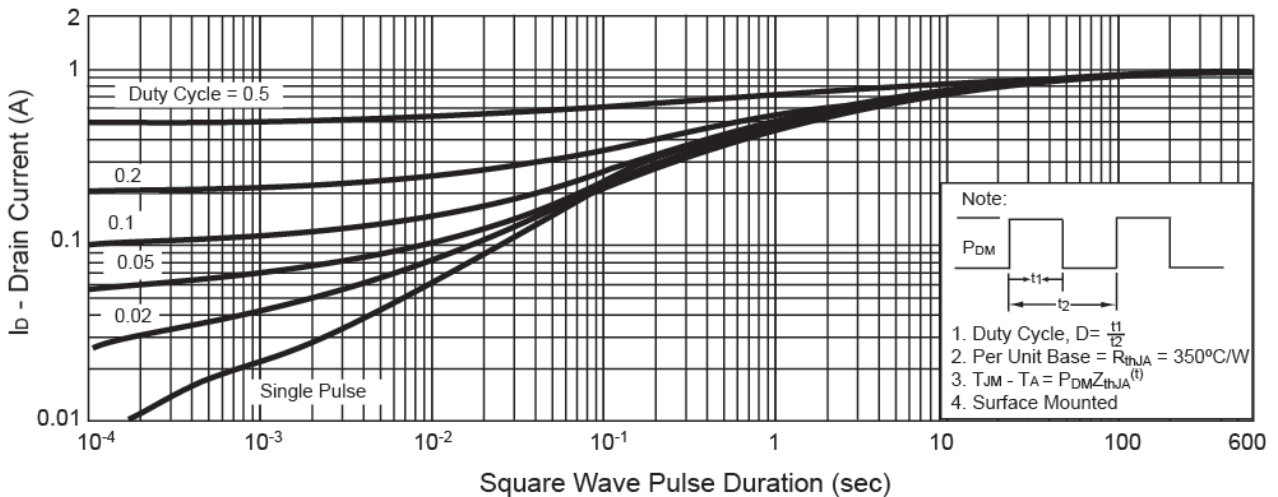
Threshold Voltage



Single Pulse Power

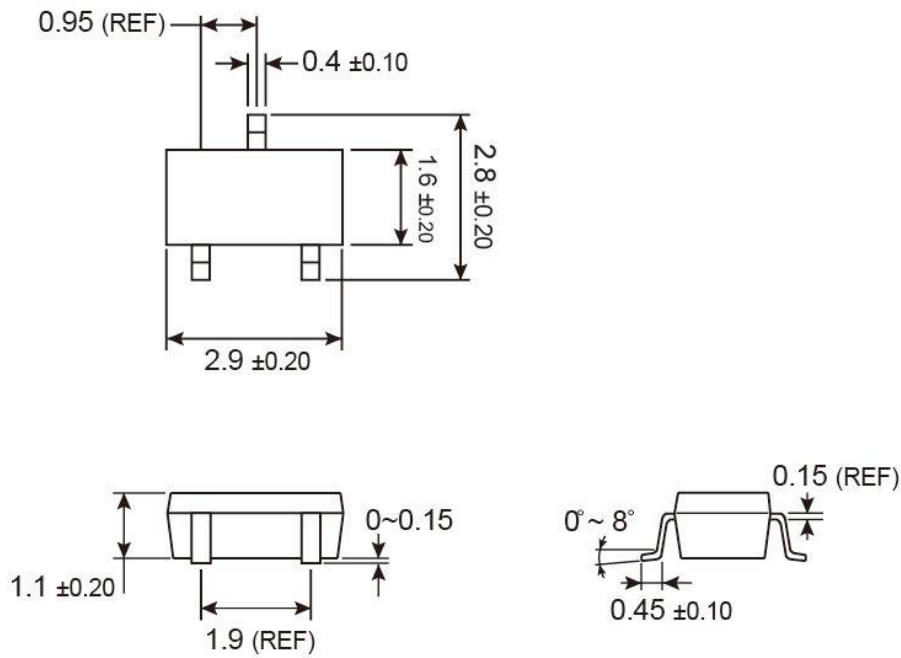


Normalized Thermal Transient Impedance, Junction-to-Ambient

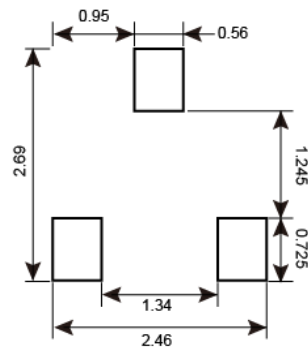


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

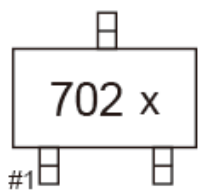
SOT-23



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



702 = TSM2N7002KCX Device Code
X = Internal Code

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