

MC14585B

4-Bit Magnitude Comparator

The MC14585B 4-Bit Magnitude Comparator is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit has eight comparing inputs (A3, B3, A2, B2, A1, B1, A0, B0), three cascading inputs (A < B, A = B, and A > B), and three outputs (A < B, A = B, and A > B). This device compares two 4-bit words (A and B) and determines whether they are “less than”, “equal to”, or “greater than” by a high level on the appropriate output. For words greater than 4-bits, units can be cascaded by connecting outputs (A > B), (A < B), and (A = B) to the corresponding inputs of the next significant comparator. Inputs (A < B), (A = B), and (A > B) on the least significant (first) comparator are connected to a low, a high, and a low, respectively.

Applications include logic in CPU's, correction and/or detection of instrumentation conditions, comparator in testers, converters, and controls.

Features

- Diode Protection on All Inputs
- Expandable
- Applicable to Binary or 8421-BCD Code
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range
- Can be Cascaded – See Figure 3
- These Devices are Pb-Free and are RoHS Compliant
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable*

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage Range	V _{DD}	-0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	V _{in} , V _{out}	-0.5 to V _{DD} + 0.5	V
Input or Output Current (DC or Transient) per Pin	I _{in} , I _{out}	±10	mA
Power Dissipation per Package (Note 1)	P _D	500	mW
Ambient Temperature Range	T _A	-55 to +125	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C
Lead Temperature (8-Second Soldering)	T _L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating: Plastic “P and D/DW”

Packages: - 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

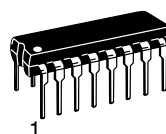
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



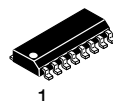
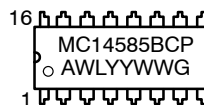
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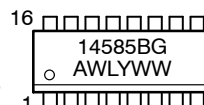
MARKING DIAGRAMS



PDIP-16
P SUFFIX
CASE 648



SOIC-16
D SUFFIX
CASE 751B



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Package

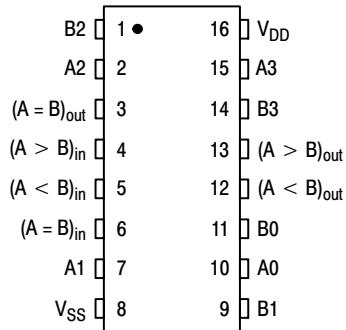
ORDERING INFORMATION

Device	Package	Shipping†
MC14585BCPG	PDIP-16 (Pb-Free)	500 Units / Rail
MC14585BDG	SOIC-16 (Pb-Free)	48 Units / Rail
MC14585BDR2G	SOIC-16 (Pb-Free)	2500/Tape & Reel
NLV14585BDR2G*	SOIC-16 (Pb-Free)	2500/Tape & Reel

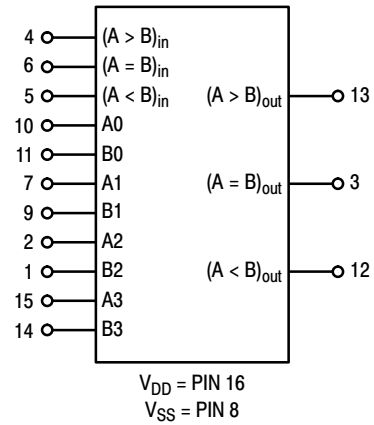
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PIN ASSIGNMENT



BLOCK DIAGRAM



TRUTH TABLE (x = Don't Care)

Inputs							Outputs		
Comparing			Cascading						
A3, B3	A2, B2	A1, B1	A0, B0	A < B	A = B	A > B	A < B	A = B	A > B
A3 > B3	x	x	x	x	x	x	0	0	1
A3 = B3	A2 > B2	x	x	x	x	x	0	0	1
A3 = B3	A2 = B2	A1 > B1	x	x	x	x	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 > B0	x	x	x	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	0	x	0	0	1
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	1	x	0	1	0
A3 = B3	A2 = B2	A1 = B1	A0 = B0	1	0	x	1	0	0
A3 = B3	A2 = B2	A1 = B1	A0 = B0	1	1	x	1	1	0
A3 = B3	A2 = B2	A1 = B1	A0 < B0	x	x	x	1	0	0
A3 = B3	A2 = B2	A1 < B1	x	x	x	x	1	0	0
A3 = B3	A2 < B2	x	x	x	x	x	1	0	0
A3 < B3	x	x	x	x	x	x	1	0	0

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (Note 2)	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0	"0" Level V _{OL}	5.0	-	0.05	-	0	0.05	-	0.05	Vdc	
		10	-	0.05	-	0	0.05	-	0.05		
		15	-	0.05	-	0	0.05	-	0.05		
	"1" Level V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	-	4.95	5.0	-	4.95		-
			10	9.95	-	9.95	10	-	9.95		-
			15	14.95	-	14.95	15	-	14.95		-
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	"0" Level V _{IL}	5.0	-	1.5	-	2.25	1.5	-	1.5	Vdc	
		10	-	3.0	-	4.50	3.0	-	3.0		
		15	-	4.0	-	6.75	4.0	-	4.0		
	"1" Level (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	-	3.5	2.75	-	3.5		-
			10	7.0	-	7.0	5.50	-	7.0		-
			15	11	-	11	8.25	-	11		-
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-3.0	-	-2.4	-4.2	-	-1.7	-	mAdc	
		5.0	-0.64	-	-0.51	-0.88	-	-0.36	-		
		10	-1.6	-	-1.3	-2.25	-	-0.9	-		
	Sink I _{OL}	15	5.0	0.64	-	0.51	0.88	-	0.36		-
			10	1.6	-	1.3	2.25	-	0.9		-
			15	4.2	-	3.4	8.8	-	2.4		-
Input Current	I _{in}	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	μAdc	
Input Capacitance (V _{in} = 0)	C _{in}	-	-	-	-	5.0	7.5	-	-	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	-	5.0	-	0.005	5.0	-	150	μAdc	
		10	-	10	-	0.010	10	-	300		
		15	-	20	-	0.015	20	-	600		
Total Supply Current (Notes 3, 4) (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0 10 15	I _T = (0.6 μA/kHz) f + I _{DD} I _T = (1.2 μA/kHz) f + I _{DD} I _T = (1.8 μA/kHz) f + I _{DD}						μAdc		

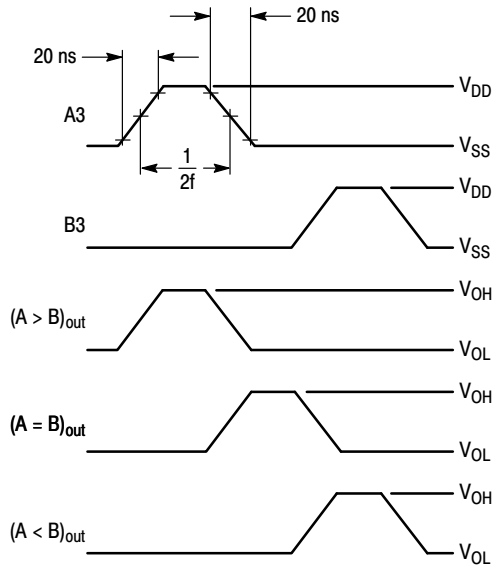
2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF: I_T(C_L) = I_T(50 pF) + (C_L - 50) Vfk where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V _{DD}	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time t _{TLH} , t _{THL} = (1.5 ns/pF) C _L + 25 ns t _{TLH} , t _{THL} = (0.75 ns/pF) C _L + 12.5 ns t _{TLH} , t _{THL} = (0.55 ns/pF) C _L + 9.5 ns	t _{TLH} , t _{THL}	5.0	-	100	200	ns
		10	-	50	100	
		15	-	40	80	
Turn-On, Turn-Off Delay Time t _{PLH} , t _{PHL} = (1.7 ns/pF) C _L + 345 ns t _{PLH} , t _{PHL} = (0.66 ns/pF) C _L + 147 ns t _{PLH} , t _{PHL} = (0.5 ns/pF) C _L + 105 ns	t _{PLH} , t _{PHL}	5.0	-	430	860	ns
		10	-	180	360	
		15	-	130	260	

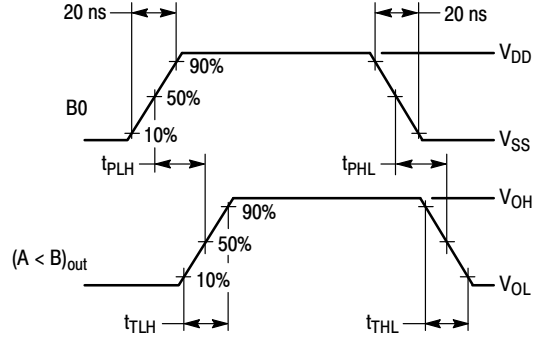
5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

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Inputs (A>B) and (A=B) high, and inputs B2, A2, B1, A1, B0, A0 and (A<B) low.
f in respect to a system clock.

Figure 1. Dynamic Power Dissipation Signal Waveforms



Inputs (A>B) and (A=B) high, and inputs B3, A3, B2, A2, B1, A1, A0, and (A<B) low.

Figure 2. Dynamic Signal Waveforms

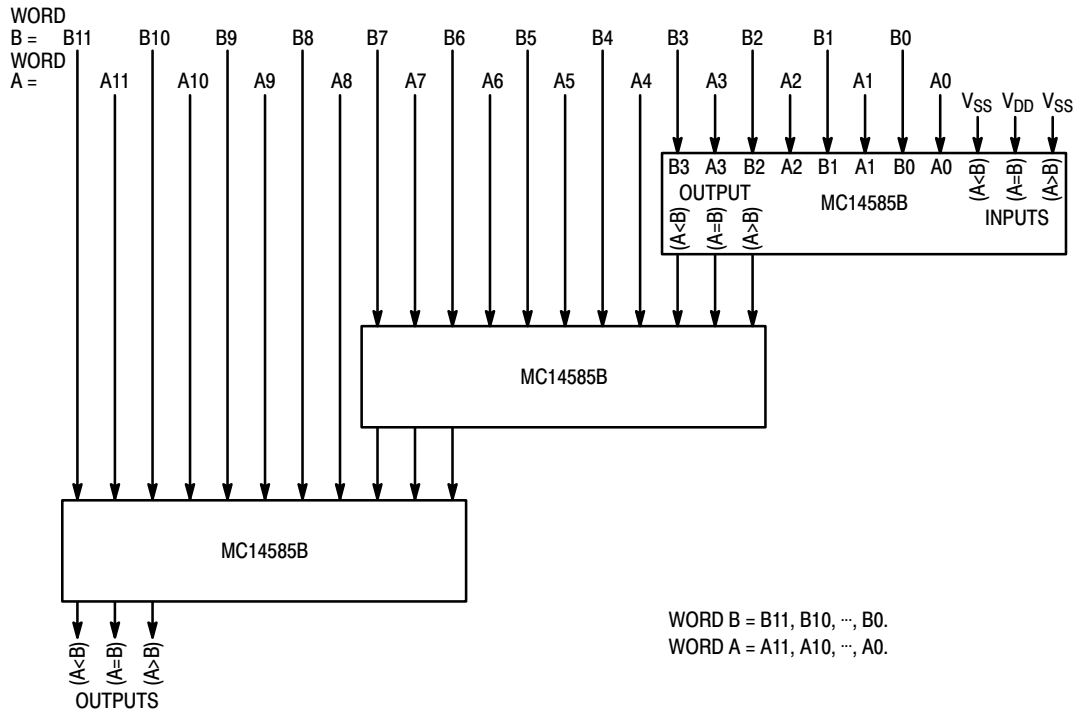
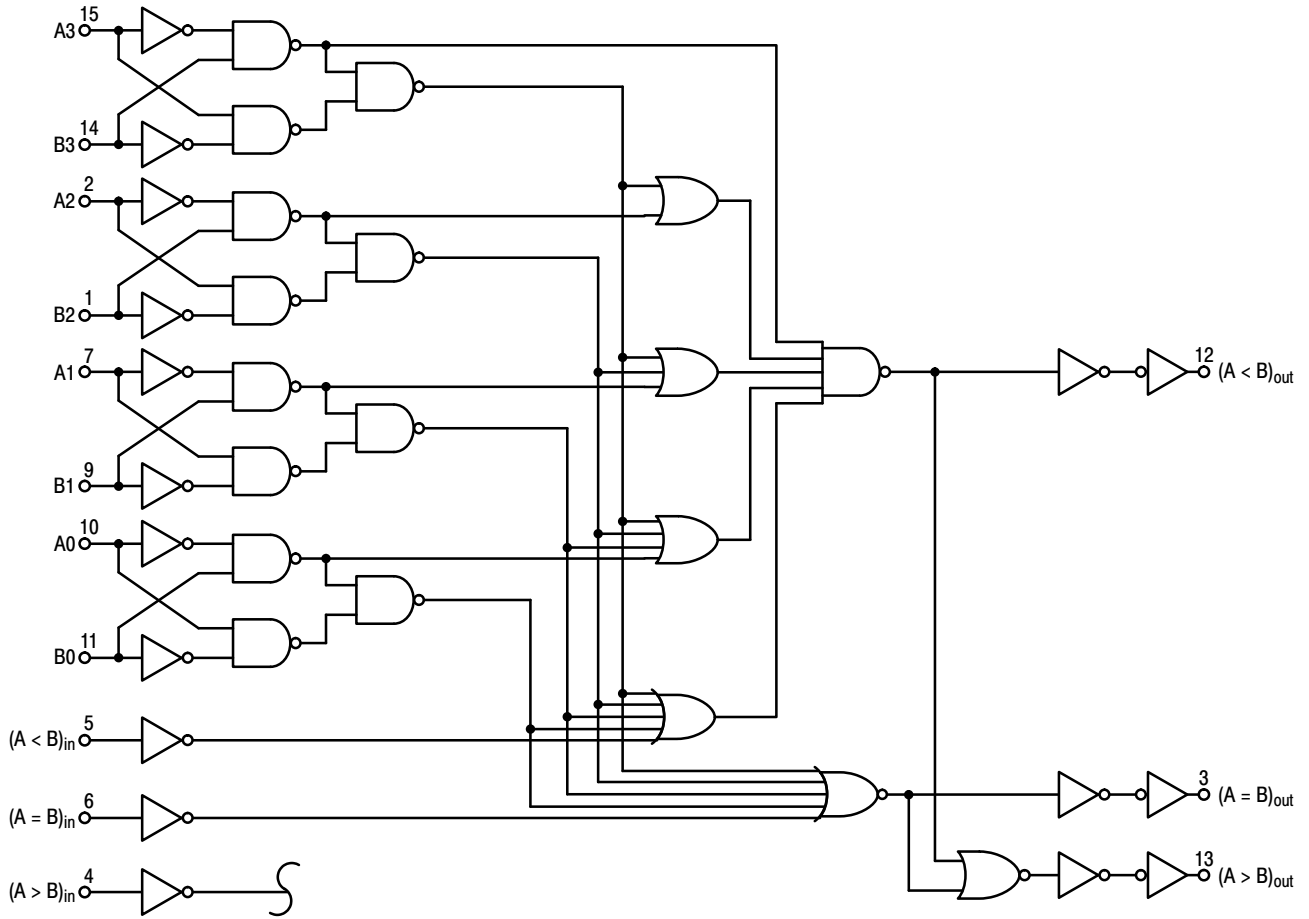


Figure 3. Cascading Comparators

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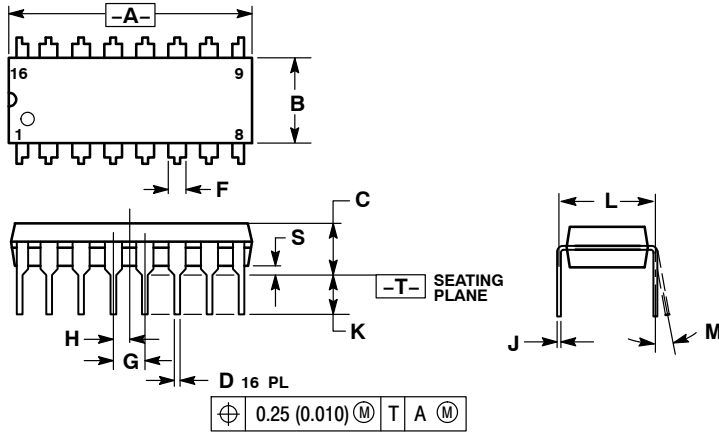
LOGIC DIAGRAM



MC14585B

PACKAGE DIMENSIONS

PDIP-16
CASE 648-08
ISSUE T



NOTES:

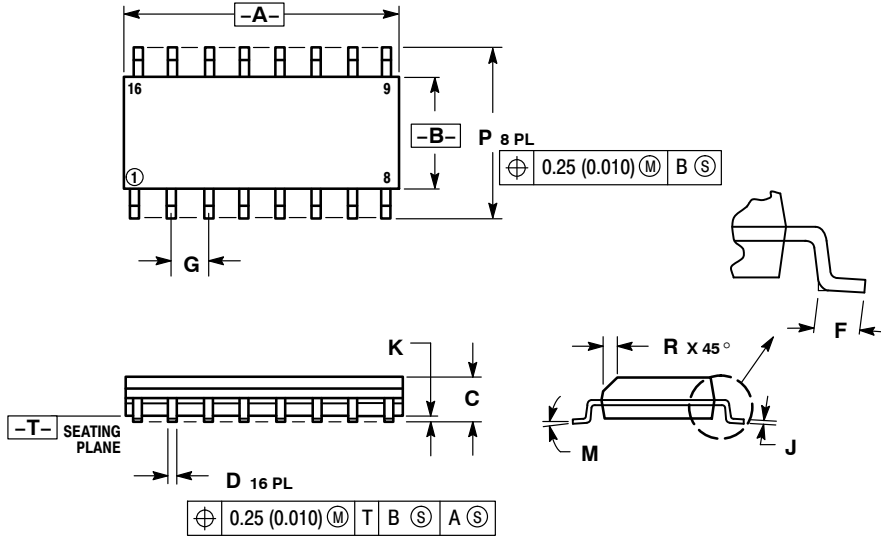
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 [°]	10 [°]	0 [°]	10 [°]
S	0.020	0.040	0.51	1.01

MC14585B

PACKAGE DIMENSIONS

SOIC-16
CASE 751B-05
ISSUE K

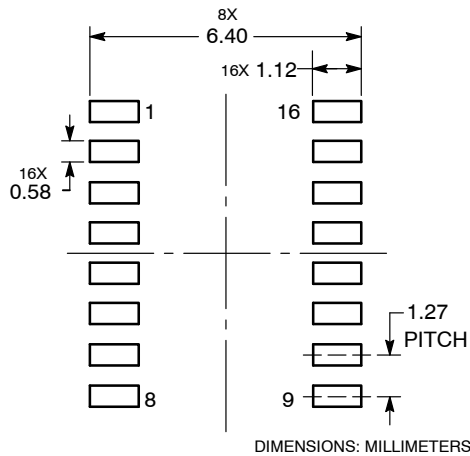


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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