
AG8888

Call Waiting Decoder

**Product
Specification**

DOC. VERSION 1.1

ELAN MICROELECTRONICS CORP.


June 2006



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Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial version	2000/08/08
1.1	Correct the table of DC ELECTRICAL CHARACTERISTIC	2006/06/01

I. GENERAL DESCRIPTION

This is a Call Waiting decoder used on the telephone. Call Waiting service works by alerting a customer engaged in a telephone call to a new incoming call. Thus, the customer can still receive important calls while engaged in a current call. The Call Waiting decoder can detect dual-tone (2130Hz and 2750Hz) alert tone and generate a valid timing on the data pins for micro controller.

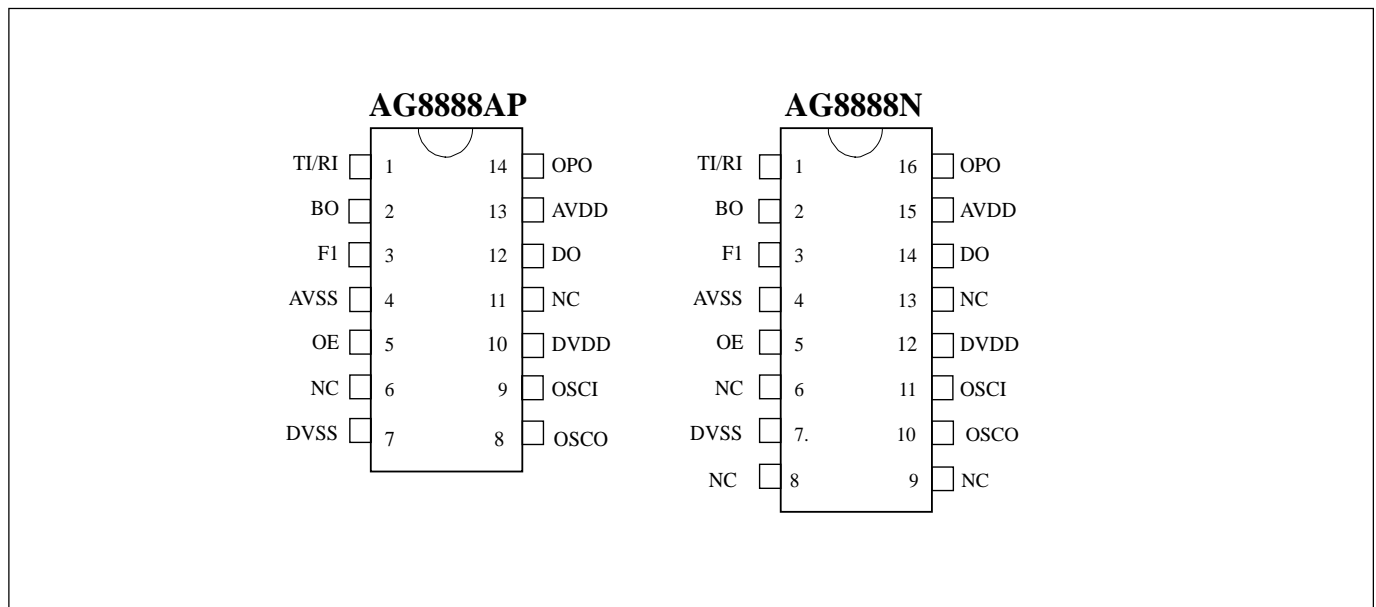
II. FEATURES

- Compatible with Bellcore special report SR-TSV-002476
- 3.6V ~ 6.0V supply voltage
- Call-Waiting (2130Hz plus 2750Hz) alert tone detector
- Sensitivity compensated by adjusting OP Amp
- Internal buffer
- Detection block for alert tone detected and digital algorithm detection
- Package series --- 14-pin DIP or 16-pin SOP (150 mil)
AG8888AP for 14-pin DIP
AG8888N for 16-pin SOP (150 mil)

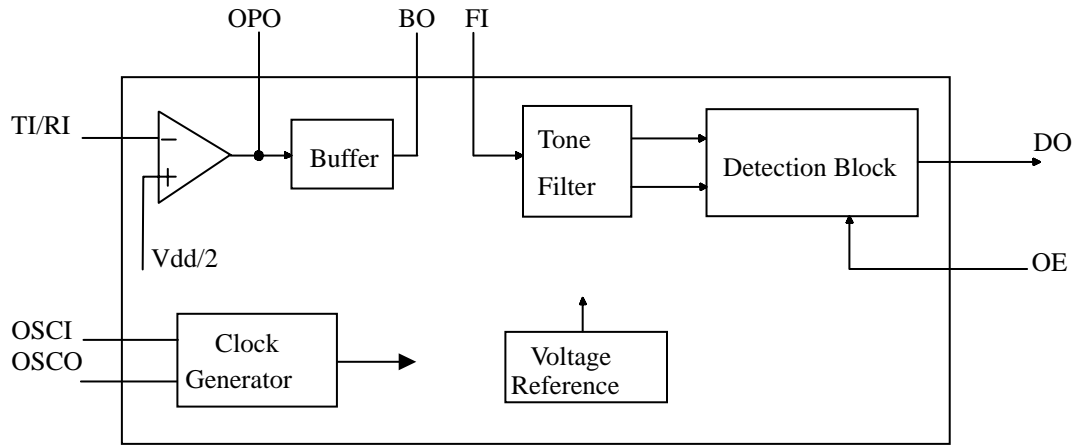
III. APPLICATION

Feature phones, cordless phones and stand-alone product

IV. PIN CONFIGURATION



V. FUNCTIONAL BLOCK DIAGRAM



VI. PIN DESCRIPTIONS

Pin	I/O	Description
TI/RI	I	Tip in or Ring in should be connected with twisted pair
OE	I	Output enable for alert tone detected. High is enable. Low is for factory test.
OSCI	I	480KHz crystal in
OSCO	O	480KHz crystal out
DO	O	Alert tone detected output. Normal low. Under OE pin set to high, when call waiting alert tone is detected, this pin goes to high.
OPO	O	Output of OP Amp
BO	O	Internal buffer output
FI	I	Band pass filter input
AVDD		Analog power.
DVDD		Digital power.
AVSS		Analog Ground.
DVSS		Digital Ground.
NC		Non connected

VII. FUNCTIONAL DESCRIPTIONS

Call Waiting service works by alerting a customer engaged in a telephone call to a new incoming call. Thus, the customer can still receive important calls while engaged in a current call. The call waiting decoder can detect alert tone (Call-Waiting Alerting Signal 2130Hz plus 2750Hz) and generate a valid timing on the data pins.

The call waiting decoder is designed to support the Caller Number Deliver feature, which is offered by regional Bell Operating Companies. The call waiting decoder has four blocks, including OP Amp, band pass filter, and detection block.

In a typical application, this IC receives Tip/Ring signals from twisted pairs. The signals as inputs of single-ended pre-amplifier (OP Amp and Buffer Amp), and the amplifier sends input signal to a band pass filter. Once the

signal is filtered, the detection block decodes the information and sends a valid timing to DO pin. The output data made available at DO pin. There is a OE pin to control DO pin's output enable.

There is an external clamp circuit between internal buffer amplifier and filter. In order to get great alert tone detection and avoid false triggering while speech signal is coming, the external clamp circuit can restrict speech signal to (0.6Vp-p from TIP/RING).

The input signal is call waiting alert tone signals. The DO pin is normal low. When OE pin set to high and this IC detects 2130Hz and 2750Hz frequency, then DO pin goes to high. Because OE pin set to low be for factory test, you should notice that the users don't set it to low.

For this decoder, we put some external elements for performance concern.

DC ELECTRICAL CHARACTERISTIC

VDD=5V, Vss=0V, Ta=25°C, fOSC=480KHz

Sym.	Description	Condition	Min.	Typ.	Max.	Unit
VDD	operating supply voltage		3.6		6	V
IDD	operating supply current			3.3	5	mA
VIL	low level input voltage				1.5	V
VIH	high level input voltage		3.5			V
VOL	low level output voltage	load=1mA		0.4		V
VOH	high level output voltage	load=1mA		4.6		V

- Note:
- 1.both tones in the composite signal have equal amplitude.
 - 2.tone pair is deviated by 0.5%.
 - 3.addes a 0.1uf capacitor between Power and Ground.

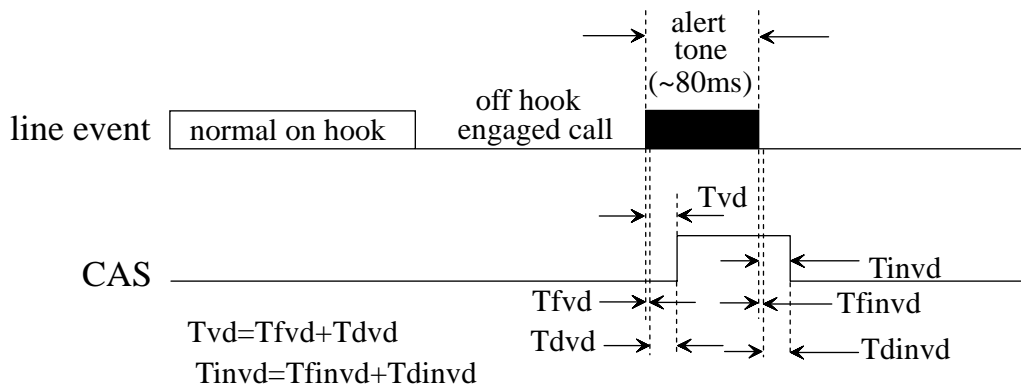
AC ELECTRICAL CHARACTERISTIC

(VDD=+5V,Ta=+25°C)

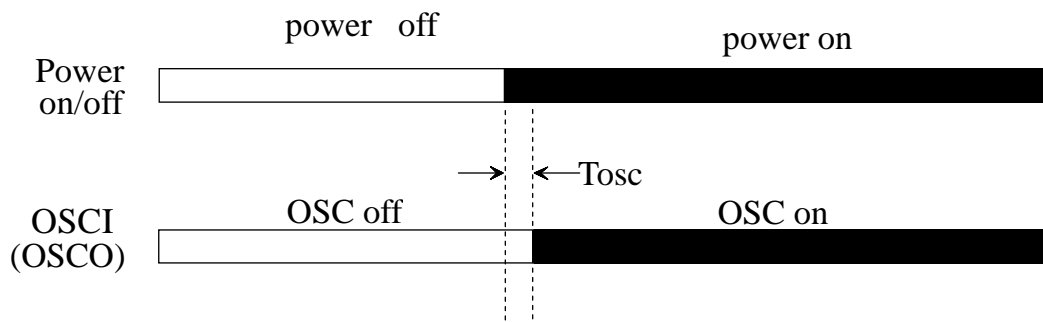
CHARACTERISTIC	Min.	Typ.	Max.	Unit
Input sensitivity ,VDD=+5V, Input G=1		-36		dBm
Input frequency tolerance for 2130Hz		±1.2		%
Input frequency tolerance for 2750Hz		±1.2		%

WAVE FORM TIMING

DO timing:



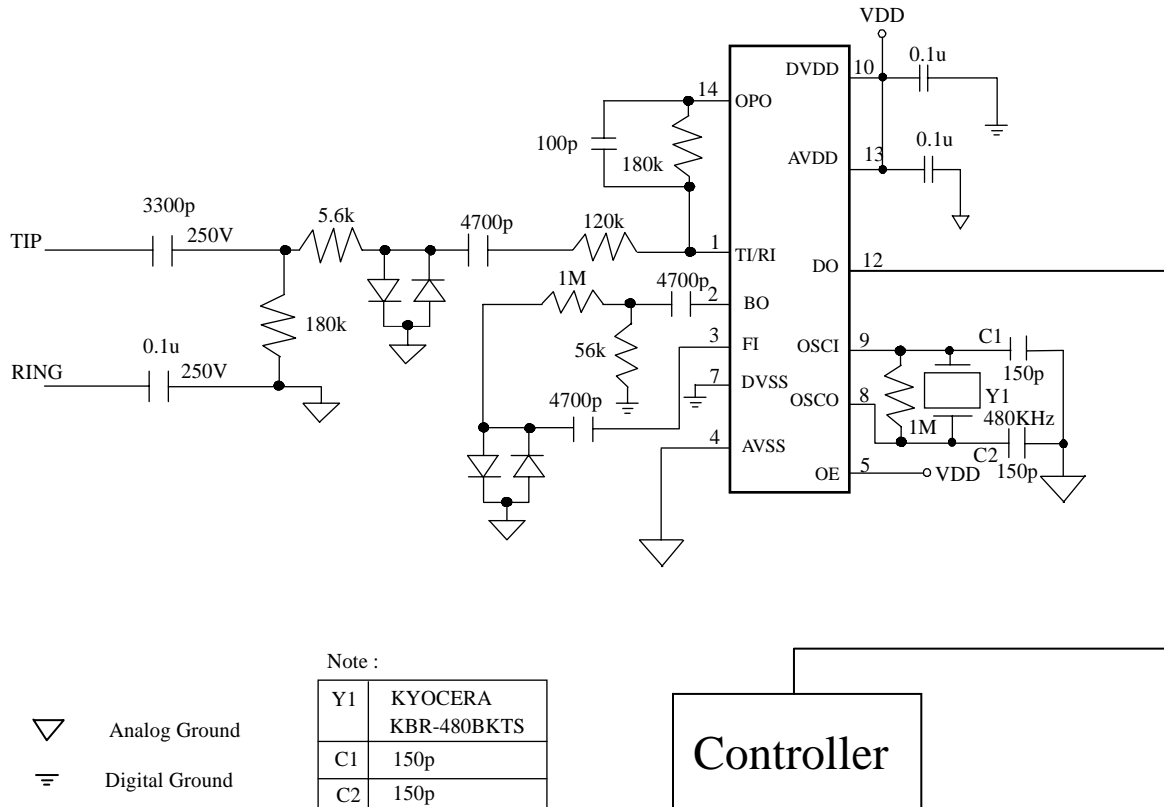
OSC timing:



Sym.	Description	Min.	Typ.	Max.	Unit
Tfvd	filter output signal valid delay		6		ms
Tfinvd	filter output signal invalid delay		6		ms
Tdvd	digital delay of valid signal		36		ms
Tdinvd	digital delay of invalid signal		20		ms
Tvd	total delay of valid signal		42		ms
Tinvd	total delay of invalid signal		26		ms
alert tone	input alert tone length (2130 ,2750 Hz @ -20dBm)		80		ms
Tosc	Oscillator enable delay time			10	ms

Note: detected alert tone length shown above is assumed that no speech signals input.
This test is under alert tone signal = -22dBm (600Ω)

APPLICATION CIRCUIT



Note :

Y1	KYOCERA KBR-480BKTS
C1	150p
C2	150p

- Analog Ground
- Digital Ground

Controller

APPLICATION NOTE

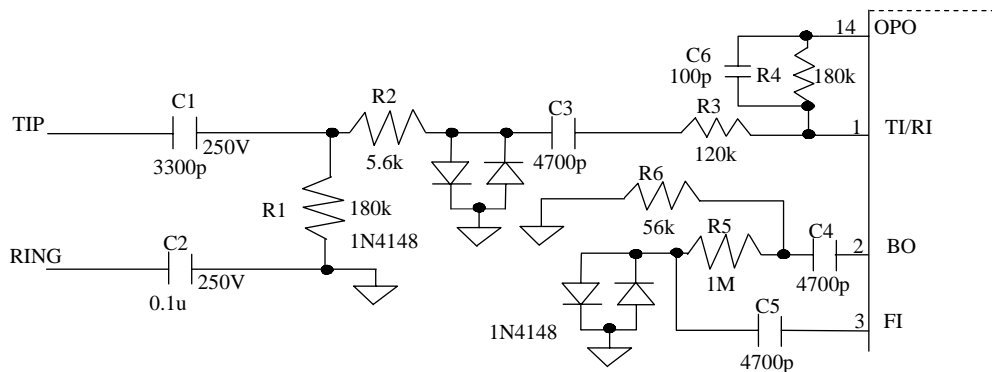
1. VDD, GND

To reduce noise effects, separate the analog and digital systems close to the device. For both the digital and analog VDD pins, use a ceramic capacitor of about 0.1uF set as close as possible to the pin to bypass to the respective GND's.

2. OE pin

Always connect OE to VDD for normal use.

3.



In the application circuit above, some of the external element values are crucial. C2 value could not be less than 0.1uF. R2 = 5.6k is proper and you had better not to change it. The diode has to use Si type diode for noise consideration.

There are an OP Amp. External resistors R3 and R4 can adjust the gain of OP Amp. The gain for OP Amp = $-R4/R3$.

4. OPO pin

This pin is the gain adjustment of OP Amp. See the partial application above. For high frequency noise immunity, the user can connect a 100pF capacitor between TI/RI pin and OPO pin.

5. OSCI pin, OSCO pin

The clock generator input XIN pin and output XOUT need to connect a feedback resistor 1M(between them for proper operation.

6. About latch up

It is necessary that AVDD and DVDD pins be the common source of power supply. This is to avoid latch up due to the voltage difference between AVDD and DVDD pins when power is ON.