成越科技股份有限公司
Cheng Yue Technology Inc.

DigiTron Technology Limited
迪創科技有限公司

CY2890-AFB, CY2890-BFA.

Digital TFT-LCD Panel Timing Controller

Resolution : 800x480, 640x480, 800x600, 1024x600
1024x768, 720x480, 320x240, 480x272

香港九龍觀塘駿業里10號業運工業大廈8樓F室
Unit F, 8/F., Yip Win Flactory Building, 10 Tsun Yip Lane, Kwun Tong
Tel: (852) 2781 3231 Fax: (852) 2781 3238
深圳热线：13554946866 QQ：393298913
Email: whj6666@126.com MSN: t-con2010@hotmail.com

Revision History

Version	DATE	Description
1.5	2007/09/15	Preliminary Datasheet

Ordering Information

Part No.	Package	Descriptions
CY2890-AFB	64pin LQFP, Green package	Outline as 10x10x1.4 mm , Default resolution as 800x480
CY2890-BFA	64pin LQFP, Green package	Outline as 10x10x1.4 mm , Default resolution as 800x600

Content

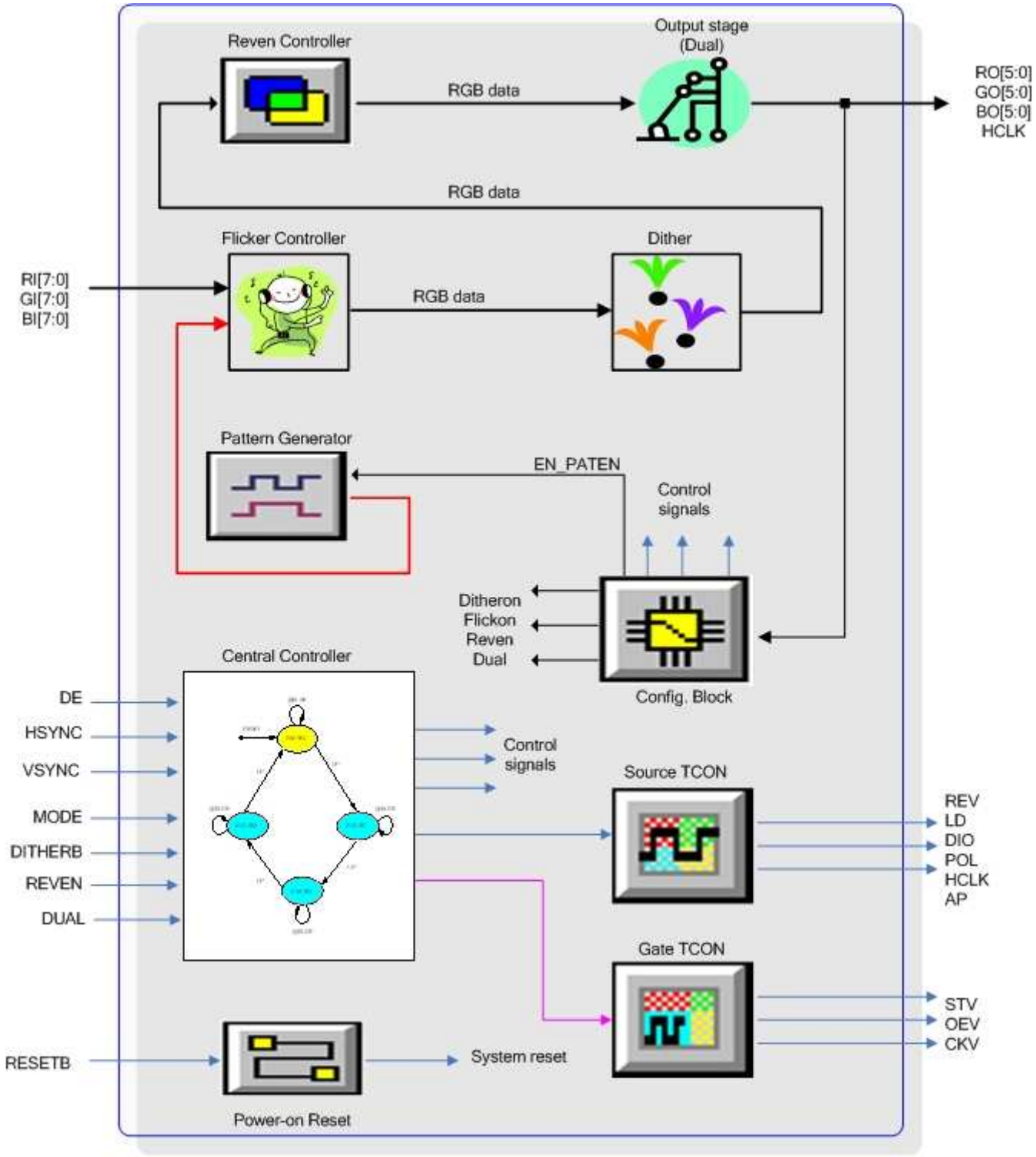
1. General Description

The CY2890- AFB and BFA are digital TFT-LCD timing controllers with built-in “dithering”, “reverse”, “dual”, “flicker”, “AP” and “pattern generator” functions. The input signal is digital R/G/B with HSYNC/VSYNC or DE. User can use the MODE pin to select input signal to be either HSYNC mode or DE mode. The R/G/B input is fixed to 8 bits data width and the output is always 6 bits. The convert from 8 bits RGB to 6 bits RGB can be either directly truncated or dithering depends on the “DITHER” function is off or on. When DITHER is on, CY2890 will emulate 8 bits gray level on 6 bits RGB bus. The users will have a more vivid picture with dither function on. The “Reverse” function is designed for reducing EMI. The key is to lower down the R/G/B transition count. The “dual” function can set the output HCLK to latch the output data at both edges. Set “dual” on can lower down the HCLK frequency to half. With the “Reverse” and “dual” functions, the board level system design can be relaxed. We also have a built-in test pattern generator for users to do a quick final test or aging burning test. The built-in test pattern generator has 24 very popular patterns. It will be free running when MODE = 1, HSYNC = 1 or MODE = 0, DE = 1. You can stop the free-running built-in test pattern at any time. The “flicker” function is used to reduce the flicker phenomenon. For CY2890-AFB and BFA the default panel resolutions are fixed, but they can be changed by external strap resistors. We support 8 different panel resolutions, which can be selected by external strap resistors. Through CY2890, all the necessary horizontal and vertical control signals to TFT-LCD are handled automatically. This includes the polarity invert control. There is a built-in power-on reset circuit in the chip, no need for user to add external reset circuit. If users want to extend the power-on reset, an external capacitor can be added.

2. Features

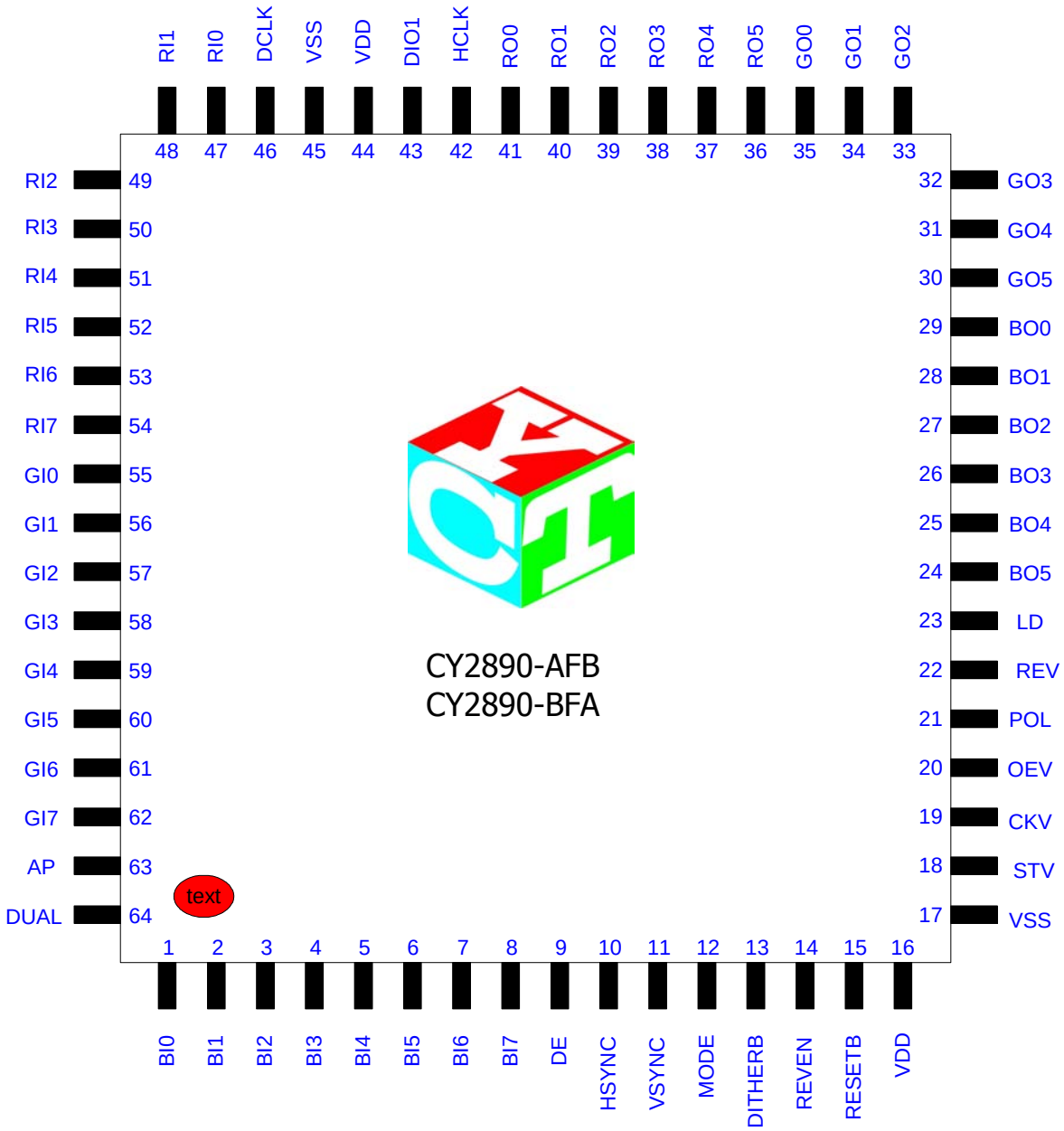
- Supporting 8 kinds of different digital TFT-LCD panels
  800 x 480 , 640 x 480, 800 x 600, 1024 x 600, 1024 x 768, 720 x 480,320 x 480, 480 x 272
  CY2890- AFB default is 800 x 480
  CY2890-BFA default is 800 x 600
- Support HSYNC mode or DE mode
- Advanced 16.7M colors Dither function
- FLICKER reduction function
- Support DUAL edge function
- Support REVERSE function
- Support AP function
- Built-in test pattern generator with 24 popular patterns
- Built-In Power-On reset circuit
- Built-in polarity inverted function
- Provide source and gate drivers control timing
- Master clock frequency: 75 MHz max.
- Single supply voltage : +3.0V to +3.6V
- Wide temperature operation range -40°C / +95°C
- ESD meet class3 critera
  HBM 4KV, MM 400V, LATCH-UP 100mA
- 64 LQFP Green Package

3. Block Diagram



CY2890-AFA/AFB/AFC/BFA Block Diagram

4. Pin Assignment



5. Pin Description

Pin No.	Symbol	I/O	Description	Internal
1	BI0	I	Blue color data input, bit0 (LSB)	pull-down
2	BI1	I	Blue color data input, bit1	pull-down
3	BI2	I	Blue color data input, bit2.	
4	BI3	I	Blue color data input, bit3.	
5	BI4	I	Blue color data input, bit4.	
6	BI5	I	Blue color data input, bit5.	
7	BI6	I	Blue color data input, bit6.	
8	BI7	I	Blue color data input, bit7 (MSB).	
9	DE / ENPG	I	MODE = H : Data enable signal input, active high MODE = L : enable built-in pattern generator when Set to High, Stop when set to Low.	pull-down
10	HSYNC / ENPG	I	MODE = L : Negative polarity horizontal sync input MODE = H : enable built-in pattern generator when Set to High, Stop when set to Low.	pull-down
11	VSYNC / TEST	I	Negative polarity vertical sync input When set to DE mode, this pin must be floating or connected to ground.	pull-down
12	MODE	I	DE / SYNC mode select H : DE mode L : SYNC mode	pull-up
13	DITHERB	I	Dithering function enable or disable setting H : disable L : enable	pull-up
14	REVEN	I	Data reverse function enable or disable H : enable L : disable	pull-down
15	RESETB	I	Active low system reset pin Set low will reset the CY2890.	pull-up
16	VDD	I	Power supply voltage.	
17	VSS	I	Power supply ground.	
18	STV	O	Gate driver start pulse.	
19	CKV	O	Gate driver shift clock.	
20	OEV	O	Gate driver output enable	
21	POL	O	Source driver polarity select	
22	REV	O	Source driver data reverse control.	
23	LD	O	Source driver latch pulse and output enable.	
24	BO5	O	Blue color data output, bit5 (MSB).	
25	BO4	O	Blue color data output, bit4.	
26	BO3	O	Blue color data output, bit3.	
27	BO2	O	Blue color data output, bit2.	
28	BO1	O	Blue color data output, bit1.	
29	BO0	O	Blue color data output, bit0 (LSB).	
30	GO5	O	Green color data output, bit5 (MSB).	

Pin No.	Symbol	I/O	Description	Internal
31	GO4	O	Green color data output, bit4.	
32	GO3	O	Green color data output, bit3.	
33	GO2	O	Green color data output, bit2.	
34	GO1	O	Green color data output, bit1.	
35	GO0	I/O	Green color data output, bit0 (LSB). Flicker on/off setting	
36	RO5	O	Red data output, bit5 (MSB).	
37	RO4	O	Red color data output, bit4.	
38	RO3	O	Red color data output, bit3	
39	RO2	I/O	Red color data output, bit2. Panel resolution select bit 2, RES[2],	
40	RO1	I/O	Red color data output, bit1. Panel resolution select bit 1, RES[1],	
41	RO0	I/O	Red color data output, bit0. Panel resolution select bit 0, RES[0],	
42	HCLK	O	Source driver clock	
43	DIO	O	Source driver start pulse	
44	VDD	I	Power supply voltage.	
45	VSS	I	Power supply ground.	
46	DCLK	I	Clock signal; latch input data at DCLK falling edge.	
47	RI0	I	Red color data input, bit0 (LSB)	pull-down
48	RI1	I	Red color data input, bit1.	pull-down
49	RI2	I	Red color data input, bit2.	
50	RI3	I	Red color data input, bit3.	
51	RI4	I	Red color data input, bit4.	
52	RI5	I	Red color data input, bit5.	
53	RI6	I	Red color data input, bit6.	
54	RI7	I	Red color data input, bit7 (MSB).	
55	GI0	I	Green color data input, bit0 (LSB)	pull-down
56	GI1	I	Green color data input, bit1	pull-down
57	GI2	I	Green color data input, bit2.	
58	GI3	I	Green color data input, bit3.	
59	GI4	I	Green color data input, bit4.	
60	GI5	I	Green color data input, bit5.	
61	GI6	I	Green color data input, bit6.	
62	GI7	I	Green color data input, bit7 (MSB).	
63	AP	O	AP out	
64	DUAL	I	DUAL function H : enable dual (double edge send out data) L : disable dual (single edge send out data)	pull-up

6. Function Description

CY2890 can support 8 different kind panel resolutions. To select different panel resolution users have to add an external pull-up resistors at pin39, 40 or 41. At power-on, CY2890 will read in pin39, 40 and 41 as RES[2:0].
In the table below, we mark “x” mean don’t do anything. We mark “pull-down” mean you have to add an external resistor to GND.

◆ Panel Select Table for CY2890-AFB

RES[2:0]				RESOLUTION	CONNECTED TO PIN EXTERNAL RESISTOR VALUE
Value	Pin39	Pin40	Pin41		
0	x	x	x	800x480	No Resistors
1	x	x	Pull-down	640x480	10K
2	x	Pull-down	X	800x600	10K
3	x	Pull-down	Pull-down	1024x600	10K
4	Pull-down	x	X	1024x768	10K
5	Pull-down	x	Pull-down	720x480	10K
6	Pull-down	Pull-down	x	320x240	10K
7	Pull-down	Pull-down	Pull-down	480x272	10K

◆ Panel Select Table for CY2890-BFA

RES[2:0]				RESOLUTION	CONNECTED TO PIN EXTERNAL RESISTOR VALUE
Value	Pin39	Pin40	Pin41		
0	x	x	x	800x600	No Resistors
1	x	x	Pull-down	640x480	10K
2	x	Pull-down	x	800x480	10K
3	x	Pull-down	Pull-down	1024x600	10K
4	Pull-down	x	x	1024x768	10K
5	Pull-down	x	Pull-down	720x480	10K
6	Pull-down	Pull-down	x	320x240	10K
7	Pull-down	Pull-down	Pull-down	480x272	10K

7. DC Characteristics

◆ Absolute maximum ratings

PARAMETER	SYMBOL	RATING	UNIT
Power supply	V_{DD}	2.5 to 3.8	V
Input voltage	V_{IN}	-0.3 to V_{DD} +0.3	V
Output voltage	V_{OUT}	-0.3 to V_{DD} +0.3	V
Storage temperature	T_{STG}	-40 to 125	℃

◆ Recommended operating conditions

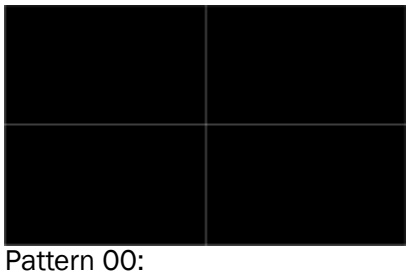
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Power supply	V_{DD}	3.0	3.3	3.6	V
Input voltage	V_{IN}	0	-	V_{DD}	V
Operating temperature	T_{OPR}	-40	-	95	℃

◆ DC Electrical characteristics

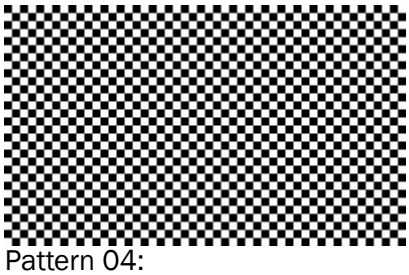
PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARK
Input low current	I_{IL}	No pull-up or pull-down	-1	-	1	μA	
Input high current	I_{IH}	No pull-up or pull-down	-1	-	1	μA	
Tri-state leakage current	I_{OZ}		-10	-	10	μA	
Logic input low voltage	V_{IL}	CMOS	-	-	$0.3V_{DD}$	V	Note 1
Schmitt input low voltage	V_{SIL}	CMOS	-	-	$0.3V_{DD}$	V	Note 2
Logic input high voltage	V_{IH}	CMOS	$0.7V_{DD}$	-	-	V	Note 1
Schmitt input high voltage	V_{SIH}	CMOS	$0.7V_{DD}$	-	-	V	Note 2
Output low voltage	V_{OL}	I_{OL} = 4mA	-	-	$0.3V_{DD}$	V	Note 3
Output high voltage	V_{OH}	I_{OH} = -4mA	$0.7V_{DD}$	-	-	V	Note 3
Output low voltage	V_{OL}	I_{OL} = 8mA	-	-	$0.3V_{DD}$	V	Note 4
Output high voltage	V_{OH}	I_{OH} = -8mA	$0.7V_{DD}$	-	-	V	Note 4
Input pull up / down resistance	R_I	V_{IL} = 0V or V_{IH} = V_{DD}	-	90	-	KΩ	Note 5

Note 1: MODE, RI0~RI7, GI0~GI7, BI0~BI7.
Note 2: DCLK, HSYNC, VSYNC, DE, RESETB
Note 3: CKV, POL, REV, LD, DIO, STV, OEV, AP, RO0~RO5, GO0~GO5, BO0~BO5.
Note 4: HCLK
Note 5: RESETB, HSYNC, VSYNC, DE, MODE, REVEN, DITHERB, DUAL, RI0, RI1, GI0, GI1, BI0, BI1

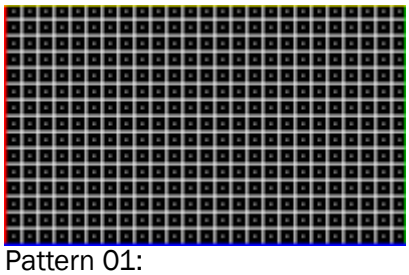
8. Built-in Patterns



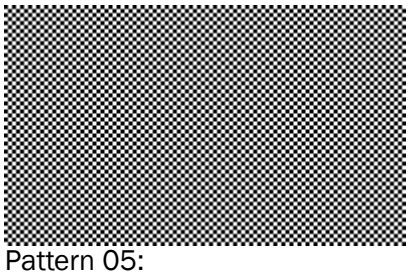
Pattern 00:
Black with white cross line,
White line boundary.



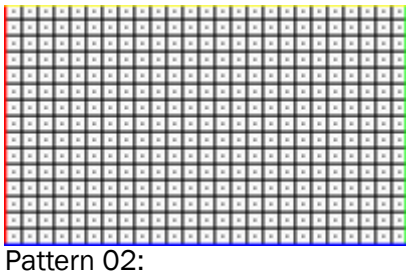
Pattern 04:
Black and white checkerboard
four pixels



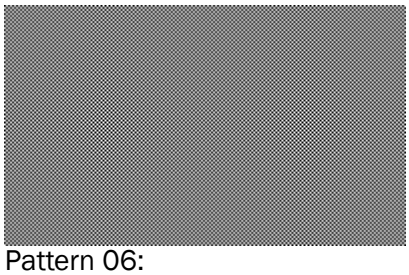
Pattern 01:
White cross hatch and dot
4 border lines



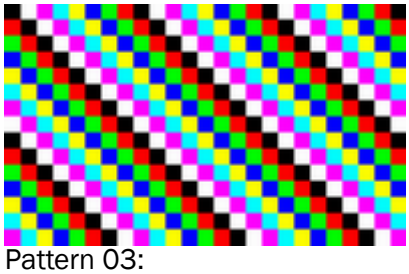
Pattern 05:
Black and white checkerboard
two pixels



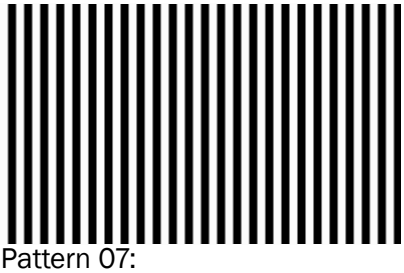
Pattern 02:
Black cross hatch and dot
4 border lines



Pattern 06:
Black and white checkerboard
one pixel and boundary

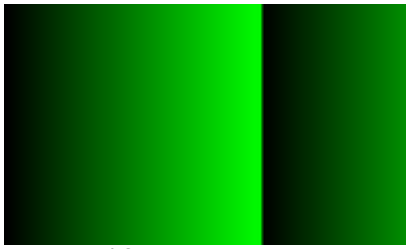


Pattern 03:
Diagonal color



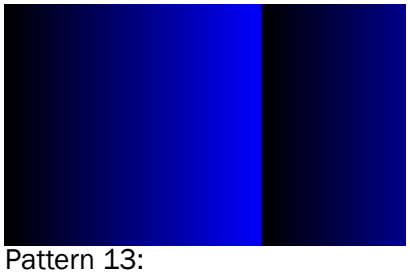
Pattern 07:
Vertical black and white bar.,
Coarse.

Pattern 08:
61,62 gray color, dither off
240~247 gray color, dither on

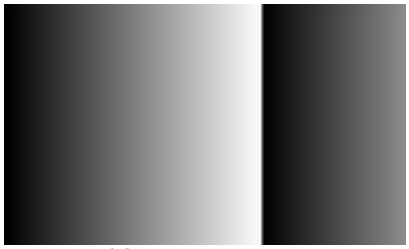


Pattern 12:
dither pattern for green

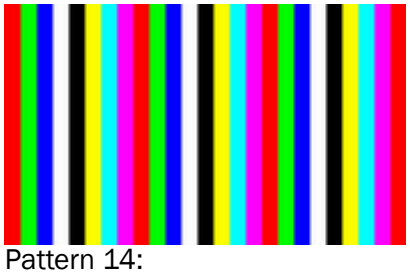
Pattern 09:
vertical gray 8 levels
64 pixels



Pattern 13:
dither pattern for blue



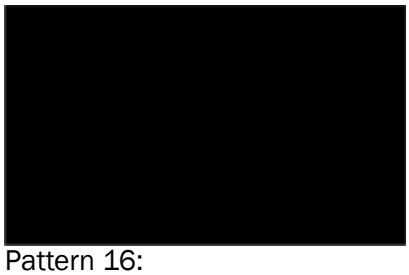
Pattern 10:
dither pattern for gray



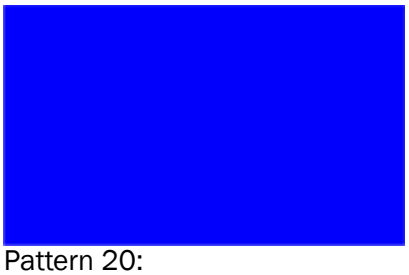
Pattern 14:
Vertical colors bar.

Pattern 11:
dither pattern for red

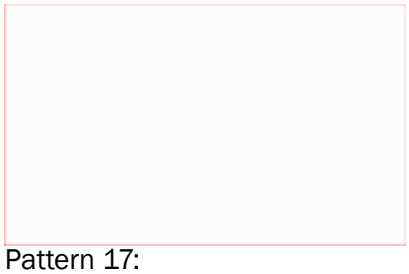
Pattern 15:
Horizontal colors bar.



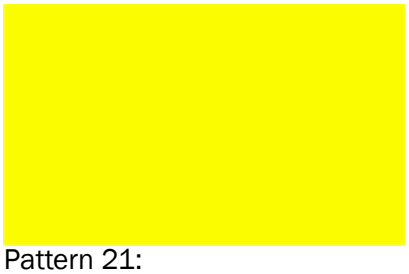
Pattern 16:
Black with white line boundary.



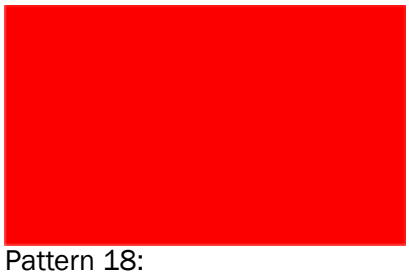
Pattern 20:
Blue with white line boundary.



Pattern 17:
White with red line boundary.

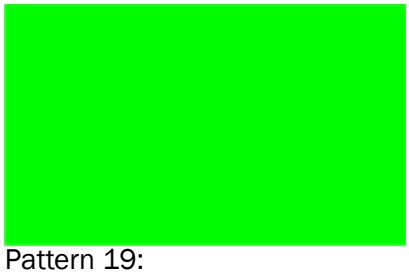


Pattern 21:
Yellow with white line boundary.



Pattern 18:
Red with white line boundary.

Pattern 22:
Magenta with white line boundary.

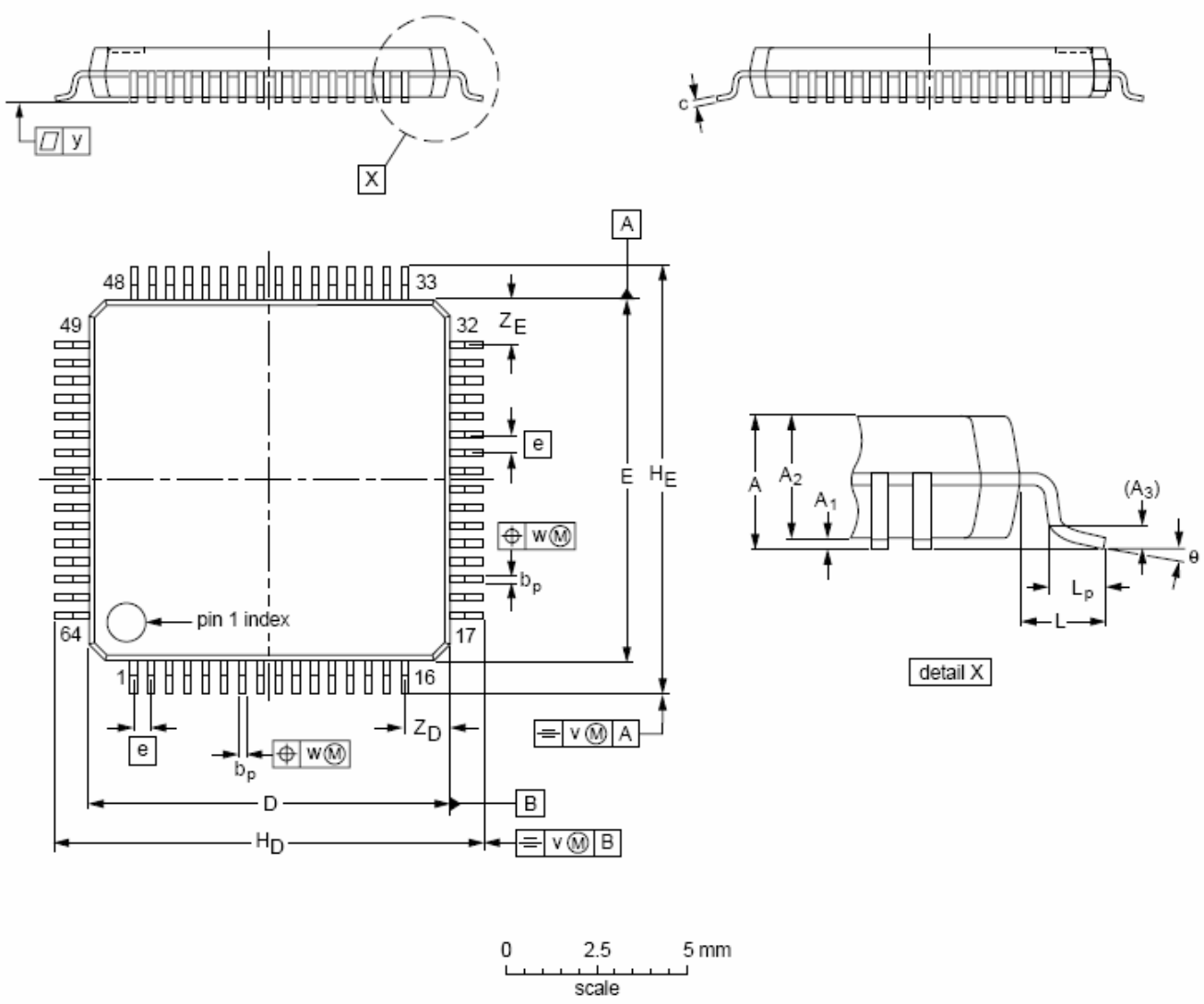


Pattern 19:
Green with white line boundary.

Pattern 23:
Cyan with white line boundary.

9. Package Information

LQFP-64 (10x10x1.4 mm)



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7° 0°