# 8 Port 10/100 Ethernet Integrated Switch

## *(Port Mirror, TCP/UDP QoS & VIP Port QoS)*

### Features

- Wide operating temperature range
  - IP178D LF (0°C to 70°C)
  - IP178D LFI (-40°C to 85°C)
- IP178C pin to pin compatible
- Support 2k MAC address
- Support auto-polarity for 10 Mbps
- Support filter/forward special DA option
- Support broadcast storm protection
- Auto MDI-MDIX option
- Two queues per port for QoS purposes
- Support Port based QoS
- Support 802.1p & DiffServ based QoS
- QoS
  - Port base
  - 802.1p
  - IP DiffServ IPV4/IPV6
  - TCP/UDP port number
  - Pins configure ports priority (VIP port)
- Support max forwarding packet length 1552/1536 bytes option
- Support port mirror function
- Support two dynamic fiber ports for Hot Plug
- Built in linear regulator control circuit
- Support Lead Free package (Please refer to the Order Information)
- 0.16um Process

### General Description

IP178D integrates an 8-port switch controller, SSRAM, and 8 10/100 Ethernet transceivers. Each of the transceivers complies with the IEEE 802.3, IEEE 802.3u, and IEEE 802.3x specifications. The transceivers are designed in DSP approach in 0.16um technology; they have high noise immunity and robust performance.

IP178D supports a lot of QoS function, including 802.1p, DiffServ, TCP/UDP port number and High priority port. User could enable QoS function from Pin or EEPROM.

IP178D also supports port mirror function for each port. User could monitor RX and TX port.

There are two fiber ports, port 6 and port 7, could be enable and disable from pin.

## Table of Contents

## Revision History

| Revision # | Change Description |
|---|---|
| IP178D-DS-R01 | Initial release |

## The difference in pin definition between IP178C/IP178CH and IP178D

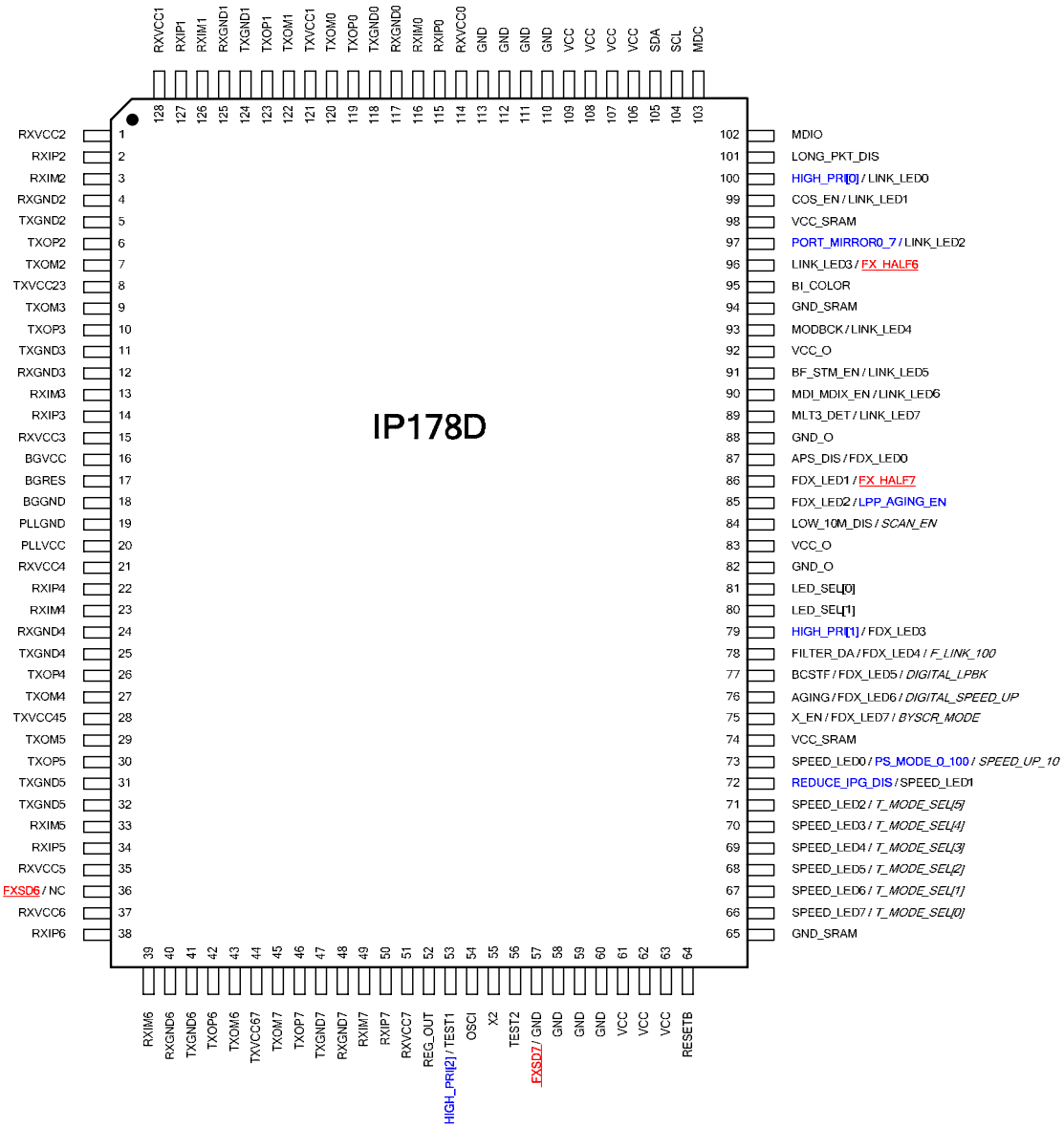
| Pin | IP178C/IP178CH | | | IP178D | | |
|---|---|---|---|---|---|---|
| | Function | Configure | Type | Function | Configure | Type |
| 36 | NC(IP178C)<br>FXSD6(IP178CH) | | | FXSD6 | | |
| 53 | TEST1 | EXTMII_EN | IPL | TEST1 | HIGH_PRI[2] | IPL |
| 56 | RXCLK | | IPH | TEST2 | | IPH |
| 57 | GND(IP178C)<br>FXSD7(IP178CH) | | | FXSD7 | | |
| 72 | SPEED_LED1 | RMII_MII | IPL | SPEED_LED1 | REDUCE_IPG_DIS | IPL |
| 73 | SPEED_LED0 | SCA_SEL | IPL | SPEED_LED0 | PS_MODE_0_100 | IPL |
| 75 | RXDV/FDX_LED7 | X_EN | IPH | FDX_LED7 | X_EN | IPH |
| 76 | RXD3/FDX_LED6 | AGING | IPH | FDX_LED6 | AGING | IPH |
| 77 | RXD2/FDX_LED5 | BCSTF | IPL | FDX_LED5 | BCSTF | IPL |
| 78 | RXD1/FDX_LED4 | FILTER_DA | IPL | FDX_LED4 | FILTER_DA | IPL |
| 79 | RXD0/FDX_LED3 | VLAN_ON | IPL | FDX_LED3 | HIGH_PRI[1] | IPL |
| 80 | TXEN | LED_SEL[1] | IPH | | LED_SEL[1] | IPH |
| 81 | TXD3 | LED_SEL[0] | IPH | | LED_SEL[0] | IPH |
| 84 | LOW_10M_DIS/<br>SCA_DIS | | IPH | LOW_10M_DIS | | IPH |
| 85 | TXD2/FDX_LED2 | FX7_EN<br>(for IP178CH only) | IPL | FDX_LED2 | LPP_AGING_EN<br>(Note1) | IPL |
| 86 | TXD1/FDX_LED1 | FX7_HALF<br>(for IP178CH only) | IPL | FDX_LED1 | FX_HALF7 | IPL |
| 87 | TXD0/FDX_LED0 | APS_DIS | IPL | FDX_LED0 | APS_DIS | IPL |
| 96 | LINK_LED3 | FX6_HALF<br>(for IP178CH only) | IPL | LINK_LED3 | FX_HALF6 | IPL |
| 97 | LINK_LED2 | FX6_EN<br>(for IP178CH only) | IPL | LINK_LED2 | PORT_MIRROR0_7<br>(Note1) | IPL |
| 100 | LINK_LED0 | P6_7_HIGH | IPL | LINK_LED0 | HIGH_PRI[0] | IPL |
| 101 | TXCLK | LONG_PKT_DIS | IPH | | LONG_PKT_DIS | IPH |
| 104 | SCL | MII_MAC | IPL | SCL | | IPL |

**Note1**: FXx_EN not require in IP178D fiber design. Please check chapter ***4.6 Fiber port configuration***

## Features comparison between IP178C and IP178D

| Function | IP178C | IP178D |
|---|---|---|
| Process | 0.18 um | 0.16 um |
| Switch structure | 8 TP + 1* MII<br>(MII related pins: 53, 72 & 104) | 8 TP |
| Port based priority | Yes | Yes |
| 802.1p priority | Yes | Yes |
| Support Fiber function | X | 2 ports with FXSD |
| VLAN | Port base and Tag base VLAN | No |
| IP DiffServ Priority | Yes | Yes |
| SCA (Smart Cable Analysis) | Yes | No |
| Port mirroring | No | Yes |
| Pins configure for port-priority | No | Yes |
| Reduce IPG function | No | Yes |
| TCP/UDP port number priority | No | Yes |
| Fiber support | No | Yes |

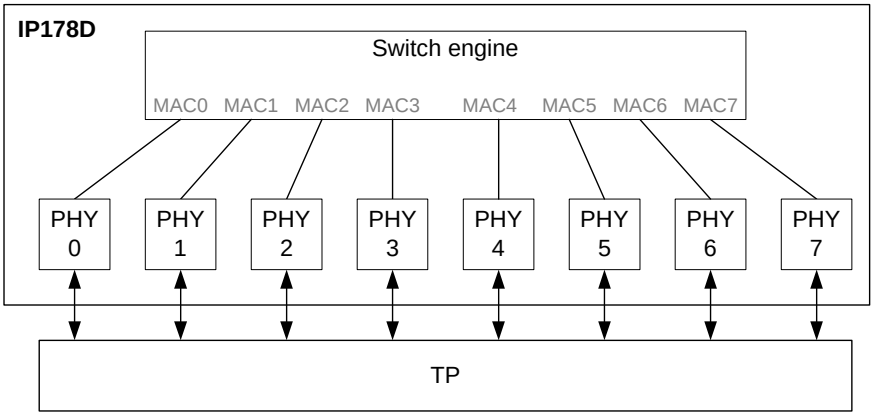
# 1 Pin diagram



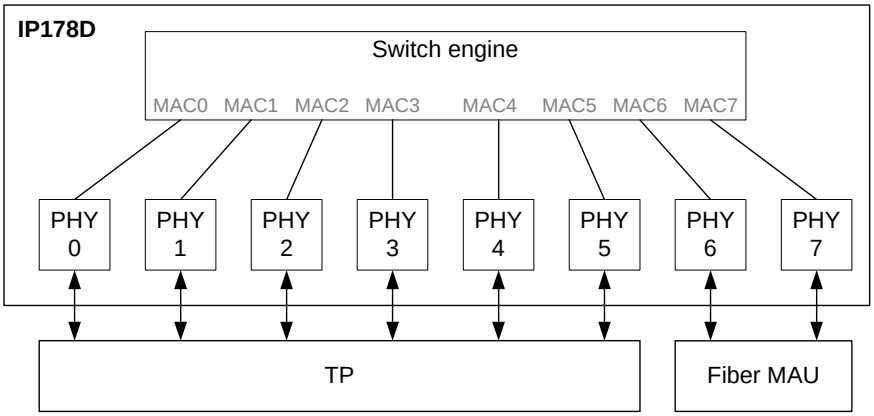
# 2 IP178D application diagram

## 2.1 An 8 TP port switch application

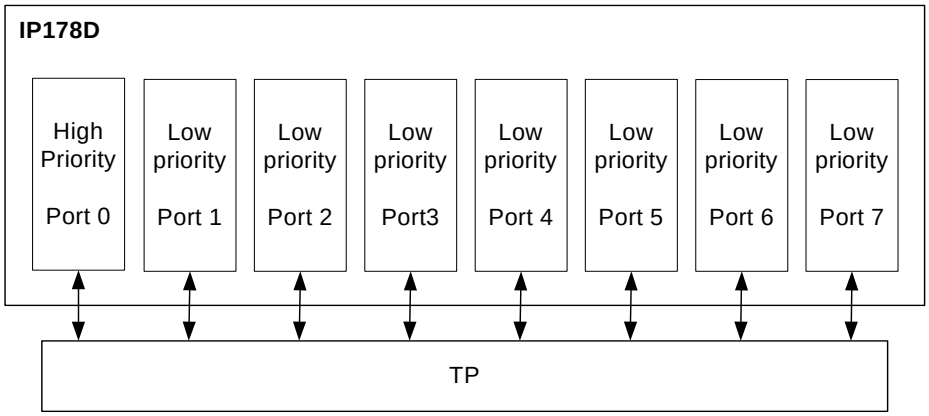
Here shows the application diagram of 8-port switch.




## 2.2 An 8-port switch mixed with two fiber ports

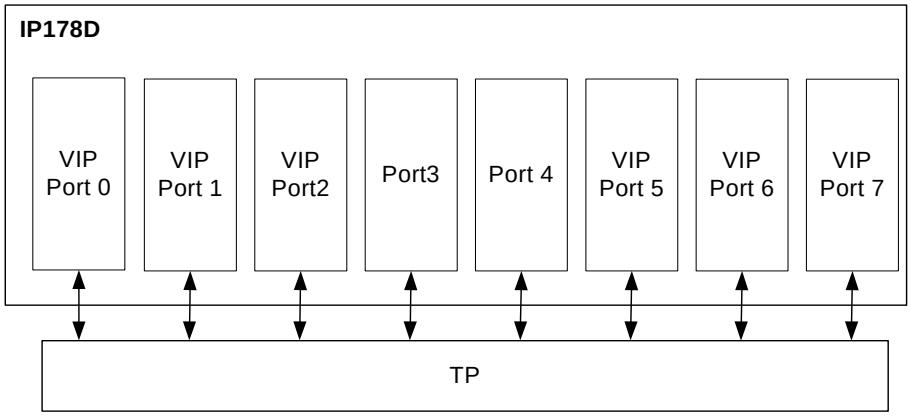


## 2.3 TCP/UDP QoS Switch for time-sensitive application from pin setting



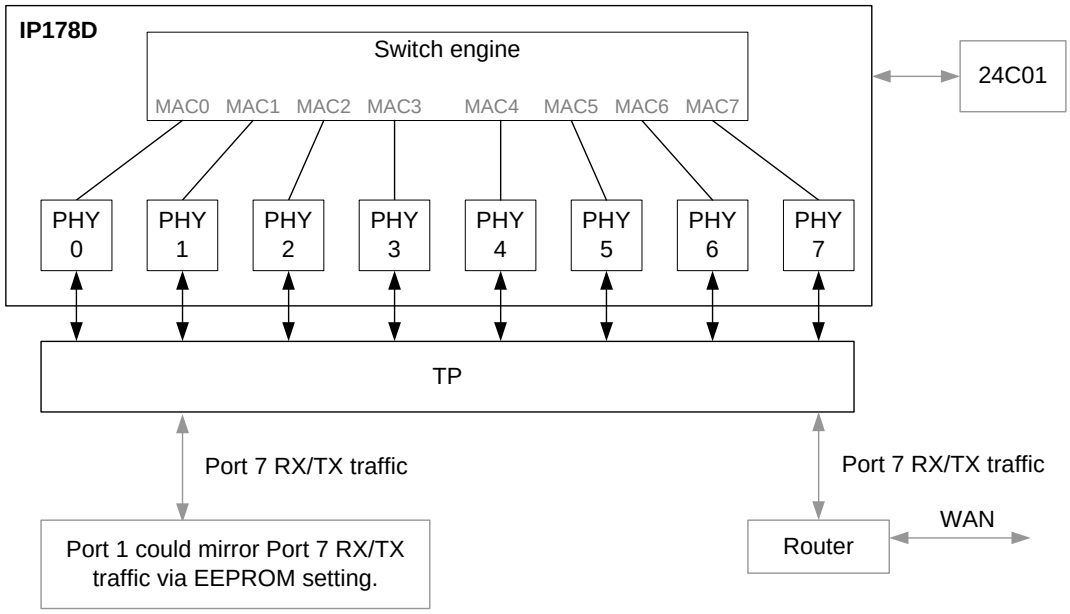

Port 0 received packet with reserved TCP/UDP port number, port 0 will enable its ingress port as a high priority port for 300 seconds.
If the other ports received packets with the same reserved port number, it also has the same behavior as port 0.

## 2.4 Switch with VIP ports for specific users from Pin setting




| Pin 53 , 79, 100 | High Priority Port (VIP port) |
|---|---|
| 0,0,1 | 6, 7 |
| 0,1,0 | 5,6,7 |
| 0,1,1 | 7 |
| 1,0,1 | 0,1 |
| 1,1,0 | 0,1,2 |
| 1,1,1 | 0 |

## 2.5 A 8-port Switch with Port mirror capability setting from EEPROM



# 3 Pin description

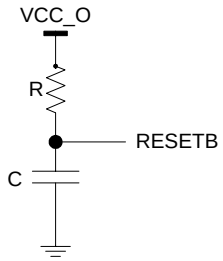
| Type | Description |
|---|---|
| I | Input pin |
| O | Output pin |
| IPL | Input pin with internal pull low |
| IPH | Input pin with internal pull high |

| Type | Description |
|---|---|
| IPL1 | Input pin with internal pull low 22.8k ohm |
| IPH1 | Input pin with internal pull high 22.8k ohm |
| IPL2 | Input pin with internal pull low 92.6k ohm |
| IPH2 | Input pin with internal pull high 113.8k ohm |

## 3.1 Analog pins

| Pin No. | Label | Type | Description |
|---|---|---|---|
| 52 | REG_OUT | O | Regulator output voltage<br><br>The internal regulator uses pin 83 / pin 92 VCC_O as reference voltage to control external transistor to generate a voltage source between 1.80v ~ 2.05v. |
| 17 | BGRES | I | Band gap resister<br><br>It is connected to GND through a 6.19k (1%) resistor in application circuit. |
| 115, 116, 127, 126, 2, 3, 14, 13, 22, 23, 34, 33, 38, 39, 50, 49 | RXIP0~7<br>RXIM0~7 | I | TP receive |
| 119, 120, 123, 122, 6, 7, 10, 9, 26, 27, 30, 29, 42, 43, 46, 45 | TXOP0~7<br>TXOM0~7 | O | TP transmit |
| 96 | FX_HALF6 | IPL1, O | Port 6 fiber port half duplex setting pin<br><br>1: port 6 is half duplex in fiber mode<br>0: port 6 is full duplex in fiber mode |
| 86 | FX_HALF7 | IPL1, O | Port 7 fiber port half duplex setting pin<br><br>1: port 7 is half duplex in fiber mode<br>0: port 7 is full duplex in fiber mode |
| 36 | FXSD6 | I | Fiber signal detection of port 6<br><br>This pin is a direct input pin for fiber signal detection |
| 57 | FXSD7 | I | Fiber signal detection of port 7<br><br>This pin is a direct input pin for fiber signal detection |

### 3.2 System clock & reset pins

| Pin No. | Label | Type | Description |
|---|---|---|---|
| 54 | OSCI | I | 25MHz system clock<br><br>It is recommended to connect OSCI and X2 to a 25MHz crystal. If the clock source is from another chip or oscillator, the clock should be active at least for 1ms before pin 64 RESETB de-asserted.<br>Pin 55 X2 should be left open in this application. |
| 55 | X2 | O | Crystal pin<br><br>A 25Mhz crystal can be connected to OSCI and X2. |
| 64 | RESETB | I | Reset<br><br>It is a low active input pad with Schmitt trigger. The reset time must be hold for more than 1 ms. If an R/C reset circuit is used, the capacitor should be connected to VCC_O as shown in the figure.<br>  <br> |

### 3.3 EEPROM interface

| Pin No. | Label | Type | Description |
|---|---|---|---|
| 105 | SDA | IPH2, O | EEPROM serial address/data I/O<br><br>After reset, it is used as data pin SDA of EEPROM. After reading EEPROM, this pin becomes an input pin. |
| 104 | SCL | IPL2, O | EEPROM serial clock input<br><br>After reset, it is used as clock pin SCL of EEPROM. After reading EEPROM, this pin becomes an input pin. Its period is longer than 10us.<br><br>IP178D stops reading the rest data in EEPROM if the first two bytes in EEPROM aren't 55AA. |

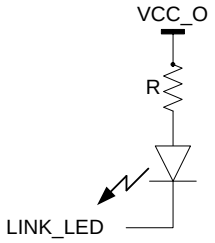
### 3.4 Serial Management Interface

| | Label | Type | Description |
|---|---|---|---|
| 103 | MDC | IPL2 | SMI management data clock<br><br>Sourced continuously from the external device that needs to access the internal registers of IP178D.<br><br>The external device uses SMI interface to access the internal registers of IP178D. IP178D doesn't access the MII registers of external PHY. |
| 102 | MDIO | IPH2 ,O | SMI management data input/output<br><br>A bi-directional multi-drop bus for accessing the internal registers. |

### 3.5 Boundry scan & test mode

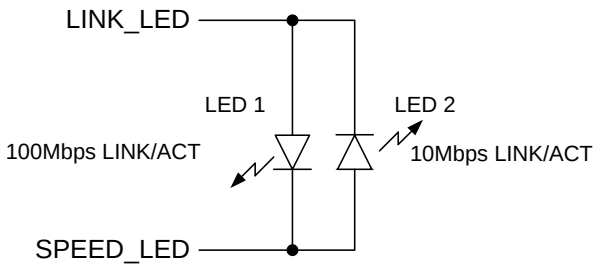
| Pin No. | Label | Type | Description |
|---|---|---|---|
| 103 | SCAN_CLK | IPL2 | Boundry scan clock input |
| 84 | **SCAN_EN** | IPH2 | Boundry scan enable<br><br>To enter the scan mode, pin 53 and 56 should be pulled low at the same time with SCAN_EN is enabled. |
| 71 | **T_MODE_SEL[5]** | IPL1, O | Test mode pin 5<br><br>This pin is a speed LED of port 2 after reset. |
| 70 | **T_MODE_SEL[4]** | IPL1, O | Test mode pin 4<br><br>This pin is a speed LED of port 3 after reset. |
| 69 | **T_MODE_SEL[3]** | IPL1, O | Test mode pin 3<br><br>This pin is a speed LED of port 4 after reset. |
| 68 | **T_MODE_SEL[2]** | IPL1, O | Test mode pin 2<br><br>This pin is a speed LED of port after reset. |
| 67 | **T_MODE_SEL[1]** | IPL1, O | Test mode pin 1<br><br>This pin is a speed LED of port 6 after reset. |
| 66 | **T_MODE_SEL[0]** | IPL1, O | Test mode pin 0<br><br>This pin is a speed LED of port 7 after reset. |

### 3.6 LED interface (I)

| Pin no. | Label | Type | Description |
|---|---|---|---|
| 89, 90, 91, 93, 96, 97, 99, 100 | LINK_LED[7:0] | O | LINK LED<br><br>The detail functions are illustrated in the following table. It should be connected to VCC_O through a LED and a resistor.<br><br>Application circuit<br><br>  <br> |
| 66, 67, 68, 69, 70, 71, 72, 73 | SPEED_LED[7:0] | O | SPEED LED<br><br>The detail functions are illustrated in the following table. It should be connected to VCC_O through a LED and a resistor. |
| 75, 76, 77, 78, 79, 85, 86, 87 | FDX_LED[7:0] | O | FDX LED<br><br>The detail functions are illustrated in the following table. It should be connected to VCC_O through a LED and a resistor. |
| 80, 81 | LED_SEL[1:0] | IPH2 | LED function selection<br><br>The data on these pins are latched at the end of reset to select LED modes. The default value is mode 3. The detail functions are illustrated in the following table. |

| LED_SEL[1:0] | LED mode | LINK_LED[7:0] | SPEED_LED[7:0] | FDX_LED[7:0] |
|---|---|---|---|---|
| 00 | Mode 0 | Off: link fail<br>On: 10 Mbps link ok<br>Flash: TX/RX | Off: link fail<br>On: 100 Mbps link ok<br>Flash: TX/RX | Off: half duplex<br>On: full duplex |
| 01 | Mode 1 | Off: link fail<br>On: link ok<br>Flash: RX | Off: 10 Mbps<br>On: 100 Mbps | Off: half duplex<br>On: full duplex<br>Flash: collision |
| 10 | Mode 2 | Off: link fail<br>On: 10 Mbps link ok<br>Flash: TX/RX | Off: link fail<br>On: 100 Mbps link ok<br>Flash: TX/RX | Off: half duplex<br>On: full duplex<br>Flash: collision |
| 11 (default) | Mode 3 | Off: link fail<br>On: link ok<br>Flash: TX/RX | Off: 10 Mbps<br>On: 100 Mbps | Off: half duplex<br>On: full duplex<br>Flash: collision |

### 3.7 LED interface (II)

| Pin no. | Label | Type | Description |
|---|---|---|---|
| 95 | BI_COLOR | IPL2 | Bi-color LED mode enable<br><br>1: Bi-color mode LED enabled.<br>LED_LINK[7:0] and LED_SPEED[7:0] are used to drive dual color LED. The functions are defined in the following table. The behavior of FDX_LED[7:0] is the same as that in mode3 on the previous page.<br><br>0: Bi-color mode LED disabled.(default)<br>Please refer to pin description of LED_SEL[1:0] for LED functions.<br><br>This pin takes precedence of LED_SEL[1:0].<br><br>Application circuit<br>  <br> |

Bi-color LED definition

| Status | LINK_LED[7:0] | SPEED_LED[7:0] | LED 1 | LED 2 |
|---|---|---|---|---|
| Link off | 1 | 1 | Off | Off |
| 100 Mbps link ok | 1 | 0 | On | Off |
| 100 Mbps link ok/ activity | 1 | Clock | Flash | Off |
| 10 Mbps link ok | 0 | 1 | Off | On |
| 10 Mbps link ok/ activity | Clock | 1 | Off | Flash |

### 3.8 Frame priority setting pins

| Pin no. | Label | Type | Description |
|---|---|---|---|
| 100 | HIGH_PRI[0] | IPL1, O | Port based priority setting, bit 0<br><br>1: enable<br>0: disabled (default)<br>It is an input signal during reset and its value is latched at the end of reset. It acts as a link LED of port 0 after reset.<br><br>VIP port setting as follow,<br>pin 53, 79, 100 HIGH_PRI[2:0] — high priority port number<br>001 — 6, 7<br>010 — 5, 6, 7<br>011 — 7<br>101 — 0, 1<br>110 — 0, 1, 2<br>111 — 0 |
| 99 | **COS_EN** | IPL1, O | Class of service enable<br><br>Packets with high priority tag are handled as high priority packets if the function is enabled.<br><br>1: enable,<br>0: disabled (default)<br><br>It is an input signal during reset and its value is latched at the end of reset. It acts as a link LED of port 1 after reset. |
| 85 | LPP_AGING_EN | IPL1, O | TCP/UDP logical port priority aging enable<br><br>0: disable TCP/UDP logical port priority aging function (default)<br>1: enable TCP/UDP logical port priority aging function<br><br>This function is valid only if pin 99 COS_EN is pulled up, It will change the ingress port behavior as a high priority port after receives the pre-defined TCP/UDP logical port priority frame and hold the ingress port as high priority for 300 seconds.<br><br>LPP_AGING_EN is full duplex LED of port 2 after reset. |
| 79 | HIGH_PRI[1] | IPL1, O | Port based priority setting, bit 1<br><br>For the port based priority setting, reference VIP ports setting as detail.<br>It is an input signal during reset and its value is latched at the end of reset. This pin acts as a duplex LED of port 3 after reset. |
| 53 | HIGH_PRI[2] | IPL1 | Port based priority setting, bit 2<br><br>For the port based priority setting, reference VIP ports setting as detail.<br><br>This pin also use as a test mode setting pin when the pin 84 SCAN_EN is enabled. |

### 3.9 Miscellaneous setting pins (I)

| Pin no. | Label | Type | Description |
|---|---|---|---|
| 101 | LONG_PKT_DIS | IPH2 | Max packet size option<br><br>1: Drop packets with length longer than 1536 bytes (default)<br>0: Drop packets with length longer than 1552 bytes |
| 97 | PORT_MIRROR_0_7 | IPL1, O | Mirror port 0 traffic to port 7<br><br>When enabled, the traffic (RX path) to port 0 will mirror to port 7.<br><br>1: mirror port 0 RX traffic to port 7<br>0: disable mirror function (default)<br><br>This pin is a link LED of port 2 after reset. |
| 93 | MODBCK | IPH1, O | Aggressive back off enable<br><br>IP178D adopts modified (aggressive) back off algorithm if this function is enabled. The maximum back off period is limited to 8-slot time. It makes IP178D have higher transmission priority in a collision event.<br><br>1: aggressive mode enable (default),<br>0: standard back off<br><br>This pin is a link LED of port 4 after reset. |
| 91 | BF_STM_EN | IPL1, O | Broadcast storm enable<br><br>1: enable<br>0: disable (default)<br><br>A port begins to drop packets if it receives broadcast packets more than the threshold defined in MII register 31.9[15:14] BQ_STM_THR_SEL [1:0] or EEPROM register 83[7:6].<br><br>This pin is a link LED of port 5 after reset. |
| 90 | MDI_MDIX_EN | IPH1, O | MDI/MDI-X enable<br><br>MDI/MDI-X auto cross over<br>1: enable (default)<br>0: disable<br><br>It is an input signal during reset and its value is latched at the end of reset to set auto MDI/MDIX function. This pin is a link LED of port 6 after reset. |
| 89 | MLT3_DET | IPL1, O | Ability for detecting MLT3 (for 10 Mbps switch to 100 Mbps)<br><br>1: enable MLT3 detection ability<br>0: disable MLT3 detection ability (default)<br><br>MLT3_DET is link LED of port 7 after reset. |

### 3.10 Miscellaneous setting pins (II)

| Pin no. | Label | Type | Description |
|---|---|---|---|
| 87 | APS_DIS | IPL1, O | Disable advance power saving mode<br><br>1: disable advance power saving mode<br>0: enable advance power saving mode (default)<br><br>APS_DIS is full duplex LED of port 0 after reset. |
| 84 | LOW_10M_DIS | IPH2 | LOW_10M_DIS<br><br>1: disable power saving mode. (default)<br>0: enable power saving mode |
| 79 | PORT_MIRROR0_7 | IPL1, O | Mirror port 0 traffic to port 7<br><br>Mirror the ingress and egress traffic to port 7. To reduce the traffic congestion at port 7, do not use it as a normal operation port.<br><br>1: enable<br>0: disable (default)<br><br>This pin is a duplex LED of port 3 after reset. |
| 78 | FILTER_DA | IPL1, O | Reserved address forward option<br><br>Filter packets with specific DA (Destination Address) from 01:80:C2:00:00:02 to 01:80:C2:00:00:0F. Packets with specific DA equal to 01:80:C2:00:00:01 are always filtered regardless the setting of this pin.<br><br>1: filter<br>0: forward (default)<br><br>This pin is a duplex LED of port 4 after reset. |
| 77 | BCSTF | IPL1, O | Broadcast frame option<br><br>1: Packets with DA equal to FF:FF:FF:FF:FF:FF are handled as broadcast frame in broadcast protection function,<br>0: Packets with DA equal to FF:FF:FF:FF:FF:FF or multi-cast frames are handled as broadcast frame in broadcast protection function.<br><br>This pin is a duplex LED of port 5 after reset. |
| 76 | AGING | IPH1, O | Aging enable<br><br>1: enable 300s aging timer (default)<br>0: disable aging function<br><br>This pin is a duplex LED of port 6 after reset. |

### 3.11 Miscellaneous setting pins (III)

| Pin no. | Label | Type | Description |
|---|---|---|---|
| 75 | X_EN | IPH1, O | Flow control enable<br><br>1: enable IEEE802.3x & back pressure (default)<br>0: disable IEEE802.3x & back pressure<br><br>The function is valid only if pin 53 is pulled low. This pin is a duplex LED of port 7 after reset. |
| 73 | PS_MODE_0_100 | IPL1, O | Power saving mode<br><br>1: power saving mode for 0 to 100 mA<br>0: power saving mode for 40 to 100 mA (default)<br><br>This pin is a speed LED of port 0 after reset. |
| 72 | REDUCE_IPG_DIS | IPL1, O | Reduce IPG function<br><br>This function reduce the IPG by random from 0 ~ 20 PPM.<br><br>1: disable reduce IPG function<br>0: enable reduce IPG function<br><br>This pin is a speed LED of port 1 after reset. |

### 3.12 Power & ground pins

| Pin no. | Label | Type | Description |
|---|---|---|---|
| 16 | BGVCC | I | Power of band gap circuit |
| 18 | BGGND | I | Power of band gap circuit |
| 19 | PLLGND | I | Ground of PLL circuit |
| 20 | PLLVCC | I | Power of PLL circuit |
| 58, 59, 60, 110, 111, 112, 113 | GND | I | Ground of internal logic |
| 61, 62, 63, 106, 107, 108, 109, | VCC | I | Power of internal logic |
| 65, 94, | GND_SRAM | I | Ground of internal SRAM |
| 74, 98, | VCC_SRAM | I | Power of internal SRAM |
| 82, 88, | GND_O | I | Ground for LED and EEPROM |
| 83, 92, | VCC_O | I | Power for LED and EEPROM (3.3V or 2.5V) |
| 114, 128, 1, 15, 21, 35, 37, 51 | RXVCC0~7 | I | Power of analog receive block |
| 117, 125, 4, 12, 24, 32, 40, 48, | RXGND0~7 | I | Ground of analog receive block |
| 118, 124, 5, 11, 25, 31, 41, 47, | TXGND0~7 | I | Ground of analog transmit buffer |
| 121, 8, 28, 44, | TXVCC01<br>TXVCC23<br>TXVCC45<br>TXVCC67 | I | Power of analog transmit buffer |

# 4 Functional Description

## 4.1 LED display (normal operation)

| **Normal operation** | | | |
|---|---|---|---|
| LED_O_SEL[1:0] | LINK_LED | SPEED_LED | FDX_LED |
| 00 | Off: link fail<br>On: 10 Mbps link ok<br>Flash: TX/RX | Off: link fail<br>On: 100 Mbps link ok<br>Flash: TX/RX | Off: half duplex<br>On: full duplex |
| 01 | Off: link fail<br>On: link ok<br>Flash: RX | Off: 10 Mbps<br>On: 100 Mbps | Off: half duplex<br>On: full duplex<br>Flash: collision |
| 10 | Off: link fail<br>On: 10 Mbps link ok<br>Flash: TXRX | Off: link fail<br>On: 100 Mbps link ok<br>Flash: TX/RX | Off: half duplex<br>On: full duplex<br>Flash: collision |
| 11 | Off: link fail<br>On: link ok<br>Flash: TX/RX | Off: 10 Mbps<br>On: 100 Mbps | Off: half duplex<br>On: full duplex<br>Flash: collision |
| Flash behavior: Off 44ms → On 176ms → Off 44ms → … | | | |

## 4.2 Flow control

IP178D jams or pauses a port, which causes output queue over the threshold. Its link partner will defer transmission after detecting the jam or pause frame. A port of IP178D defers transmission when it receives a jam or a pause frame. The source address (SA) of pause control frame will be { IP178D OUI (0090C3), port number}. For example, the SA of port 1 pause control frame will be " 00 90 C3 00 00 01".

When CoS is enabled, IP178D may disable the flow control function for a short term to guarantee the bandwidth of high priority packets. A port disables its flow control function for 2 ~ 3 seconds when it receives a high priority packet. It doesn't transmit pause frame or jam pattern during the period but it still responses to pause frame or jam pattern.

The flow control function can be enabled by pulling up pin 75 X_EN or by programming MII register 30.1.10.

## 4.3 Broadcast storm protection

A port of IP178D begins to drops broadcast packets if the received broadcast packets are more than the threshold defined in MII register 31.9[15:14] or EEPROM register 83[7:6] BQ_STM_THR_SEL [1:0] in 10ms (100Mbps) or 100ms (10Mbps)

The function can be enabled by pulling high pin 91 BF_STM_EN or programming MII register 30.1[6].

IP178D handles multicast frame as a broadcast frame in broadcast storm protection function if pin 77 BCSTF is pulled low.

## 4.4 CoS

IP178D supports two types of CoS. One is port base priority function and the other is frame base priority function. IP178D supports two levels of priority queues. A high priority packet will be queued to the high priority queue to share more bandwidth. The ratio of bandwidth of high priority and low priority queue is defined in MII register 30.1[15] or EEPROM 3[7].

### 4.4.1 Port base priority

The packets received from high priority port will be handled as high priority frames if the port base priority is enabled. It is enabled by programming the corresponding bit in MII register 31.0[9] ~ 31.7[9] or EEPROM register 65[1] ~79[1]. Each port of IP178D can be configured as a high priority port individually.

### 4.4.2 VIP ports

This port based priority function can active either by register or pin setting. There are three pins dedicate for enabling the port based priority function. The follow illustration shows the pin setting part of the port based priority function.

| pin number | 53 | 79 | 100 |
|---|---|---|---|
| name | HIGH_PRI[2] | HIGH_PRI[1] | HIGH_PRI[0] |

| HIGH[2:0] | High priority port |
|---|---|
| 001 | 6, 7 |
| 010 | 5, 6, 7 |
| 011 | 7 |
| 101 | 0, 1 |
| 110 | 0, 1, 2 |
| 111 | 0 |
| others | reserved |

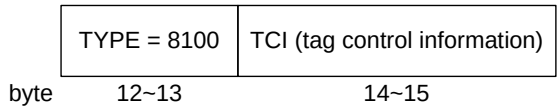
### 4.4.3 Frame base priority

#### 4.4.3.1 VLAN tag and TCP/IP TOS

IP178D examines the specific bits of VLAN tag and TCP/IP TOS for priority frames if the frame base priority is enabled. The packets will be handled as high priority frames if the tag value meets the high priority requirement, that is, VLAN tag bigger than 3 or TCP/IP TOS field not equal to 3'b000. It is enabled by programming the corresponding bit in MII register 31.0[10]~31.7[10] or EEPROM register 65[2]~79[2]. The frame base priority function of each port can be enabled individually.

IP178D supports an easy way to enable a sub set of CoS function without programming EEPROM or MII registers. Frame base priority function of all ports is enabled if pin 99 COS_EN is pulled high. The setting in register takes precedence of the setting on pins.

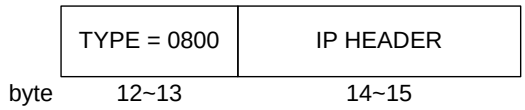
VLAN field




TCI definition:

Bit[15:13]: User Priority 7~0
Bit 12: Canonical Format Indicator (CFI)
Bit[11~0]: VLAN ID.
IP178D uses bit[15:13] to define priority.

TOS field




IP header definition:
Byte 14
Bit[7:0]: IP protocol version number & header length.

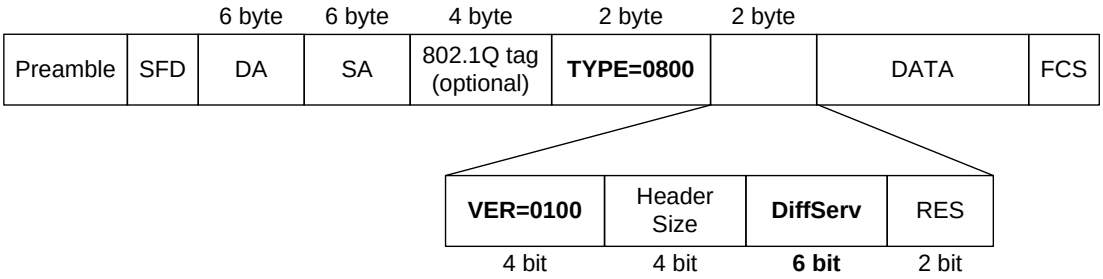
Byte 15: Service type
Bit[7~5]: IP Priority (Precedence ) from 7~0
Bit 4: No Delay (D)
Bit 3: High Throughput
Bit 2: High Reliability (R)
Bit[1:0]: Reserved
IP178D uses bit[7:5] to define priority.
0~3: low priority
4~7: high priority

#### 4.4.3.2 IPv4/IPv6 DiffServ

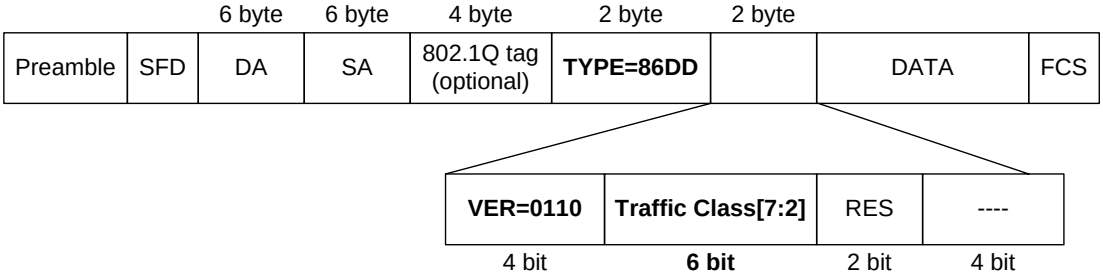
IP178D checks the DiffServ field of a IPv4 frame or Traffic class field [7:2] (TC[7:2]) of a IPv6 frame and uses them to decide the frame's priority if MII register 31.30.[13] DIFFSERV_EN is enabled. IP178D uses DiffServ or TC[7:2] as index to select one of 64 bits. If the bit is "1", the received frame is handled as a high priority frame. IP178D recognize the following DSCP (Differentiated Service Code Point) Octet as high priority frame.

6'b101110
6'b001010
6'b010010
6'b011010
6'b100010
6'b11x000

**IPv4 frame format**




**IPv6 frame format**



#### 4.4.3.3 TCP/UDP logical port priority

IP178D can configure the ingress port frame priority by using the TCP/UDP frame logical port number. When the incoming IP packet with TCP or UDP protocols, the 16 bits destination or source port field in the TCP/UDP header can be used for assign the frame priority. It means the source's logical port or the destination's logical port in the incoming packet match any of the pre-defined logical ports, the incoming frame will give a high priority mark and put it in the high priority queue.
TCP/UDP logical port priority function of all ports is enabled if pin 99 COS_EN is pulled high. The logical port priority of each pre-defined port number or user defined range of logical port number can be enabled individually by programming the corresponding bit in the MII register 30.14[5:0] or EEPROM register 10[5:0].

- Pre-defined logical ports list

| Service | TCP | Description |
|---|---|---|
| SSH | 22 | secure shell |
| HTTPs | 443 | secure HTTP (SSL) |
| RDP | 3389 | Windows Remote Desktop Protocol |
| XWIN | 6000 | X11 – used for X-Windows |

These pre-defined logical ports can be enable individually by programming MII register 30.14[3:0] or EEPROM register 10[3:0].

- User defined range logical ports list (defaulting setting)

| Service | TCP | Description |
|---|---|---|
| telnet | 23 | Remote terminal protocol |
| VNC | 5800 | VNC remote desktop protocol |

For the user defined range logical ports, it contains two set of range and can be changed by programming via MII register or EEPROM register. Each range consists of a high and low limit register to set the TCP or UDP logical port range. The high limit port number can not large than the low limit port number. The default logical port number of range 0 and 1 are default set to 23 and 5800, for this case the high and low limit port number is the same value. If an incoming IP frame with TCP/UDP port number is between the low and high limit, it will be treated as a high priority frame.

## 4.5 Port Mirroring

There are some circumstances that the network administrator requires to monitor the network status. The port mirroring function can help the network administrator diagnose the network.

A port mirroring function can be accomplished by assigning a monitored port and a snooping port. The IP178D supports four kinks of monitoring methods: source port, destination port, one port of source and destination, source-destination pair. This function can be enabled by programming the corresponding bit in MII registers 30.3~30.4.

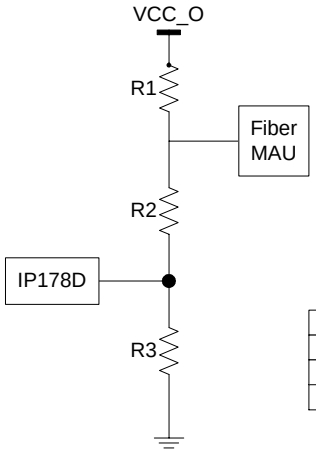
## 4.6 Buffer Aging

When buffer aging was enabled, a frame stayed in output port for transmission is discarded if buffer aging time has exceeded one second. The buffer aging time is the maximum delay time for transmission on output port. This function can be set from MII register 30.13.13.

## 4.7 Fiber port configuration

Port 6 and 7 of IP178D can be configured to be a fiber port or a TP port individually. A port becomes a fiber port if its FXSDx is connected to a fiber MAU or pulled to high. A port becomes a TP port if it's FXSDx is pulled low.

| Voltage on FXSDx | TP port | Fiber port | Fiber signal detect | Condition |
|---|---|---|---|---|
| < 0.6 V | Yes | -- | -- | |
| > 0.6 V < 1.2 V | -- | Yes | Off | Fiber unplugged |
| > 1.2 V | -- | Yes | On | Fiber plugged |



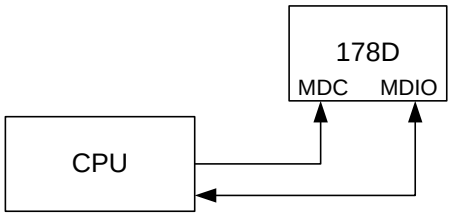

| | 3V | 5V |
|---|---|---|
| R1 | 130 | 82 |
| R2 | 0 | 0 |
| R3 | 82 | 130 |

R2 and R3 may change

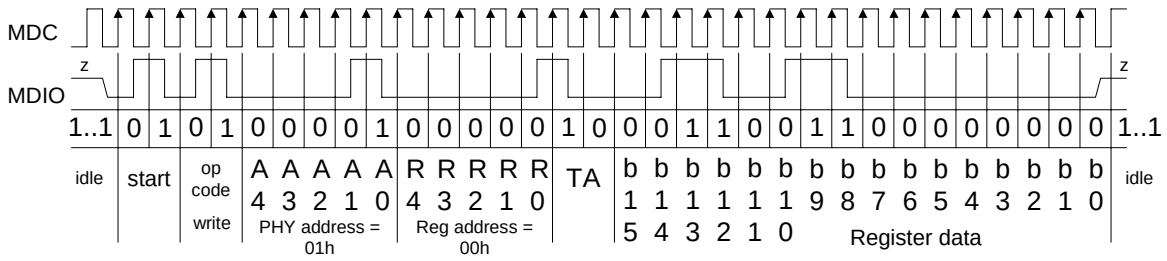
## 4.8 Serial management interface

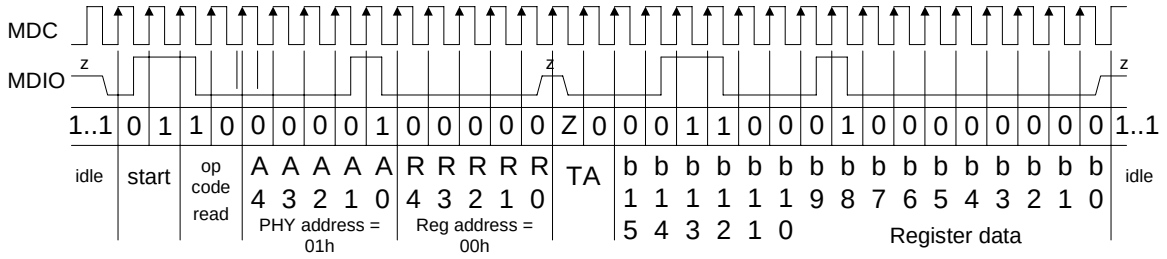
User can access IP178D's MII registers through serial management interface with pin MDC and MDIO. Its format is shown in the following table. To access MII register in IP178D, MDC should be at least one more cycle than MDIO. That is, a complete command consists of 32 bits MDIO data and at least 33 MDC clocks. When the SMI is idle, MDIO is in high impedance.

**Syatem diagram**




| **Frame format** | **<Idle><start><op code><PHY address><Registers address><turnaround><data><idle>** |
|---|---|
| Read Operation | <Idle><01><10><$A_4A_3A_2A_1A_0$><$R_4R_3R_2R_1R_0$><Z0><br><$b_{15}$ $b_{14}$ $b_{13}$ $b_{12}$ $b_{11}$ $b_{10}$ $b_9$ $b_8$ $b_7$ $b_6$ $b_5$ $b_4$ $b_3$ $b_2$ $b_1b_0$><Idle> |
| Write Operation | <Idle><01><01><$A_4A_3A_2A_1A_0$><$R_4R_3R_2R_1R_0$><10><br><$b_{15}$ $b_{14}$ $b_{13}$ $b_{12}$ $b_{11}$ $b_{10}$ $b_9$ $b_8$ $b_7$ $b_6$ $b_5$ $b_4$ $b_3$ $b_2$ $b_1b_0$><Idle> |



# 5 Register descriptions

## 5.1 Register map

### 5.1.1 EEPROM map

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 0~1 | Load EEPROM (55AA) | | | | | | | |
| 2 | bp_kind | bf_stm_en | mlt3_det_en | aps_dis | aging | | mod bck | drop extra long packet |
| 3 | priority_rate | led_o_sel | | reduce_ipg | drop16 | x_en | mod_carrier_algorithm | bk_en |
| 4 | input_filter | hash_mode | | | | | | bi_color |
| 5 | tmode_sel | | | | | | mdi_mdix_en | |
| 6 | port_mirror_en | port_mirror_mode | | | sel_mirror_port | | | |
| 7 | sel_rx_port_mirror | | | | | | | |
| 8 | sel_tx_port_mirror | | | | | | | |
| 9 | fiber_duplex[7:6] | | | | | | | |
| 10 | | | userdef_range_en[1:0] | predef_port_en[3:0] | | | | |
| 11 | userdef_range0_high[7:0] | | | | | | | |
| 12 | userdef_range0_high[15:8] | | | | | | | |
| 13 | userdef_range0_low[7:0] | | | | | | | |
| 14 | userdef_range0_low[15:8] | | | | | | | |
| 15 | userdef_range1_high[7:0] | | | | | | | |
| 16 | userdef_range1_high[15:8] | | | | | | | |
| 17 | userdef_range1_low[7:0] | | | | | | | |
| 18 | userdef_range1_low[15:8] | | | | | | | |
| 19 | lpp_aging_en_[7:0] | | | | | | | |
| 20 ~ 64 | | | | | | | | |
| 65 | | | | | | port0_cos_en | port0_high_priority | |
| 66 | | | | | | | | |
| 67 | | | | | | port1_cos_en | port1_high_priority | |

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 68 | | | | | | | | |
| 69 | | | | | | port2_cos_en | port2_high_priority | |
| 70 | | | | | | | | |
| 71 | | | | | | port3_cos_en | port3_high_priority | |
| 72 | | | | | | | | |
| 73 | | | | | | port4_cos_en | port4_high_priority | |
| 74 | | | | | | | | |
| 75 | | | | | | port5_cos_en | port5_high_priority | |
| 76 | | | | | | | | |
| 77 | | | | | | port6_cos_en | port6_high_priority | |
| 78 | | | | | | | | |
| 79 | | | | | | port7_cos_en | port7_high_priority | |
| 80 ~ 81 | | | | | | | | |
| 82 | unit_high_thr_sel | | | predrop_en | pkt_low_thr_sel | | pkt_high_thr_sel | |
| 83 | bf_stm_thr_sel | | share_full_thr_sel | | unit_default_thr_sel | | unit_low_thr_sel | |
| 84 ~ 124 | | | | | | | | |
| 125 | | diffserv_en | bf_ffff_only | special_add_forward | | | | |

### 5.1.2 MII register map

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 30.0 | Software Reset Register(55AA) | | | | | | | | | | | | | | | |
| 30.1 | priority_rate | led_o_sel | | reduce_ipg | drop16 | x_en | modify_carrier_algorithm | bk_en | bp_kind | bf_stm_en | mlt3_det_en | aps_dis | aging | | modback | drop_extra_long_packet |
| 30.2 | tmode_sel | | | | | | mdi_mdix_en | | input_filetr | hash_mode | | | | | | bi_color |
| 30.3 | port_mirror_en | port_mirror_mode | | | | | | | sel_rx_port_mirror | | | | | | | |
| 30.4 | sel_mirror_port | | | | | | | | sel_tx_port_mirror | | | | | | | |
| 30.12 | | | | | | | | | | | | | | | | |
| 30.13 | fiber_duplex[7] | fiber_duplex[6] | | | | | | | port_backpress_en | | | | | | | |
| 30.14 | lpp_aging_en[7:0] | | | | | | | | | | userdef_range_en[1:0] | predef_port_en[3:0] | | | | |
| 30.15 | userdef_range0_high[15:0] | | | | | | | | | | | | | | | |
| 30.16 | userdef_range0_low[15:0] | | | | | | | | | | | | | | | |
| 30.17 | userdef_range1_high[15:0] | | | | | | | | | | | | | | | |
| 30.18 | userdef_range1_low[15:0] | | | | | | | | | | | | | | | |

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31.0 | | | | | | port0_cos_en | port 0_high_ priority | | | | | | | | | |
| 31.1 | | | | | | port1_cos_en | port 1_high_ priority | | | | | | | | | |
| 31.2 | | | | | | port2_cos_en | port 2_high_ priority | | | | | | | | | |
| 31.3 | | | | | | port3_cos_en | port 3_high_ priority | | | | | | | | | |
| 31.4 | | | | | | port4_cos_en | port 4_high_ priority | | | | | | | | | |
| 31.5 | | | | | | port5_cos_en | port 5_high_ priority | | | | | | | | | |
| 31.6 | | | | | | port6_cos_en | port 6_high_ priority | | | | | | | | | |
| 31.7 | | | | | | port7_cos_en | port 7_high_ priority | | | | | | | | | |
| 31.8 | | | | | | | | | | | | | | | | |
| 31.9 | bf_stm_thr_sel | | share_full_thr_sel | | unit_default_thr_sel | | unit_low_thr_sel | | unit_high_thr_sel | | | predrop _en | pkt_low_thr_sel | | pkt_high_thr_sel | |
| 31.10~29 | | | | | | | | | | | | | | | | |
| 31.30 | | | diffserv_en | bf_ffff_only | special_add_forward | | | | | | | | | | | |

## 5.2 PHY registers

R/W = Read/Write, SC = Self-Clearing, RO = Read Only, LL = Latching Low, LH = Latching High

### 5.2.1 Basic MII registers of port 0

#### 5.2.1.1 MII control registers (address 00)

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 0 | 0.15 | -- | | Reset | 0 |
| 0 | 0.14 | -- | R/W | Loop back<br>1 = Loop back mode<br>0 = normal operation<br>When this bit set, IP178D will be isolated from the network media, that is, the assertion of TXEN at the MII will not transmit data on the network. All MII transmission data will be returned to MII receive data path in response to the assertion of TXEN. | 0 |
| 0 | 0.13 | -- | RW | Speed Selection<br>1 = 100 Mbps<br>0 = 10 Mbps<br>It is valid only if bit 0.12 is set to be 0. | 1 |
| 0 | 0.12 | -- | RW | Auto-Negotiation Enable<br>1 = Auto-Negotiation Enable<br>0 = Auto-Negotiation Disable | 1 |
| 0 | 0.11 | -- | R/W | Power Down | 0 |
| 0 | 0.10 | -- | | Isolate | 0 |
| 0 | 0.9 | -- | RW SC | Restart Auto- Negotiation<br>1 = re-starting Auto-Negotiation<br>0 = Auto-Negotiation re-start complete<br>Setting this bit to logic high will cause IP178D to restart an Auto-Negotiation cycle, but depending on the value of bit 0.12 (Auto-Negotiation Enable). If bit 0.12 is cleared then this bit has no effect, and it is Read Only. This bit is self-clearing after Auto-Negotiation process is completed. | 0 |
| 0 | 0.8 | -- | R/W | Duplex mode<br>1 = full duplex<br>0 = half duplex<br>It is valid only if bit 0.12 is set to be 0. | 0 |
| 0 | 0.7 | -- | R/W | Collision test | 0 |
| 0 | 0[6:0] | -- | R/W | Write as 0, ignore on read | - |

#### 5.2.1.2 MII status registers (address 01)

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 0 | 1.15 | -- | RO | 100Base-T4 capable<br>1 = 100Base-T4 capable<br>0 = not 100Base-T4 capable<br>IP178D does not support 100Base-T4. This bit is fixed to be 0. | 0 |
| 0 | 1.14 | -- | RO | 100Base-X full duplex Capable<br>1 = 100Base-X full duplex capable<br>0 = not 100Base-X full duplex capable<br>The default of this bit will change depend on the external setting of IP178D. If external pin setting without 100Base-X full duplex support, then this bit will change default to logic 0. | 1 |
| 0 | 1.13 | -- | RO | 100Base-X half duplex Capable<br>1 = 100Base-X half duplex capable<br>0 = not 100Base-X half duplex capable<br>The default of this bit will change depend on the external setting of IP178D. If external pin setting without 100Base-X half duplex support, then this bit will change default to logic 0 | 1 |
| 0 | 1.12 | -- | RO | 10Base-T full duplex Capable<br>1 = 10Base-T full duplex capable<br>0 = not 10Base-T full duplex capable<br>The default of this bit will change depend on the external setting of IP178D. If external pin setting without 100Base-T full duplex support, then this bit will change default to logic 0 | 1 |
| 0 | 1.11 | -- | RO | 10Base-T half duplex Capable<br>1 = 10Base-T half duplex capable<br>0 = not 10Base-T half duplex capable<br>The default of this bit will change depend on the external setting of IP178D. If external pin setting without 100Base-X full duplex support, then this bit will change default to logic 0 | 1 |
| 0 | 1[10:7] | -- | RO | Reserved<br>Ignore on read | - |
| 0 | 1.6 | -- | RO | MF preamble Suppression<br>1 = preamble may be suppressed<br>0 = preamble always required | 1 |
| 0 | 1.5 | -- | RO | Auto-Negotiation Complete<br>1 = Auto-Negotiation complete<br>0 = Auto-Negotiation in progress<br>When read as logic 1, indicates that the Auto-Negotiation process has been completed, and the contents of register 4 and 5 are valid. When read as logic 0, indicates that the Auto-Negotiation process has not been completed, and the contents of register 4 and 5 are meaningless. If Auto-Negotiation is disabled (bit 0.12 set to logic 0), then this bit will always read as logic 0. | 0 |

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 0 | 1.4 | -- | RO LH | Remote fault<br>1 = remote fault detected<br>0 = not remote fault detected<br>When read as logic 1, indicates that IP178D has detected a remote fault condition. This bit is set until remote fault condition gone and before reading the contents of the register. This bit is cleared after IP178D reset. | 0 |
| 0 | 1.3 | -- | RO | Auto-Negotiation Ability<br>1 = Auto-Negotiation capable<br>0 = not Auto-Negotiation capable<br>When read as logic 1, indicates that IP178D has the ability to perform Auto-Negotiation. The value of this bit will depend on the external mode setting of IP178D operation mode. | 1 |
| 0 | 1.2 | -- | RO LL | Link Status<br>1 = Link Pass<br>0 = Link Fail<br>When read as logic 1, indicates that IP178D has determined a valid link has been established. When read as logic 0, indicates the link is not valid. This bit is cleared until a valid link has been established and before reading the contents of this registers. | 0 |
| 0 | 1.1 | -- | | Jabber Detect<br>1 = jabber condition detected<br>0 = no jabber condition detected<br>When read as logic 1, indicates that IP178D has detected a jabber condition. This bit is always 0 for 100 Mbps operation and is cleared after IP178D reset. This bit is set until jabber condition is cleared and reading the contents of the register. | 0 |
| 0 | 1.0 | -- | RO | Extended capability<br>1 = Extended register capabilities<br>0 = No extended register capabilities<br>IP178D has extended register capabilities. | 1 |

#### 5.2.1.3 PHY Identifier (address 02)

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 0 | 2 | -- | RO | IP178D OUI (Organizationally Unique Identifier) ID, the MSB is 3rd bit of IP178D OUI ID, and the LSB is 18th bit of IP178D OUI ID. IP178D OUI is 0090C3. | 0243h |

#### 5.2.1.4 PHY Identifier (address 03)

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 0 | 3[15:10] | -- | RO | PHY identifier<br>IP178D OUI ID, the MSB is 19th bit of IP178D OUI ID, and LSB is 24th bit of IP178D OUI ID. | 3h |
| 0 | 3[9:4] | -- | RO | Manufacture's Model Number<br>IP178D model number | 18h |
| 0 | 3[3:0] | -- | RO | Revision Number<br>IP178D revision number | 0 |

#### 5.2.1.5 Auto-Negotiation Advertisement registers (address 04)

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 0 | 4.15 | -- | | Next Page<br>Not supported | 0 |
| 0 | 4.14 | -- | RW | Reserved by IEEE, write as 0, ignore on read | 0 |
| 0 | 4.13 | -- | R/W | Remote Fault<br>Not supported | 0 |
| 0 | 4[12:11] | -- | RO | Reserved for future IEEE use, write as 0, ignore on read | 0 |
| 0 | 4.10 | -- | RW | Pause<br>1 = Advertises that this device has implemented pause function<br>0 = No pause function supported | 0 |
| 0 | 4.9 | -- | RW | 100BASE-T4 Not supported | 0 |
| 0 | 4.8 | -- | R/W | 100BASE-TX full duplex<br>1 = 100BASE-TX full duplex is supported<br>0 = 100BASE-TX full duplex is not supported | 1 |
| 0 | 4.7 | -- | R/W | 100BASE-TX<br>1 = 100BASE-TX is supported<br>0 = 100BASE-TX is not supported | 1 |
| 0 | 4.6 | -- | R/W | 10BASE-T full duplex<br>1 = 10BASE-T full duplex is supported<br>0 = 10BASE-T full duplex is not supported | 1 |
| 0 | 4.5 | -- | R/W | 10BASE-T<br>1 = 10BASE-T is supported<br>0 = 10BASE-T is not supported | 1 |
| 0 | 4[4:0] | -- | R/W | Selector Field<br>Use to identify the type of message being sent by Auto-Negotiation. | 00001 |

#### 5.2.1.6 Link partner ability registers (address 05)

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 0 | 5.15 | | RO | Next Page<br>1 = Next Page ability is supported by link partner<br>0 = Next Page ability does not supported by link partner | 0 |
| 0 | 5.14 | | RO | Acknowledge<br>1 = Link partner has received the ability data word<br>0 = Not acknowledge | 0 |
| 0 | 5.13 | | RO | Remote Fault<br>1 = Link partner indicates a remote fault<br>0 = No remote fault indicate by link partner<br>If this bit is set to logic 1, then bit 1.4 (Remote fault) will set to logic 1. | 0 |
| 0 | 5[12:11] | -- | RO | Reserved by IEEE for future use, write as 0, read as 0. | 0 |
| 0 | 5.10 | -- | RO | Pause<br>1 = Link partner support IEEE802.3x<br>0 = Link partner does not support IEEE802.3x<br>IP178D will reload the default value after rest or link failure. | 1 |
| 0 | 5.9 | -- | RO | 100BASE-T4<br>1 = Link partner support 100BASE-T4<br>0 = Link partner does not support 100BASE-T4 | 0 |
| 0 | 5.8 | -- | RO | 100BASE-TX full duplex<br>1 = Link partner support 100BASE-TX full duplex<br>0 = Link partner does not support 100BASE-TX full duplex | 0 |
| 0 | 5.7 | -- | RO | 100BASE-TX<br>1 = Link partner support 100BASE-TX<br>0 = Link partner does not support 100BASE-TX | 0 |
| 0 | 5.6 | -- | RO | 10BASE-T full duplex<br>1 = Link partner support 10BASE-T full duplex<br>0 = Link partner does not support 10BASE-T full duplex | 0 |
| 0 | 5.5 | -- | RO | 10BASE-T<br>1 = Link partner support 10BASE-T<br>0 = Link partner does not support 10BASE-T | 0 |
| 0 | 5[4:0] | -- | RO | Selector Field<br>Protocol selector of the link partner | 00000 |

### 5.2.2 Basic MII registers of port 1-7

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| **Port 1 MII register 0~5** | | | | | |
| 1 | 0~5 | -- | | Please refer to MII registers 0.0~0.5. | |

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| **Port 2 MII register 0~5** | | | | | |
| 2 | 0~5 | -- | | Please refer to MII registers 0.0~0.5. | |

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| **Port 3 MII register 0~5** | | | | | |
| 3 | 0~5 | -- | | Please refer to MII registers 0.0~0.5. | |

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| **Port 4 MII register 0~5** | | | | | |
| 4 | 0~5 | -- | | Please refer to MII registers 0.0~0.5. | |

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| **Port 5 MII register 0~5** | | | | | |
| 5 | 0~5 | -- | | Please refer to MII registers 0.0~0.5. | |

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| **Port 6 MII register 0~5** | | | | | |
| 6 | 0~5 | -- | | Please refer to MII registers 0.0~0.5. | |

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| **Port 7 MII register 0~5** | | | | | |
| 7 | 0~5 | -- | | Please refer to MII registers 0.0~0.5. | |

## 5.3 Switch control registers (I)

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| **EEPROM enable register / Software reset register** | | | | | |
| 30 | -- | 1, 0 | | EEPROM enable register<br>This register should be filled with 55AA in EERPOM register 0 and 1. IP178D will examine the specified pattern to confirm if there is a valid EEPROM. The initial setting is updated with the content of EEPROM only if the specified pattern 55AA is found. | |
| 30 | 0 | -- | R/W | Software reset register<br>MII register 0 is software reset register. User can reset IP178D by writing 55AA to this register. | |
| 30 | 0[15] | -- | R | BFLL_FULL, free buffer is full<br>1: full,<br>0: not full<br>This bit is for debug only. | |
| 30 | 0[14] | | | Reserved | |
| 30 | 0[13] | -- | R | Empty, all output queue is empty<br>1: empty<br>0: not empty<br>This bit is for debug only. | |
| 30 | 0[12:0] | | | Reserved | |

## 5.4 Switch control registers (II)

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 30 | 1[15] | 3[7] | R/W | PRIORITY_RATE<br>1: 8 packets<br>0: 16 packets<br><br>Output Queue Scheduling: high priority packet rate | 1'b0 |
| 30 | 1[14:13] | 3[6:5] | R/W | LED_O_SEL<br>LED mode selection | P(1,1) |

| | LINK_LED | SPEED_LED | FDX_LED |
|---|---|---|---|
| 00 | Off: link fail<br>On: 10 Mbps link ok<br>Flash: TX/RX | Off: link fail<br>On: 100 Mbps link ok<br>Flash: TX/RX | Off: half duplex<br>On: full duplex |
| 01 | Off: link fail<br>On: link ok<br>Flash: RX | Off: 10 Mbps<br>On: 100 Mbps | Off: half duplex<br>On: full duplex<br>Flash: collision |
| 10 | Off: link fail<br>On: 10 Mbps link ok<br>Flash: TX/RX | Off: link fail<br>On: 100 Mbps link ok<br>Flash: TX/RX | Off: half duplex<br>On: full duplex<br>Flash: collision |
| 11 | Off: link fail<br>On: link ok<br>Flash: TX/RX | Off: 10 Mbps<br>On: 100 Mbps | Off: half duplex<br>On: full duplex<br>Flash: collision |

| | | | | | |
|---|---|---|---|---|---|
| 30 | 1[12] | 3[4] | R/W | REDUCE_IPG<br>This function reduce the IPG by random from 0 ~ 20 PPM.<br>1: enable, 0:disable | 1'b1 |
| 30 | 1[11] | 3[3] | R/W | Drop16<br>1: enable, 0:disable | 1'b0 |
| 30 | 1[10] | 3[2] | R/W | X_EN<br>IEEE 802.3x flow control enable<br>1: enable, 0:disable | P(1) |
| 30 | 1[9] | 3[1] | R/W | MOD_CARRIER_ALGORITHM<br>Modified carrier based collision algorithm<br>1: enable, 0:disable | 1'b0 |
| 30 | 1[8] | 3[0] | R/W | BK_EN, Backpressure enable<br>1: enable, 0: disable | P(1) |
| 30 | 1[7] | 2[7] | R/W | BP_KIND, Backpressure type selection<br>It is valid only if BK_EN is set to 1'b1.<br><br>0: carrier base backpressure<br>1: reserved | 1'b0 |
| 30 | 1[6] | 2[6] | R/W | BF_STM_EN, Broadcast storm enable<br>1: enable<br>IP178D drops the incoming packet if the number of broadcast packet in queue is over the threshold.<br>0: disable | P(0) |

## 5.5 Switch control registers (III)

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 30 | 1[5] | 2[5] | R/W | MLT3_DET<br>Ability for detecting MLT3 (for 10 Mbps switch to 100 Mbps)<br>0: disable MLT3 detection ability (default)<br>1: enable MLT3 detection ability. | P(0) |
| 30 | 1[4] | 2[4] | R/W | APS_DIS<br>Disable advanced power saving mode<br>0: enable advance power saving mode (default)<br>1: disable advance power saving mode | P(0) |
| 30 | 1[3:2] | 2[3:2] | R/W | AGING. Aging time of address table selection<br>An address tag in hashing table will be removed if this function is turned on and its aging timer expires. | P(1,0) |
| | | | | 00 — no aging | |
| | | | | 01 — 30s | |
| | | | | 10 — 300s (default) | |
| | | | | 11 — reserved | |
| 30 | 1[1] | 2[1] | R/W | MODBCK. Turn on modified back off algorithm<br>The maximum back off period is limited to 8-slot time if this function is turned on.<br>1: turn on, 0: turn off | P(1) |
| 30 | 1[0] | 2[0] | R/W | Drop extra long packet<br>Max forwarded packet length<br><br>0: 1536 bytes (default)<br>1: 1552 bytes | P(0) |

## 5.6 Test mode control registers

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| **Test mode control registers** | | | | | |
| 30 | 2[15:10] | 5[7:2] | R/W | TMODE_SEL. Test mode selection<br>This function is for testing only. The default value must be adopted for normal operation. | 6'b0 |
| 30 | 2[9] | 5[1] | R/W | MDI_MDIX_EN. Auto MDIMDIX enable<br>1: Auto MDIMDIX (default)<br>0: fixed MDI<br>Note: IP178D always uses a MDIX transformer. | P(1) |
| 30 | 2[8] | | | Reserved | |
| 30 | 2[7] | 4[7] | R/W | INPUT_FILTER<br>Packet is filtered in input port.<br>1: perform input filtering when queue full<br>0: no operation (default) | 0 |
| 30 | 2[6:5] | 4[6:5] | R/W | HASH_MODE<br>MAC address table hashing mode<br>00: direct + CRC mapping (default)<br>11: direct mapping | 2'b00 |
| 30 | 2[4:1] | | | Reserved | |
| 30 | 2[0] | 4[0] | R/W | BI_COLOR<br>Bi-color LED mode<br>0: disable (default)<br>1: enable | P(0) |

## 5.7 Port mirroring control registers

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 30 | 3[15] | 6[7] | R/W | PORT_MIRROR_EN | 1'b0 |
| | 3[14:13] | 6[6:5] | R/W | PORT_MIRROR_MODE<br>Select a mirror mode to monitor<br>00: mirror one port of RX (default)<br>01: mirror one port of TX<br>10: mirror source-destination pair<br>(TX and RX port should be different)<br>11: mirror one port of TX and RX<br>(TX and RX port must be the same) | 2'b00 |
| | 3[12:8] | | | Reserved | |
| | 3[7:0] | 7[7:0] | R/W | SEL_RX_PORT_MIRROR<br>Select the source (receive) port to be mirrored<br>0000_0001: port 0 (default)<br>0000_0010: port 1<br>0000_0100: port 2<br>0000_1000: port 3<br>0001_0000: port 4<br>0010_0000: port 5<br>0100_0000: port 6<br>1000_0000: port 7 | 8'h01 |
| | 4[15:13] | 6[2:0] | R/W | SEL_MIRROR_PORT<br>Select a mirror port to monitor any other port<br>000: port 0<br>001: port 1<br>010: port 2<br>011: port 3<br>100: port 4<br>101: port 5<br>110: port 6<br>111: port 7 (default) | 3'b111 |
| | 4[12:8] | | | Reserved | |
| | 4[7:0] | 8[7:0] | R/W | SEL_TX_PORT_MIRROR<br>Select the destination (transmit) port to be mirrored<br>0000_0001: port 0 (default)<br>0000_0010: port 1<br>0000_0100: port 2<br>0000_1000: port 3<br>0001_0000: port 4<br>0010_0000: port 5<br>0100_0000: port 6<br>1000_0000: port 7 | 8'h01 |

### 5.8 Fiber duplex setting registers

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 30 | 13[15:14] | 9[7:6] | R/W | FIBER_DUPLEX<br>Fiber duplex setting for each port.<br>1: fiber port is full-duplex<br>0: fiber port is half_duplex<br>bit[15]: port 7 duplex ability setting<br>bit[14]: port 6 duplex ability setting | 2'b11 |
| 30 | 13.13 | 9[5] | R/W | BUF_AGING_EN | 1'b0 |
| 30 | 13.12 | 9[4] | R/W | SRC_BLK_PROTECT | 1'b1 |
| 30 | 13[13:8] | | | Reserved | |

### 5.9 Backpressure setting registers

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 30 | 13[7:0] | -- | R/W | PORT_BACKPRESSURE_EN<br>Backpressure ability setting at half-duplex mode for each port. To ensure this function works correctly, BK_EN (backpressure enable, reg 30.1[8]) should set to logic zero first.<br>1: enable backpressure ability<br>0: disable<br>bit[7]: port 7 enable backpressure ability<br>bit[6]: port 6 enable backpressure ability<br>bit[5]: port 5 enable backpressure ability<br>bit[4]: port 4 enable backpressure ability<br>bit[3]: port 3 enable backpressure ability<br>bit[2]: port 2 enable backpressure ability<br>bit[1]: port 1 enable backpressure ability<br>bit[0]: port 0 enable backpressure ability | 8'h00 |

## 5.10 TCP/UDP port priority registers

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 30 | 14[15:8] | 19[7:0] | R/W | LPP_AGING_EN<br>TCP/UDP logical port priority aging enable<br>0: disable TCP/UDP logical port priority aging function<br>1: enable TCP/UDP logical port priority aging function<br>When this function active, once receive a IP frame with TCP/UDP protocol and the logical port number is the pre-defined port number, the ingress port will treat as a port based high priority port for 300 seconds. After the internal timer expired, the ingress port will change back to previous behavior.<br>bit[15]: port 7 logical port priority aging enable<br>bit[14]: port 6 logical port priority aging enable<br>bit[13]: port 5 logical port priority aging enable<br>bit[12]: port 4 logical port priority aging enable<br>bit[11]: port 3 logical port priority aging enable<br>bit[10]: port 2 logical port priority aging enable<br>bit[9]: port 1 logical port priority aging enable<br>bit[8]: port 0 logical port priority aging enable | P(0) |
| 30 | 14[7:6] | | | Reserved | |
| 30 | 14[5:4] | 10[5:4] | R/W | USERDEF_RANGE_EN<br>User defined logic port range enable.<br>bit[5]: user define range 1 register enable<br>bit[4]: user define range 0 register enable | 2'b11 |
| 30 | 14[3:0] | 10[3:0] | R/W | PREDEF_PORT_EN<br>Pre-defined logic port number enable.<br>bit[3]: logic port set 3 enable, port 6000<br>bit[2]: logic port set 2 enable, port 3389<br>bit[1]: logic port set 1 enable, port 443<br>bit[0]: logic port set 0 enable, port 22 | 4'hF |
| 30 | 15 | 12, 11 | R/W | USERDEF_RANGE0_HIGH<br>User defined logic port range 0 high limit | 16'd23 |
| 30 | 16 | 14, 13 | R/W | USERDEF_RANGE0_LOW<br>User defined logic port range 0 low limit | 16'd23 |
| 30 | 17 | 16.15 | R/W | USERDEF_RANGE1_HIGH<br>User defined logic port range 1 high limit | 16'd 5800 |
| 30 | 18 | 18.17 | R/W | USERDEF_RANGE1_LOW<br>User defined logic port range 1 low limit | 16'd 5800 |

### 5.11 CoS control registers – port 0

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 31 | 0[10] | 65[2] | R/W | Port 0 Class of service enable<br>1: enable, 0: disabled (default)<br>Packets with high priority tag from port 0 are handled as high priority packets. | 1'b0 |
| | 0[9] | 65[1] | R/W | Port 0 set to be high priority port<br>1: enable, 0: disabled (default)<br>Packets received from port 0 are handled as high priority packets. | 1'b0 |

### 5.12 CoS control registers – port 1

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 31 | 1[10] | 67[2] | R/W | Port 1 Class of service enable<br>1: enable, 0: disabled (default)<br>Packets with high priority tag from port 1 are handled as high priority packets. | 1'b0 |
| | 1[9] | 67[1] | R/W | Port 1 set to be high priority port<br>1: enable, 0: disabled (default)<br>Packets received from port 1 are handled as high priority packets. | 1'b0 |

### 5.13 CoS control registers – port 2

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 31 | 2[10] | 69[2] | R/W | Port 2 Class of service enable<br>1: enable, 0: disabled (default)<br>Packets with high priority tag from port 2 are handled as high priority packets. | 1'b0 |
| | 2[9] | 69[1] | R/W | Port 2 set to be high priority port<br>1: enable, 0: disabled (default)<br>Packets received from port 2 are handled as high priority packets. | 1'b0 |

### 5.14 CoS control registers – port 3

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 31 | 3[10] | 71[2] | R/W | Port 3 Class of service enable<br>1: enable, 0: disabled (default)<br>Packets with high priority tag from port 3 are handled as high priority packets. | 1'b0 |
| | 3[9] | 71[1] | R/W | Port 3 set to be high priority port<br>1: enable, 0: disabled (default)<br>Packets received from port 3 are handled as high priority packets. | 1'b0 |

### 5.15 CoS control registers – port 4

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| **CoS and port base VLAN register 4** | | | | | |
| 31 | 4[10] | 73[2] | R/W | Port 4 Class of service enable<br>1: enable, 0: disabled (default)<br>Packets with high priority tag from port 4 are handled as high priority packets. | 1'b0 |
| | 4[9] | 73[1] | R/W | Port 4 set to be high priority port<br>1: enable, 0: disabled (default)<br>Packets received from port 4 are handled as high priority packets. | 1'b0 |

### 5.16 CoS control registers – port 5

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 31 | 5[10] | 75[2] | R/W | Port 5 Class of service enable<br>1: enable, 0: disabled (default)<br>Packets with high priority tag from port 5 are handled as high priority packets. | 1'b0 |
| | 5[9] | 75[1] | R/W | Port 5 set to be high priority port<br>1: enable, 0: disabled (default)<br>Packets received from port 5 are handled as high priority packets. | 1'b0 |

### 5.17 CoS control registers – port 6

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 31 | 6[10] | 77[2] | R/W | Port 6 Class of service enable<br>1: enable, 0: disabled (default)<br>Packets with high priority tag from port 6 are handled as high priority packets. | 1'b0 |
| | 6[9] | 77[1] | R/W | Port 6 set to be high priority port<br>1: enable, 0: disabled (default)<br>Packets received from port 6 are handled as high priority packets. | 1'b0 |

### 5.18 CoS control registers – port 7

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 31 | 7[10] | 79[2] | R/W | Port 7 Class of service enable<br>1: enable, 0: disabled (default)<br>Packets with high priority tag from port 7 are handled as high priority packets. | 1'b0 |
| | 7[9] | 79[1] | R/W | Port 7 set to be high priority port<br>1: enable, 0: disabled (default)<br>Packets received from port 7 are handled as high priority packets. | 1'b0 |

### 5.19 Switch control registers (IV)

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| 31 | 9[15:14] | 83[7:6] | R/W | BF_STM_THR_SEL[1:0].<br>Broadcast storm threshold selection<br>00: 2 packets/10ms for 100Mbps port, or 2 packets/100ms for 10Mbps port,<br>01: 6 packets/10ms for 100Mbps port, or 6 packets/100ms for 10Mbps port,<br>10: 14 packets/10ms for 100Mbps port, or 14 packets/100ms for 10Mbps port,<br>11: 30 packets/10ms for 100Mbps port, or 30 packets/100ms for 10Mbps port | 2'b00 |
| | 9[13:12] | 83[5:4] | R/W | SHARE_FULL_THR_SEL[1;0].<br>Share buffer threshold selection<br>00: 160 units<br>01: 180 units<br>10: 140 units<br>11: 120 units | 2'b00 |
| | 9[11:10] | 83[3:2] | R/W | UNIT_DEFAULT_THR_SEL[1:0].<br>Output Queue minimum threshold selection<br>00: 40 units<br>01: 32 units<br>10: 48 units<br>11: 56 units | 2'b00 |
| | 9[9:8] | 83[1:0] | R/W | UNIT_LOW_THR_SEL | 2'b00 |
| | 9[7:6] | 82[7:6] | R/W | UNIT_HIGH_THR_SEL[1;0].<br>Output Queue Flow control ON threshold selection<br>If share buffer is over share buffer full threshold, Output Queue Flow control ON threshold will be dynamic changed to 28.<br>Others,<br>00: 50 units<br>01: 70 units<br>10: 90 units<br>11: 110 units | 2'b00 |
| | 9[5] | | | Reserved | |
| | 9[4] | 82[4] | R/W | PREDROP_EN<br>1: Drop an incoming broadcast packet if any port is congested.<br>0: forward an incoming broadcast packet to un-congested ports instead of congested ports. | 0 |
| | 9[3:2] | 82[3:2] | R/W | PKT_LOW_THR_SEL[1:0].<br>Packet low water mark threshold selection<br>00: 40 units<br>01: 30 units<br>10: 20 units<br>11: 10 units | 2'b00 |

| PHY | MII | ROM | R/W | Description | Default |
|---|---|---|---|---|---|
| | 9[1:0] | 82[1:0] | R/W | PKT_HIGH_THR_SEL[1:0].<br>Packet high water mark threshold selection<br>00: 50 units<br>01: 40 units<br>10: 30 units<br>11: 20 units | 2'b00 |

## 5.20 Switch control registers (V)

| PHY | MII | ROM | R/W | Description | | Default |
|---|---|---|---|---|---|---|
| 31 | 30[15:8] | 125 | R/W | [15:14]: Reserved<br>[13]: DIFFSERV_EN<br>[12]: BF_FFFF_ONLY<br>1: broadcast DA=FFFFFFFF<br>0: broadcast DA=FFFFFFFF and multicast frame | | 8'h0d |
| | | | | [11:8]: special_add_forward | | |
| | | | | bit 3 | Reserved MAC address (0180C2000010-0180C20000FF)<br>1: forward (default),<br>0: discard. | |
| | | | | bit 2 | Reserved MAC address (0180C2000002- 0180C200000F)<br>1: forward (default),<br>0: discard.<br>The default value is the inverted value of pin 78 FILTER_RSV_DA. | |
| | | | | bit 1 | Reserved MAC address (0180C2000001)<br>1: forward,<br>0: discard (default) | |
| | | | | bit 0 | Reserved MAC address (0180C2000000)<br>1: forward (default)<br>0: discard | |
| | 30[7:0] | | | Reserved | | |

## 6 Crystal Specifications

| Item | Parameter | Range |
|---|---|---|
| 1 | Nominal Frequency | 25.000 MHz |
| 2 | Oscillation Mode | Fundamental Mode |
| 3 | Frequency Tolerance at 25℃ | +/- 50 ppm |
| 4 | Temperature Characteristics | +/- 50 ppm |
| 5 | Operating Temperature Range | -10℃ ~ +70℃ |
| 6 | Equivalent Series Resistance | 40 ohm Max. |
| 7 | Drive Level | 100 μW |
| 8 | Load Capacitance | 20 pF |
| 9 | Shunt Capacitance | 7 pF Max |
| 10 | Insulation Resistance | Mega ohm Min./DC 100V |
| 11 | Aging Rate A Year | +/- 5 ppm/year |

# 7 Electrical Characteristics

## 7.1 Absolute Maximum Rating

Stresses exceed those values listed under Absolute Maximum Ratings may cause permanent damage to the device. Functional performance and device reliability are not guaranteed under these conditions. All voltages are specified with respect to GND.

| | |
|---|---|
| Supply Voltage | – 0.3V to 4.0V |
| Input Voltage | – 0.3V to 5.0V |
| Output Voltage | – 0.3V to 5.0V |
| Storage Temperature | – 65°C to 150°C |
| Ambient Operating Temperature (Ta) (IP178D LF) | 0°C to 70°C |
| Ambient Operating Temperature (Ta) (IP178D LFI) | – 40 °C to 85°C |

## 7.2 DC Characteristic

**Operating Conditions**

| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Supply Voltage | VCC | 1.80 | 1.95 | 2.05 | V | |
| Supply Voltage | VCC_O | 3.135<br>2.25 | 3.3<br>2.5 | 3.465<br>2.75 | V | VCC_O =3.3V<br>VCC_O =2.5V |
| Power Consumption | | | 1.35 | | W | 100 Mbps full, VCC=1.95V |

**Input Clock**

| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Frequency | | | 25 | | MHz | |
| Frequency Tolerance | | -50 | | +50 | PPM | |

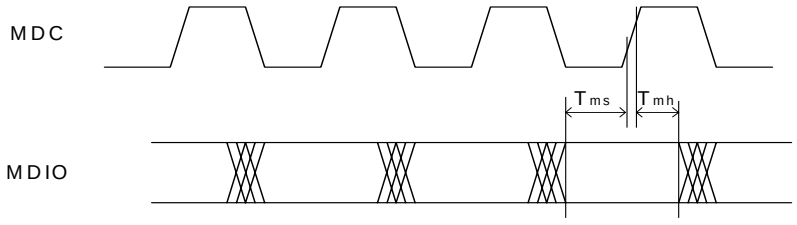
**I/O Electrical Characteristics**

| Parameter | Sym | Min. | Max. | Unit | Conditions |
|---|---|---|---|---|---|
| Input Low Voltage<br>-LED PAD direct mode<br>-LED PAD bicolor mode<br>-NOT LED PAD | VIL | | <br>0.39*VCC_O<br>0.36*VCC_O<br>0.4*VCC_O | V | |
| Input High Voltage<br>-LED PAD direct mode<br>-LED PAD bicolor mode<br>-NOT LED PAD | VIH | <br>0.58*VCC_O<br>0.58*VCC_O<br>0.6*VCC_O | | V | |
| Output Low Voltage | VOL | | 0.4 | V | IOH=4mA, VCC_O_x=3.3V |
| Output High Voltage | VOH | 2.4 | | V | IOL=4mA, VCC_O_x=3.3V |

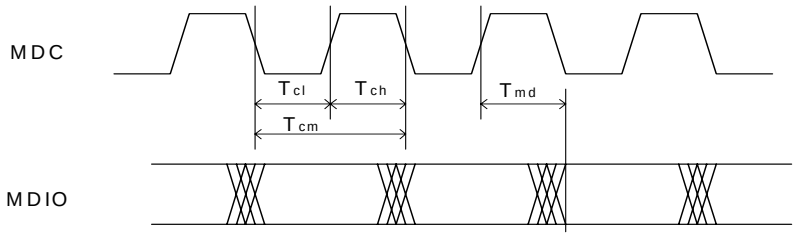
## 7.3 AC Timing

### 7.3.1 Serial Management Imierface Timing

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{ch}$ | MDC High Time | 40 | - | - | ns |
| $T_{cl}$ | MDC Low Time | 40 | - | - | ns |
| $T_{cm}$ | MDC period | 80 | - | - | ns |
| $T_{md}$ | MDIO output delay | - | - | 15 | ns |
| $T_{mh}$ | MDIO setup time | 10 | - | - | ns |
| $T_{ms}$ | MDIO hold time | 10 | - | - | ns |




**Write Cycle**

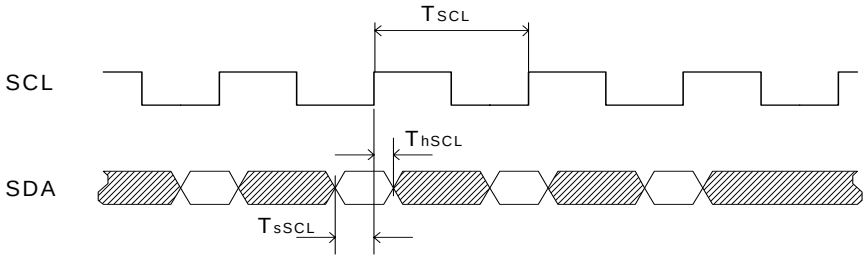



**Read Cycle**

### 7.3.2 EEPROM Timing

#### 7.3.2.1 Data read cycle

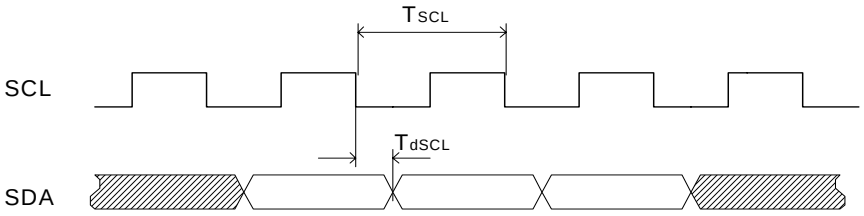
| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{SCL}$ | Receive clock period | - | 20480 | - | ns |
| $T_{sSCL}$ | SDA to SCL setup time | 2 | - | - | ns |
| $T_{hSCL}$ | SDA to SCL hold time | 0.5 | - | - | ns |




Read data cycle

#### 7.3.2.2 Command cycle

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{SCL}$ | Transmit clock period | - | 20480 | - | ns |
| $T_{dSCL}$ | SCL falling edge to SDA | - | - | 5200 | ns |




Comand cycle

## 7.4 Thermal Data

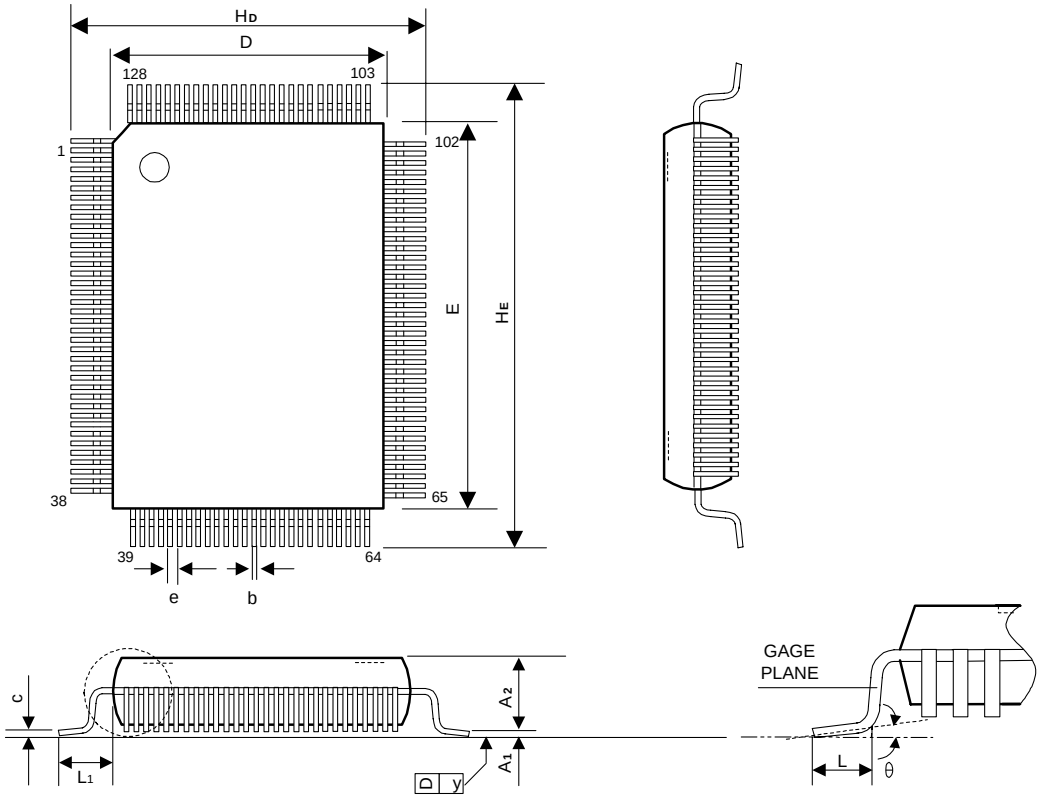
| Theta Ja | Theta Jc | Conditions | Units |
|---|---|---|---|
| 30.7~32.5 | 11.6~12.4 | 2 Layer PCB | $^{o}$C/W |
| 25.0~26.6 | 11.1~11.7 | 4 Layer PCB | $^{o}$C/W |

## 8 Order Information

| Part No. | Package | Notice |
|---|---|---|
| IP178D LF | 128-PIN PQFP | |
| IP178D LFI | 128-PIN PQFP | -40°C to 85°C |

# 9 Package Detail

## 128 PQFP Outline Dimensions




| Symbol | Dimensions In Inches | | | Dimensions In mm | | |
|---|---|---|---|---|---|---|
| | Min. | Nom. | Max. | Min. | Nom. | Max. |
| A1 | 0.010 | 0.014 | 0.018 | 0.25 | 0.35 | 0.45 |
| A2 | 0.107 | 0.112 | 0.117 | 2.73 | 2.85 | 2.97 |
| b | 0.007 | 0.009 | 0.011 | 0.17 | 0.22 | 0.27 |
| c | 0.004 | 0.006 | 0.008 | 0.09 | 0.15 | 0.20 |
| HD | 0.669 | 0.677 | 0.685 | 17.00 | 17.20 | 17.40 |
| D | 0.547 | 0.551 | 0.555 | 13.90 | 14.00 | 14.10 |
| HE | 0.906 | 0.913 | 0.921 | 23.00 | 23.20 | 23.40 |
| E | 0.783 | 0.787 | 0.791 | 19.90 | 20.00 | 20.10 |
| e | - | 0.020 | - | - | 0.50 | - |
| L | 0.025 | 0.035 | 0.041 | 0.65 | 0.88 | 1.03 |
| L1 | - | 0.063 | - | - | 1.60 | - |
| y | - | - | 0.004 | - | - | 0.10 |
| θ | 0° | - | 12° | 0° | - | 12° |

Note:
1. Dimension D & E do not include mold protrusion.
2. Dimension B does not include dambar protrusion. Total in excess of the B dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot.