# International IⓇR Rectifier

IRS2106/IRS21064(S)PbF

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V, 5 V, and 15 V input logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5 V offset
- Lower di/dt gate driver for better noise immunity
- Outputs in phase with inputs (IRS2106)
- RoHS compliant

Packages

8-Lead PDIP

14-Lead PDIP

8-Lead SOIC

14-Lead SOIC
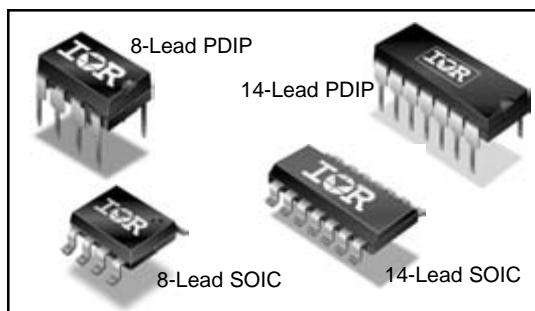
Description

The IRS2106/IRS21064 are high voltage, high speed power MOSFET and IGBT drivers with independent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic.

Feature Comparison

Part	Input logic	Cross-conduction prevention logic	Deadtime (ns)	Ground Pins	t_{on}/t_{off} (ns)
2106/2301	HIN/LIN	no	none	COM	220/200
21064				V_{SS}/COM	
2108	HIN/$\overline{LIN}$	yes	Internal 540	COM	220/200
21084			Programmable 540 - 5000	V_{SS}/COM	
2109/2302	IN/$\overline{SD}$	yes	Internal 540	COM	750/200
21094			Programmable 540 - 5000	V_{SS}/COM	
2304	HIN/LIN	yes	Internal 100	COM	160/140

The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 V.

Typical Connection

(Refer to Lead Assignments for correct pin configuration). These diagrams show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High-side floating absolute voltage		-0.3	625	V
V_S	High-side floating supply offset voltage		$V_B - 25$	$V_B + 0.3$	
V_{HO}	High-side floating output voltage		$V_S - 0.3$	$V_B + 0.3$	
V_{CC}	Low-side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low-side output voltage		-0.3	$V_{CC} + 0.3$	
V_{IN}	Logic input voltage		$V_{SS} - 0.3$	$V_{CC} + 0.3$	
V_{SS}	Logic ground (IRS21064 only)		$V_{CC} - 25$	$V_{CC} + 0.3$	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25\ °C$	(8 lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
		(14 lead PDIP)	—	1.6	
		(14 lead SOIC)	—	1.0	
Rth_{JA}	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
		(14 lead PDIP)	—	75	
		(14 lead SOIC)	—	120	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-50	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

IRS2106/IRS21064(S)PbF

Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at a 15 V differential.

Symbol	Definition	Min.	Max.	Units
VB	High-side floating supply absolute voltage	V_S + 10	V_S + 20	
V_S	High-side floating supply offset voltage	Note 1	600	
V_{HO}	High-side floating output voltage	V_S	V_B	
V_{CC}	Low-side and logic fixed supply voltage	10	20	V
V_{LO}	Low-side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage	V_{SS}	V_{CC}	
V_{SS}	Logic ground (IRS21064 only)	-5	5	
T_A	Ambient temperature	-40	125	$^\circ$C

Note 1: Logic operational for V_S of -5 V to +600 V. Logic state held for V_S of -5 V to -V_{BS}. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, V_{SS} = COM, C_L = 1000 pF, T_A = 25 °C.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	220	300		V_S = 0 V
t_{off}	Turn-off propagation delay	—	200	280		V_S = 0 V or 600 V
MT	Delay matching, HS & LS turn-on/off	—	0	30	ns	
t_r	Turn-on rise time	—	100	220		V_S = 0 V
t_f	Turn-off fall time	—	35	80		

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, V_{SS} = COM and T_A = 25 °C unless otherwise specified. The V_{IL}, $V_{IH,}$ and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to the respective input leads. The V_O, I_O, and R_{on} parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage	2.5	—	—		V_{CC} = 10 V to 20 V
V_{IL}	Logic "0" input voltage	—	—	0.8	V	
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	0.05	0.2		I_O = 2 mA
V_{OL}	Low level output voltage, V_O	—	0.02	0.1		
I_{LK}	Offset supply leakage current	—	—	50		V_B = V_S = 600 V
I_{QBS}	Quiescent V_{BS} supply current	20	75	130		V_{IN} = 0 V or 5 V
I_{QCC}	Quiescent V_{CC} supply current	60	120	180		
I_{IN+}	Logic "1" input bias current V_{IN} = 5 V	—	5	20	µA	
I_{IN-}	Logic "0" input bias current V_{IN} = 0 V	—	—	5		
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8		
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0	V	
V_{CCUVH} V_{BSUVH}	Hysteresis	0.3	0.7	—		
I_{O+}	Output high short circuit pulsed current	130	290	—	mA	V_O = 0 V, PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	270	600	—		V_O = 15 V, PW ≤ 10 µs

Functional Block Diagrams

IRS2106/IRS21064(S)PbF
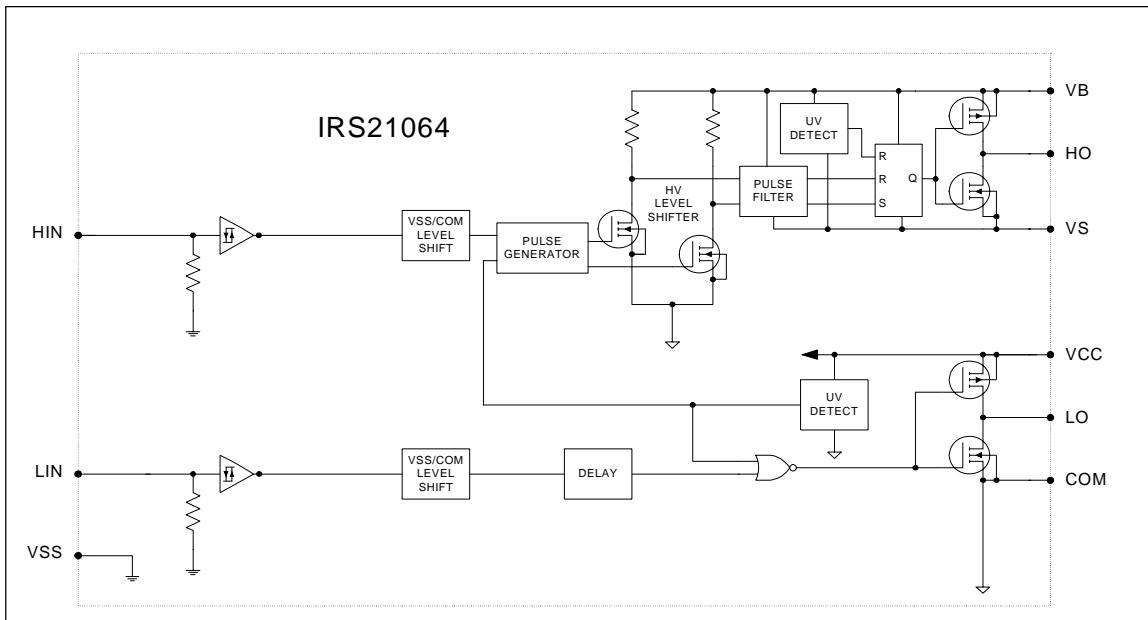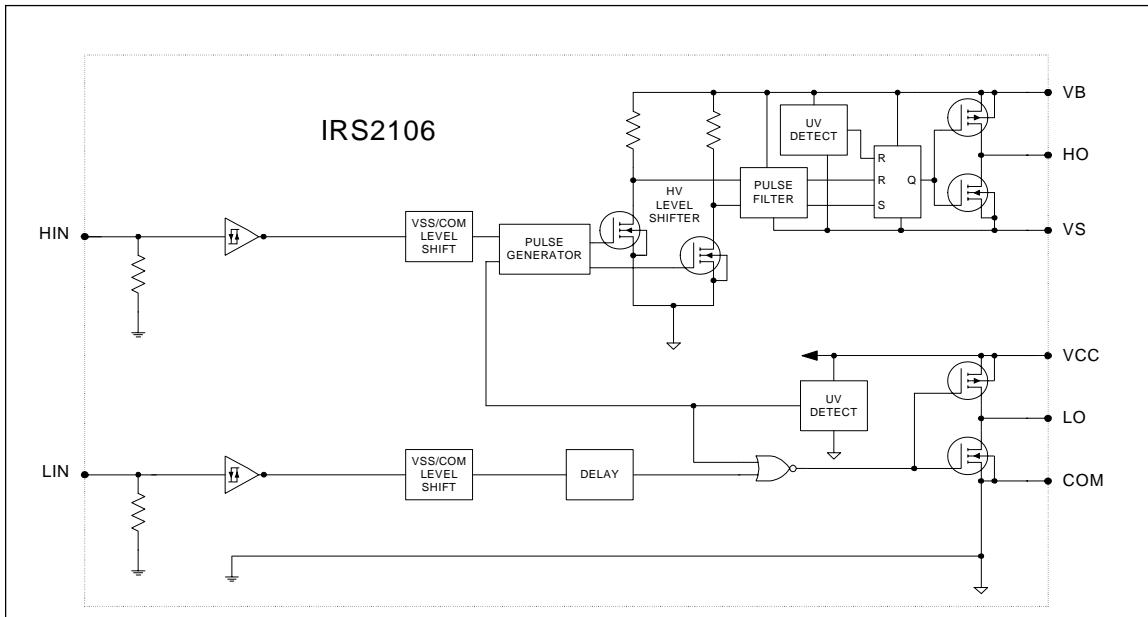
Lead Definitions

Symbol	Description
HIN	Logic input for high-side gate driver output (HO), in phase
LIN	Logic input for low-side gate driver output (LO), in phase
VSS	Logic ground (IRS21064 only)
V_B	High-side floating supply
HO	High-side gate drive output
V_S	High-side floating supply return
V_{CC}	Low-side and logic fixed supply
LO	Low-side gate drive output
COM	Low-side return

Lead Assignments
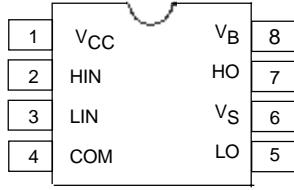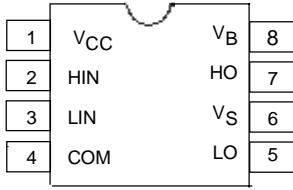
1 V_{CC} V_B 8 2 HIN HO 7 3 LIN V_S 6 4 COM LO 5 8 Lead PDIP	1 V_{CC} V_B 8 2 HIN HO 7 3 LIN V_S 6 4 COM LO 5 8 Lead SOIC
IRS2106PbF	**IRS2106SPbF**
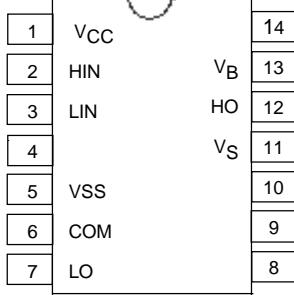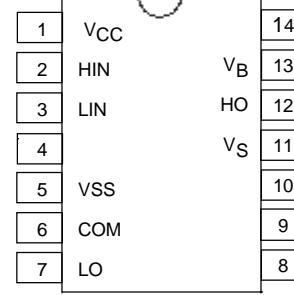
1 V_{CC} 14 2 HIN V_B 13 3 LIN HO 12 4 V_S 11 5 VSS 10 6 COM 9 7 LO 8 14 Lead PDIP	1 V_{CC} 14 2 HIN V_B 13 3 LIN HO 12 4 V_S 11 5 VSS 10 6 COM 9 7 LO 8 14 Lead SOIC
IRS21064PbF	**IRS21064SPbF**
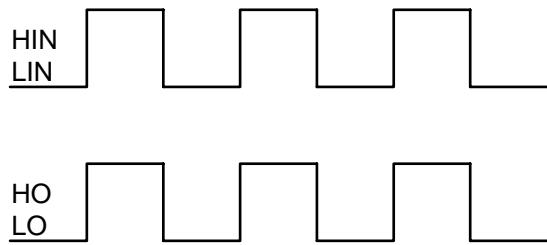
Figure 1. Input/Output Timing Diagram
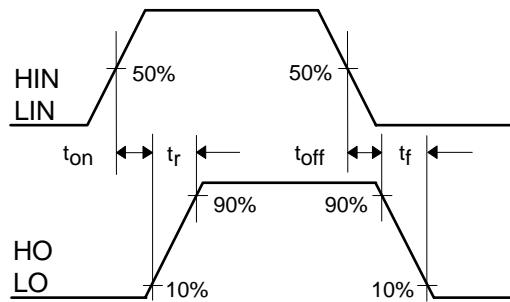
Figure 2. Switching Time Waveform Definitions
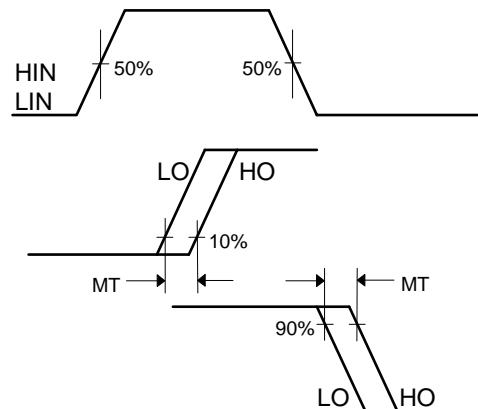
Figure 3. Delay Matching Waveform Definitions

IRS2106/IRS21064(S)PbF
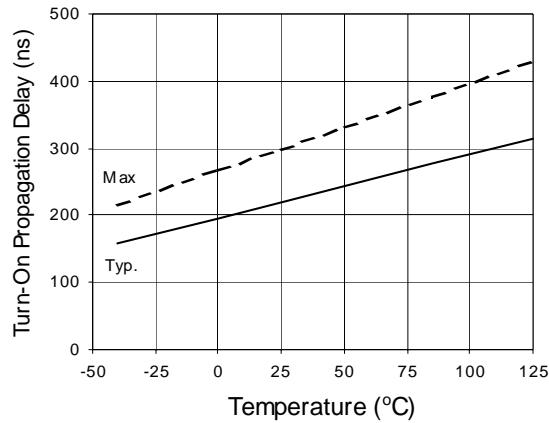
**Figure 4A. Turn-On Propagation Delay
vs. Temperature**
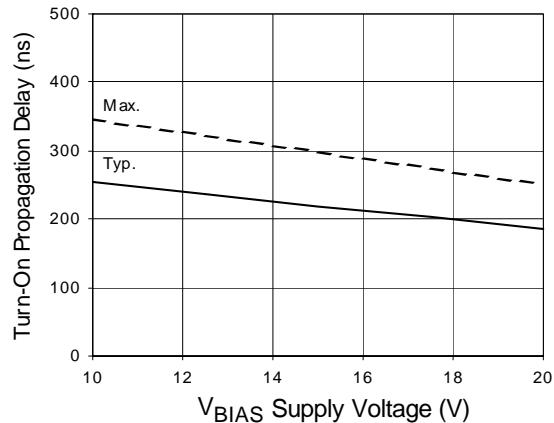
**Figure 4B. Turn-On Propagation Delay
vs. Supply Voltage**
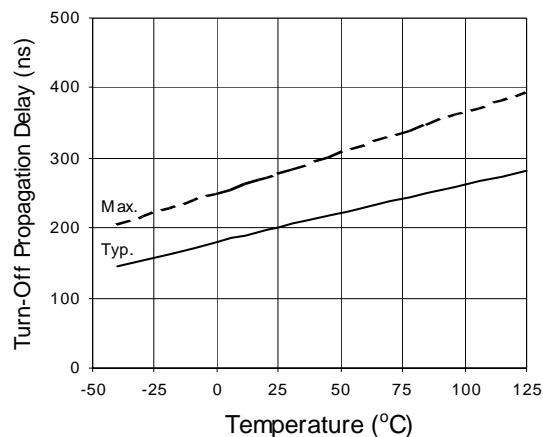
**Figure 5A. Turn-Off Propagation Delay
vs. Temperature**
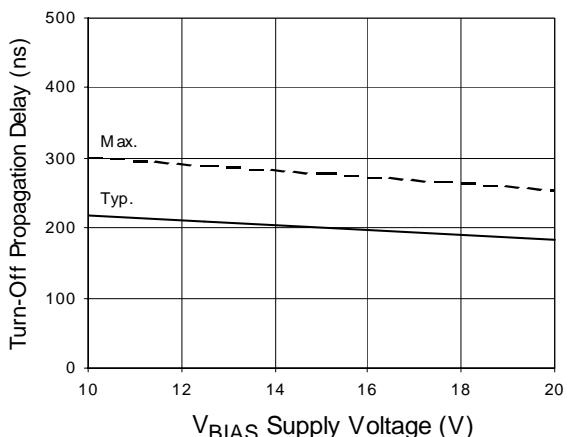
**Figure 5B. Turn-Off Propagation Delay
vs. Supply Voltage**
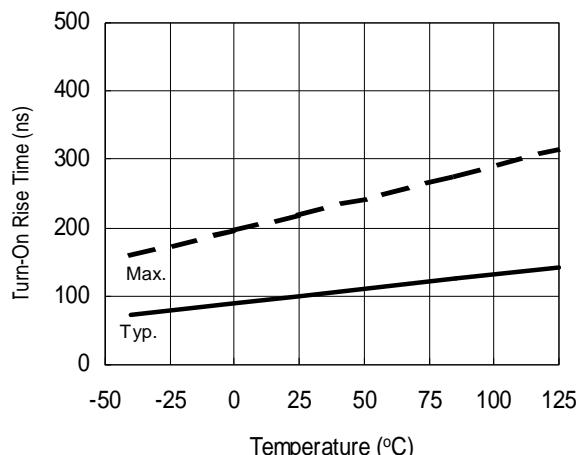
**Figure 6A. Turn-On Rise Time
vs. Temperature**
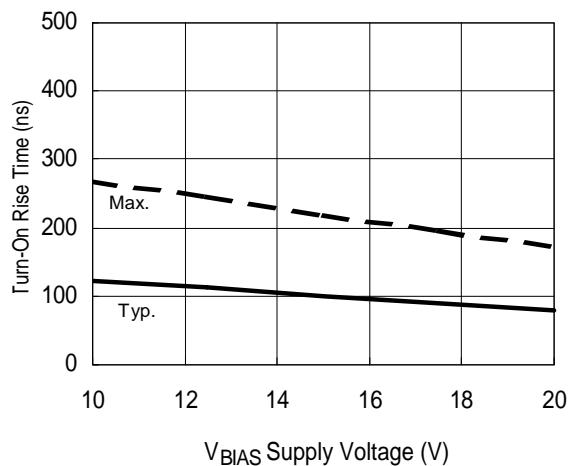
**Figure 6B. Turn-On Rise Time
vs. Supply Voltage**
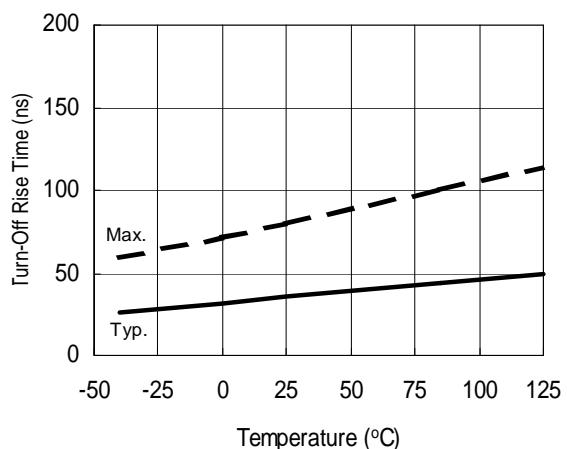
**Figure 7A. Turn-Off Fall Time
vs. Temperature**
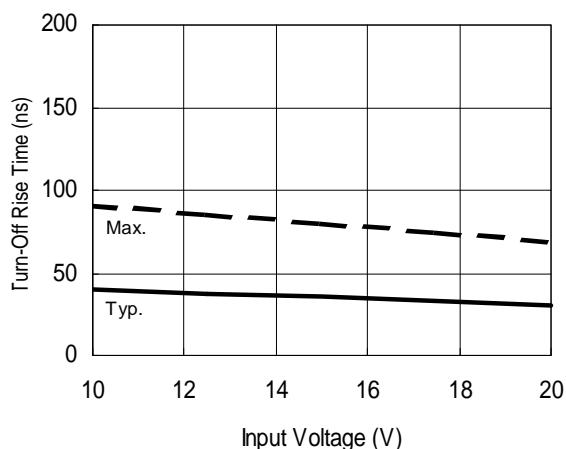
**Figure 7B. Turn-Off Fall Time
vs. Supply Voltage**

International
IOR Rectifier
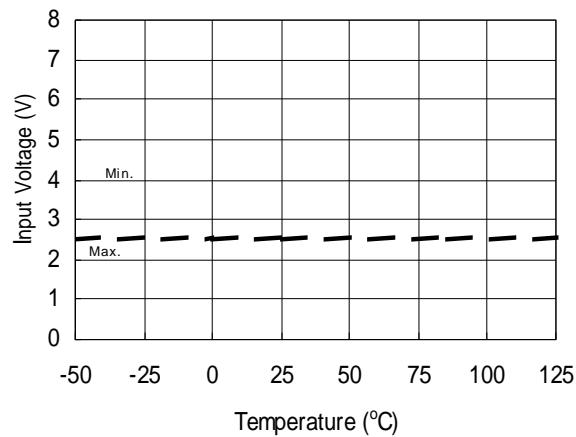
**Figure 8A. Logic "1" Input Voltage
vs. Temperature**
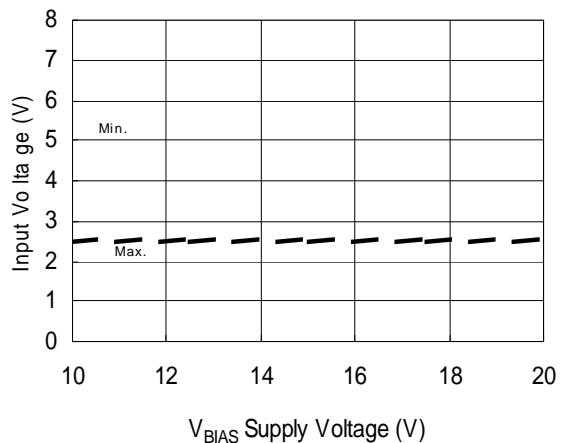
**Figure 8B. Logic "1" Input Voltage
vs. Supply Voltage**
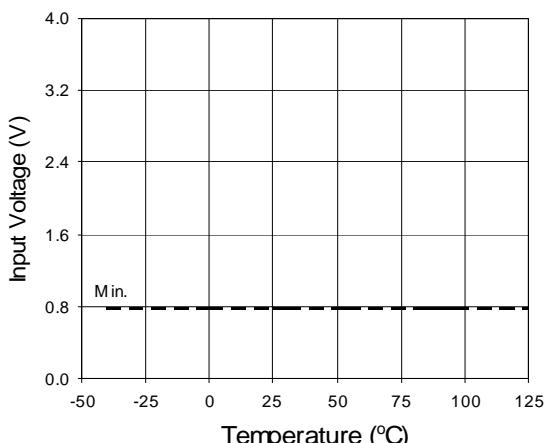
**Figure 9A. Logic "0" Input Voltage
vs. Temperature**
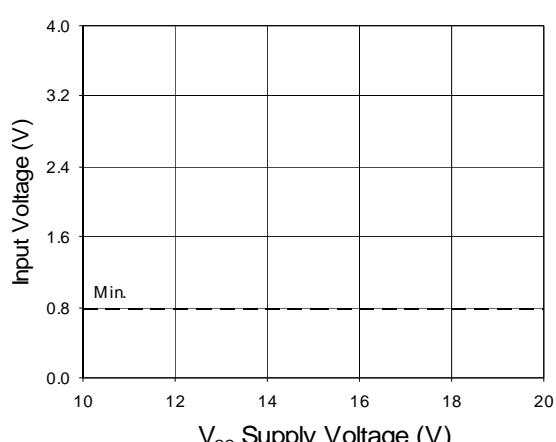
**Figure 9B. Logic "0" Input Voltage
vs. Supply Voltage**
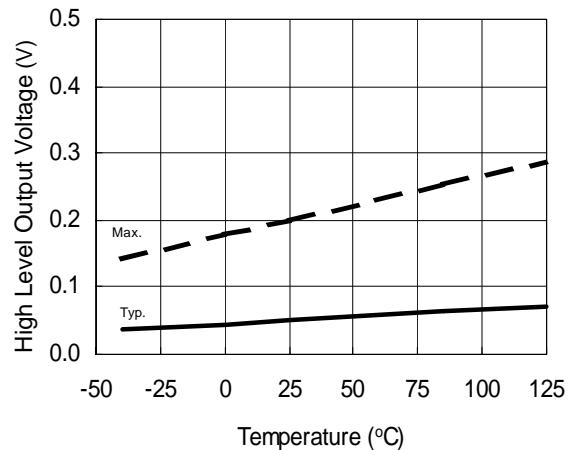
**Figure 10A. High Level Output Voltage
vs. Temperature**
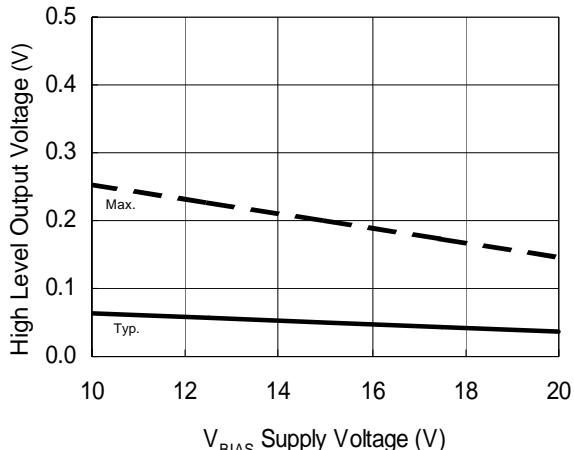
**Figure 10B. High Level Output Voltage
vs. Supply Voltage**
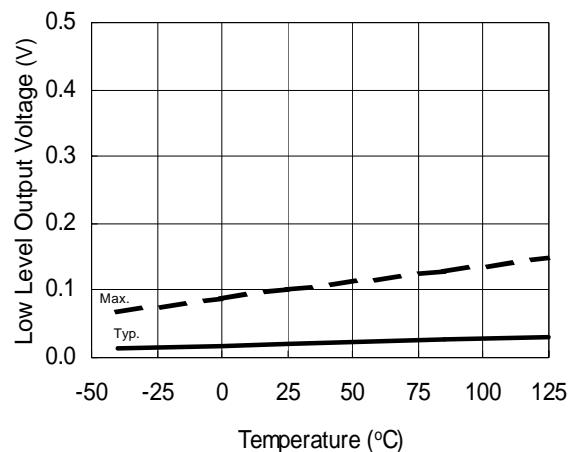
**Figure 11A. Low Level Output Voltage
vs. Temperature**
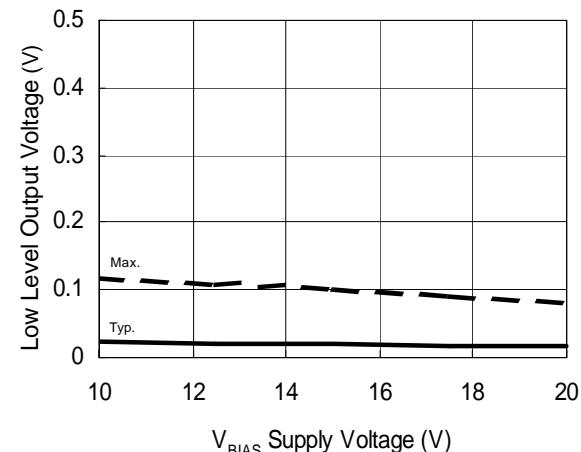
**Figure 11B. Low Level Output Voltage
vs. Supply Voltage**
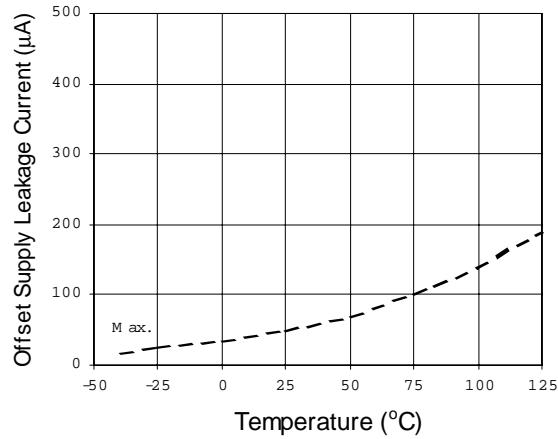
**Figure 12A. Offset Supply Leakage Current
vs. Temperature**
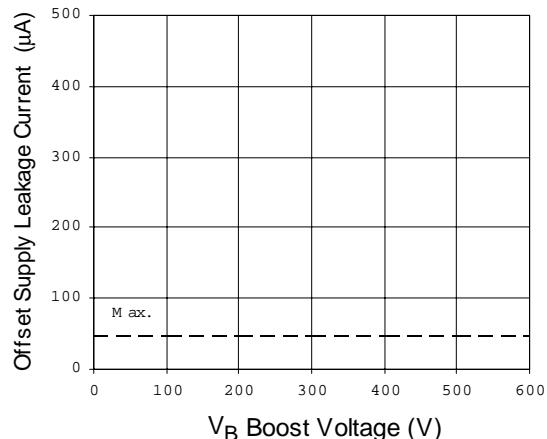
**Figure 12B. Offset Supply Leakage Current
vs. Supply Voltage**
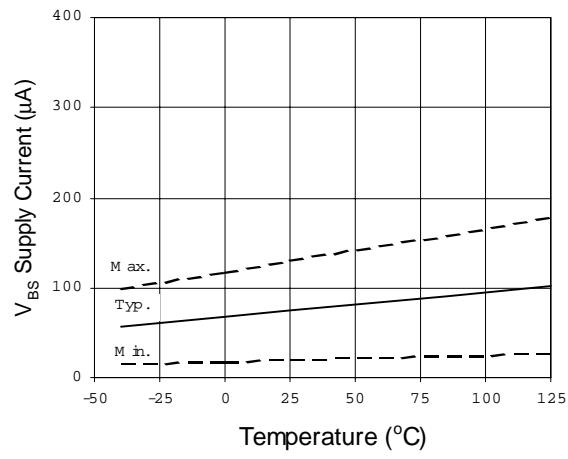
**Figure 13A. V$_{BS}$ Supply Current
vs. Temperature**
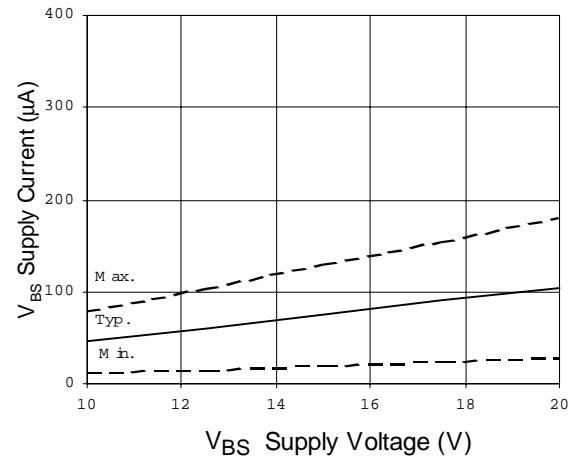
**Figure 13B. V$_{BS}$ Supply Current
vs. Supply Voltage**
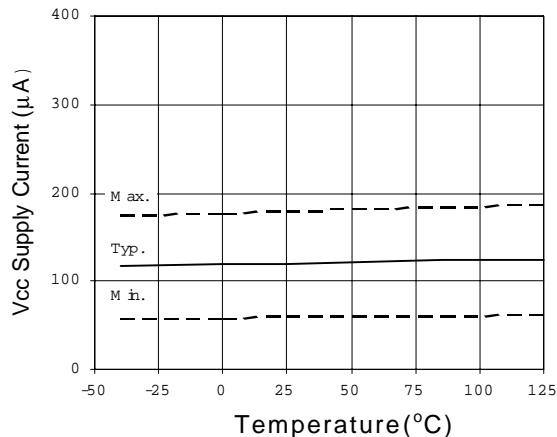
Figure 14A. Quiescent V_{CC} Supply Current vs. Temperature
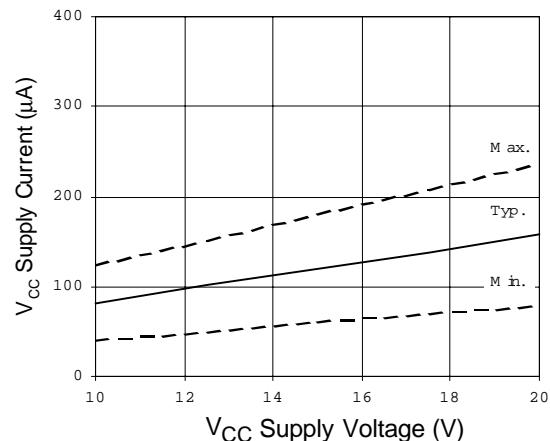
**Figure 14B. Quiescent V_{CC} Supply Current vs. V_{CC} Supply Voltage**
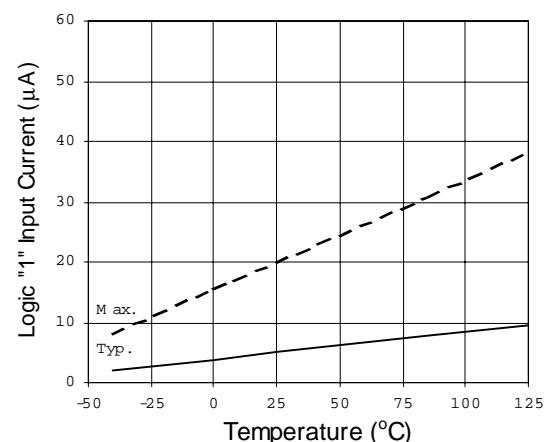
**Figure 15A. Logic "1" Input Current vs. Temperature**
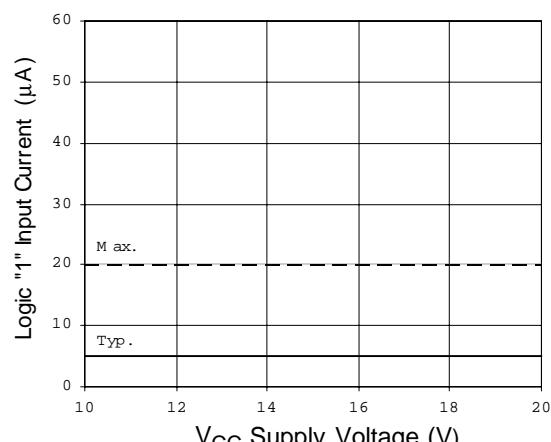
Figure 15B. Logic "1" Bias Current vs. Supply Voltage
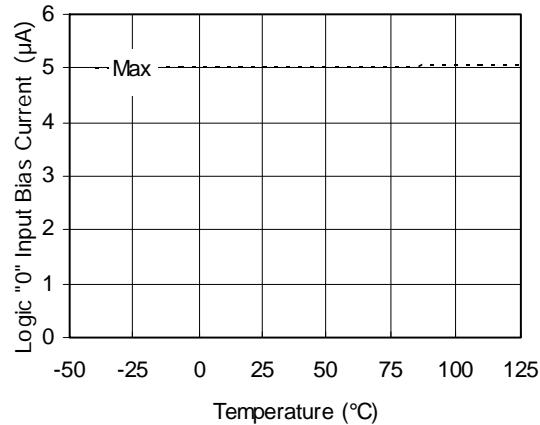
**Figure 16A. Logic "0" Input Bias Current
vs. Temperature**
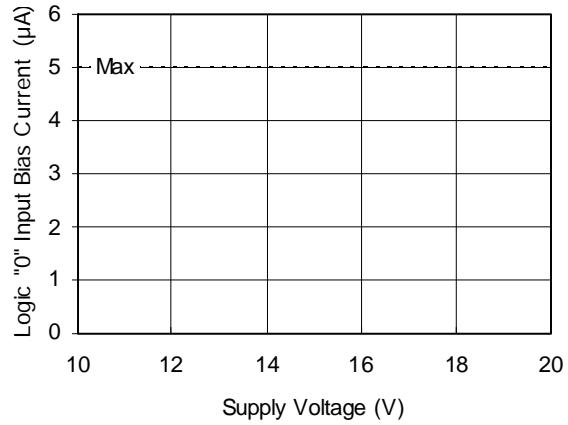
**Figure 16B. Logic "0" Input Bias Current
vs. Voltage**
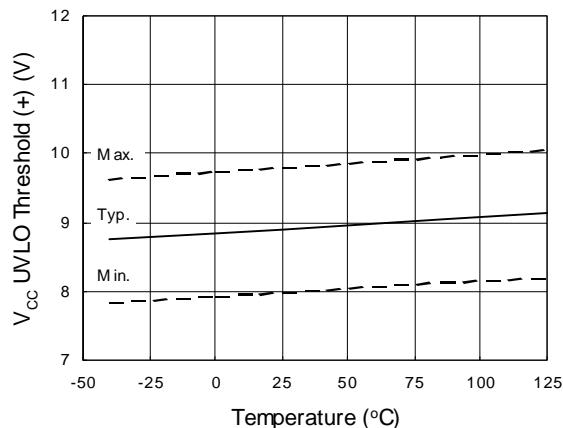
**Figure 17. V$_{CC}$ Undervoltage Threshold (+)
vs. Temperature**
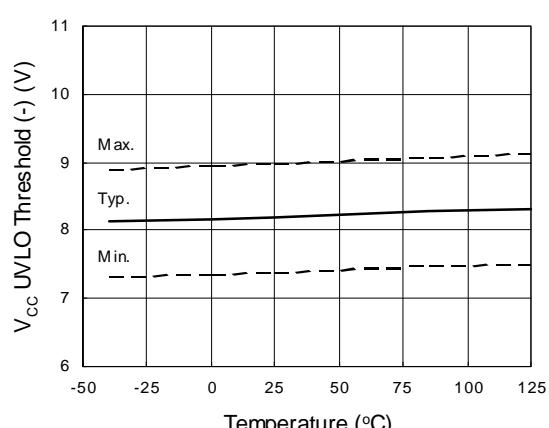
**Figure 18. V$_{CC}$ Undervoltage Threshold (-)
vs. Temperature**
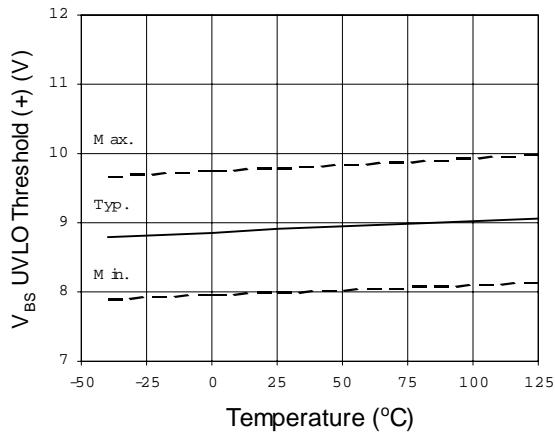
Figure 19. V$_{BS}$ Undervoltage Threshold (+)
vs. Temperature
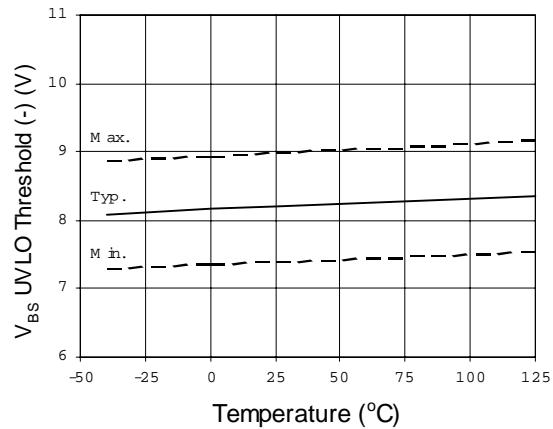
Figure 20. V$_{BS}$ Undervoltage Threshold (-)
vs. Temperature
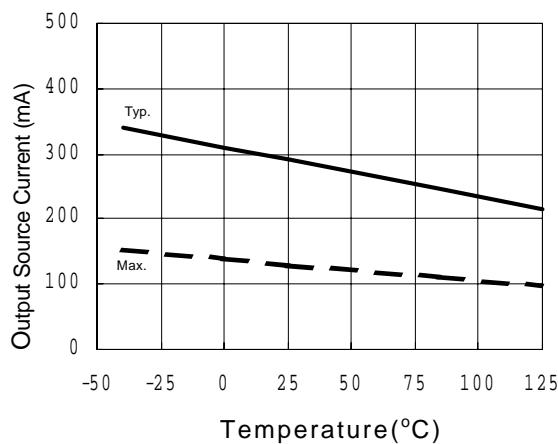
Figure 21A. Output Source Current
vs. Temperature
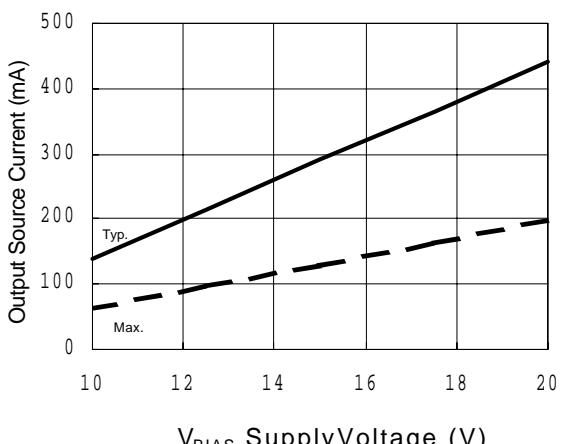
Figure 21B. Output Source Current
vs. Supply Voltage
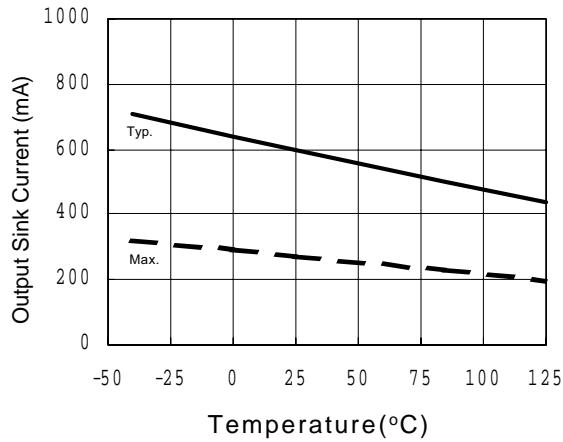
**Figure 22A. Output Sink Current
vs. Temperature**
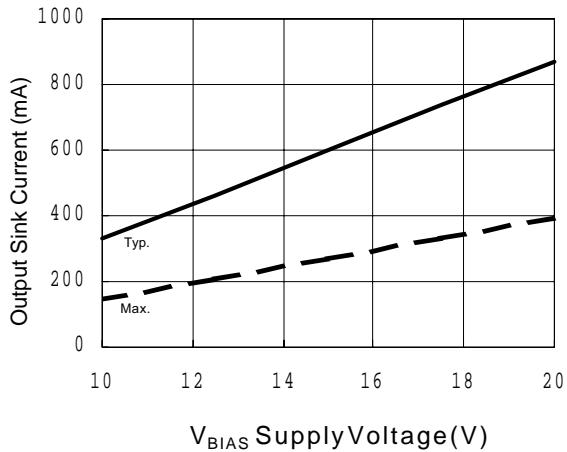
**Figure 22B. Output Sink Currentt
vs. Supply Voltage**
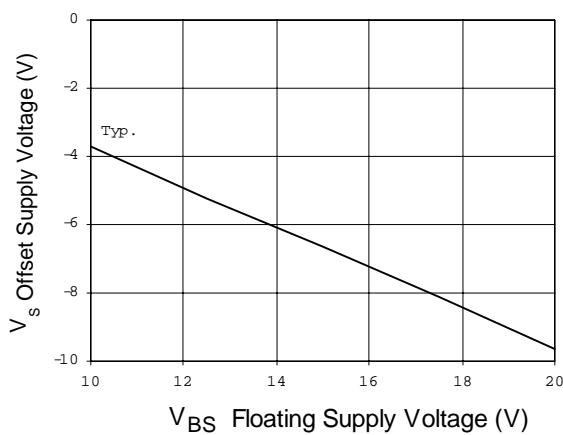
**Figure 23. Maximum V_S Negative Offset
vs. Supply Voltage**
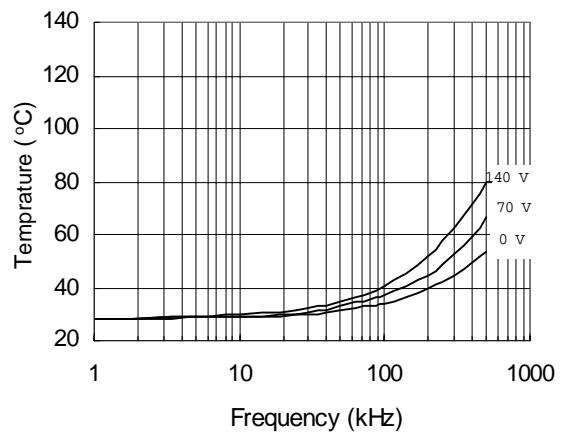
**Figure 24. IRS2106 vs. Frequency (IRFBC20),
Rgate=33 Ω, VCC=15 V**
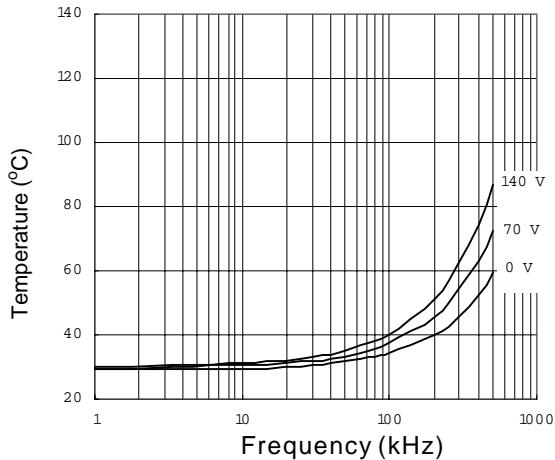
Figure 25. IRS2106 vs. Frequency (IRFBC30),
R_{gate}=22 Ω, V_{CC}=15 V
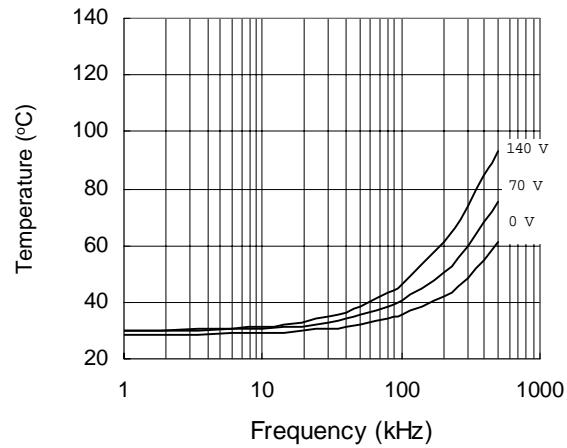
Figure 26. IRS2106 vs. Frequency (IRFBC40),
R_{gate}=15 Ω, V_{CC}=15 V
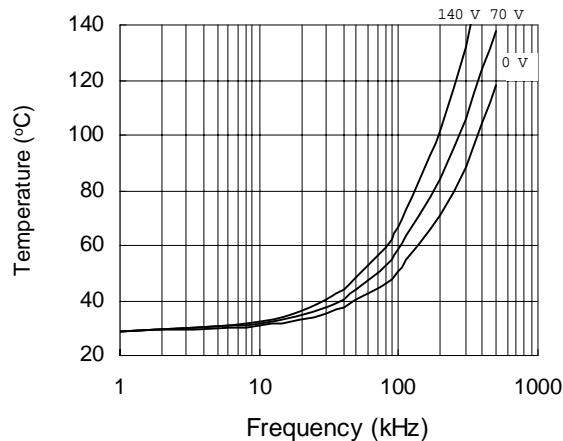
Figure 27. IRS2106 vs. Frequency (IRFPE50),
R_{gate}=10 Ω, V_{CC}=15 V
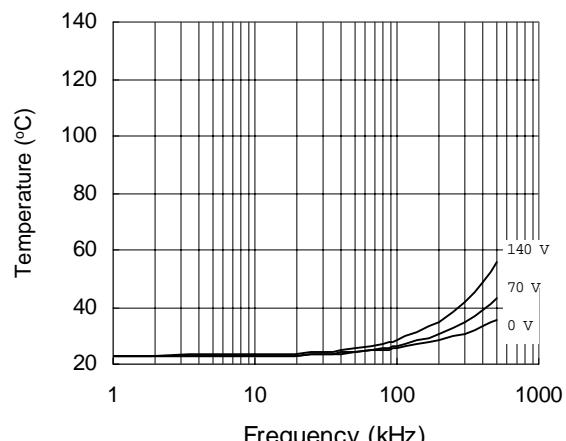
Figure 28. IRS21064 vs. Frequency (IRFBC20),
R_{gate}=33 Ω, V_{CC}=15 V

International
IOR Rectifier
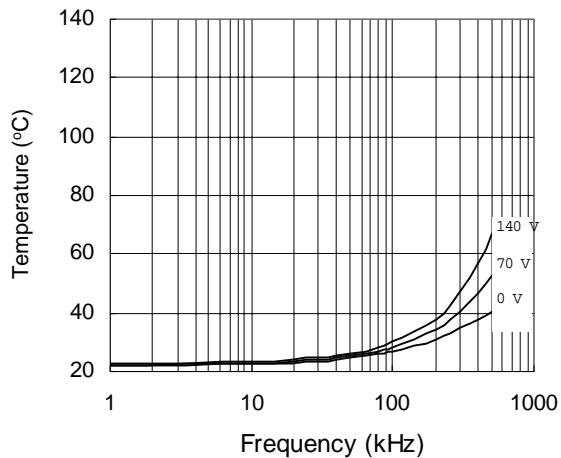
Figure 29. IRS21064 vs. Frequency (IRFBC30),
R_{gate}=22 Ω, V_{CC}=15 V
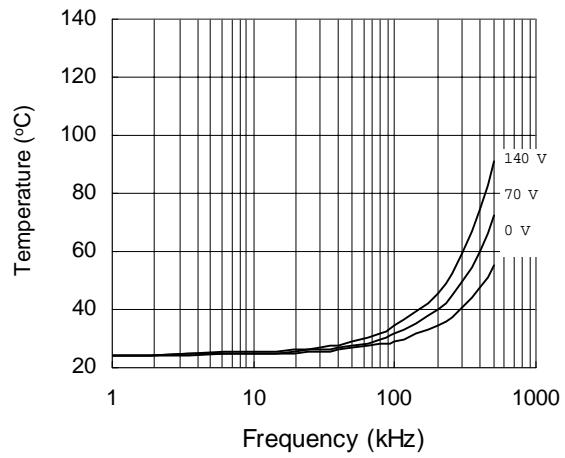
Figure 30. IRS21064 vs. Frequency (IRFBC40),
R_{gate}=15 Ω, V_{CC}=15 V
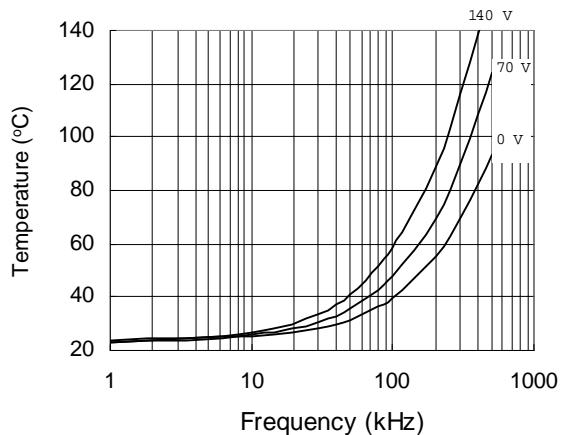
Figure 31. IRS21064 vs. Frequency (IRFPE50),
R_{gate}=10 Ω, V_{CC}=15 V
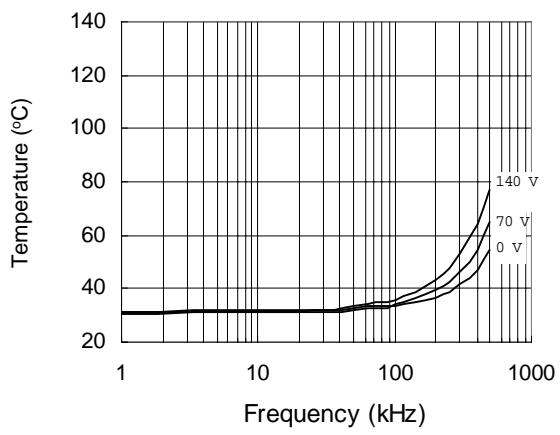
Figure 32. IRS2106S vs. Frequency (IRFBC20),
R_{gate}=33 Ω, V_{CC}=15 V
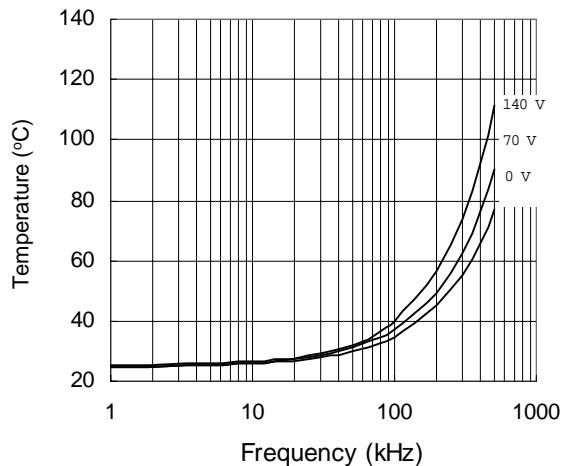
Figure 33. IRS2106S vs. Frequency (IRFBC30),
R_{gate}=22 Ω, V_{CC}=15 V
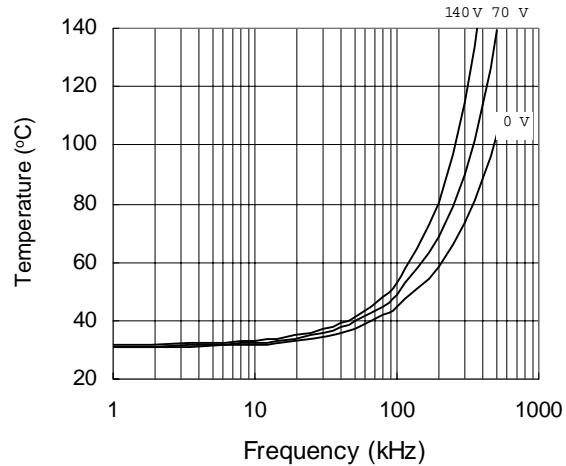
Figure 34. IRS2106S vs. Frequency (IRFBC40),
R_{gate}=15 Ω, V_{CC}=15 V
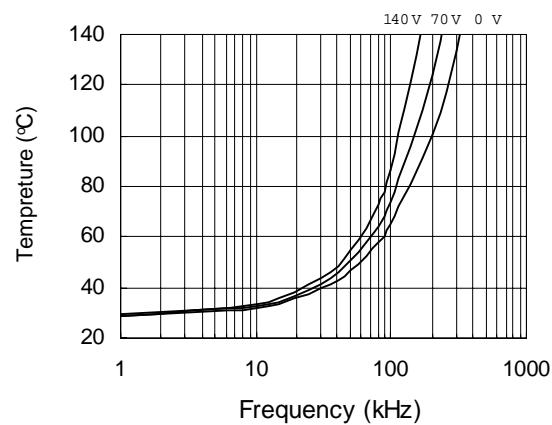
Figure 35. IRS2106S vs. Frequency (IRFPE50),
R_{gate}=10 Ω, V_{CC}=15 V
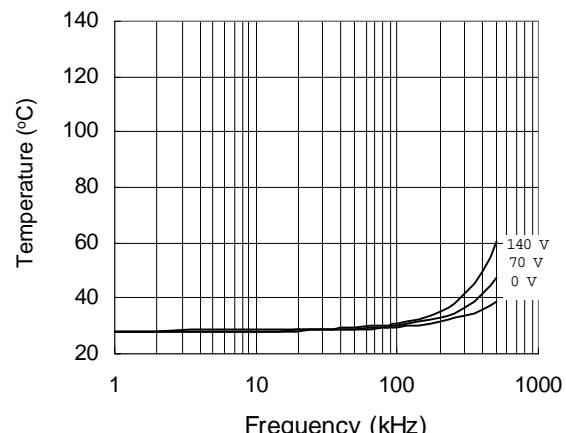
Figure 36. IRS21064S vs. Frequency (IRFBC20),
R_{gate}=33 Ω, V_{CC}=15 V
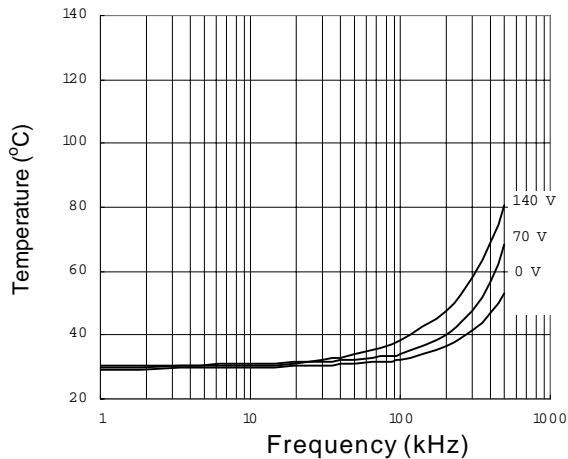
Figure 37. IRS21064S vs. Frequency (IRFBC30),
R_{gate}=22 Ω, V_{CC}=15 V

Figure 38. IRS21064S vs. Frequency (IRFBC40),
R_{gate}=15 Ω, V_{CC}=15 V

Figure 39. IRS21064S vs. Frequency (IRFPE50),
R_{gate}=10 Ω, V_{CC}=15 V

Case Outlines

NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M−1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS−001AB.
⑤ MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
⑥ DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

8 Lead PDIP

01-6014
01-3003 01 (MS-001AB)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

⑤ DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
⑥ DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
⑦ DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8 Lead SOIC

01-6027
01-0021 11 (MS-012AA)

14 Lead PDIP

20.19 [.795]
18.42 [.725]

−A−
⑥

14

7.11 [.280]
6.10 [.240]

−B−

1

14X 1.77 [.070]
1.15 [.045]

0.39 [.015]
MIN.

−C−

5.33 [.210]
MAX

4.06 [.160]
2.93 [.115]

2.54 [.100]
12X

14X 0.558 [.022]
0.356 [.014]

⊕ 0.25 [.010] Ⓜ C BⓈ AⓈ

14X 0° − 15°

7.62 [.300]
⑤

14X 0.381 [.015]
0.204 [.008]

NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M−1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS−001AC.
⑤ MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
⑥ DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

01-6010
01-3002 03 (MS-001AC)

14 Lead SOIC (narrow body)

8.74 [.344]
8.56 [.337]

−A−
⑥

⑥
−B−

3.99 [.157]
3.81 [.150]

14

1

6.20 [.2440]
5.80 [.2284]

⊕ 0.25 [.010] Ⓜ C BⓂ

−C−

0.25 [.0098]
0.10 [.0040]

1.27 [.050]
12X

0.46 [.018]
0.36 [.014] 14X

⊕ 0.25 [.010] Ⓜ C BⓈ AⓈ

0.48 [.019]
0.28 [.011] X 45°

0° − 8°

1.75 [.0688]
1.35 [.0532]

1.27 [.050]
0.41 [.016]

⑤ 14X

0.25 [.0098]
0.19 [.0075] 14X

NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M−1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS−012AB.
⑤ DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
⑥ DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].

01-6019
01-3063 00 (MS-012AB)

IRS2106/IRS21064(S)PbF

**Tape & Reel
8-lead SOIC**

LOADED TAPE FEED DIRECTION

NOTE : CONTROLLING
DIMENSION IN MM

CARRIER TAPE DIMENSION FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062
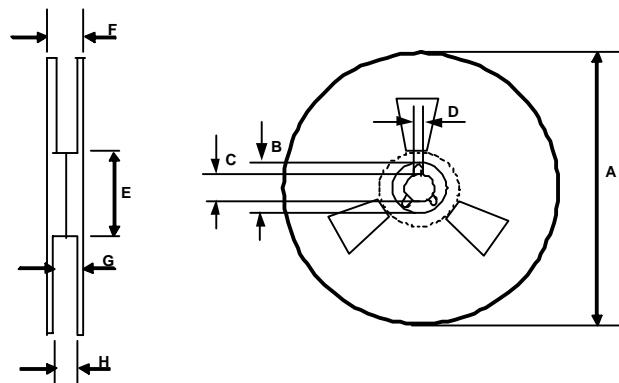
REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

International
IOR Rectifier

**Tape & Reel
14-lead SOIC**

LOADED TAPE FEED DIRECTION

NOTE : CONTROLLING
DIMENSION IN MM
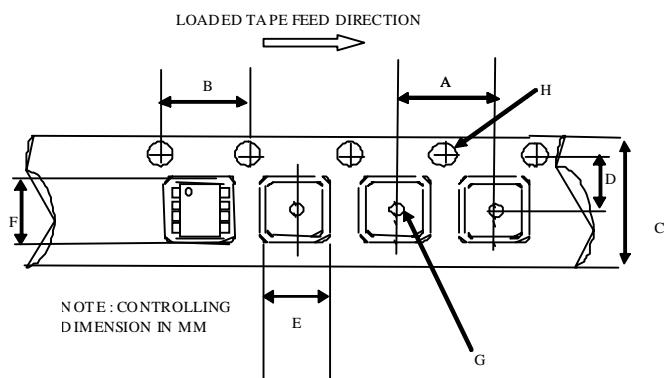
CARRIER TAPE DIMENSION FOR 14 SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	6.40	6.60	0.252	0.260
F	9.40	9.60	0.370	0.378
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062
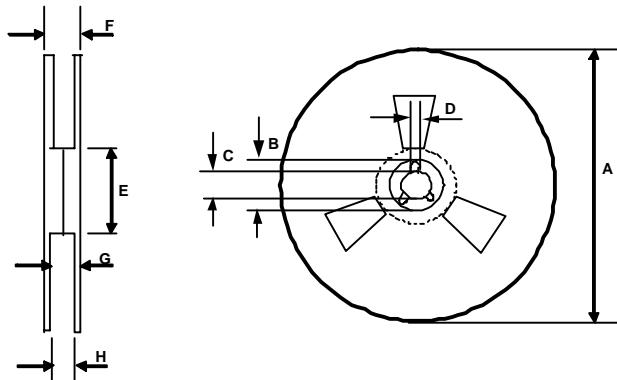
REEL DIMENSIONS FOR 14 SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

International
IGR Rectifier

LEADFREE PART MARKING INFORMATION

Part number —— IRSxxxxx

Date code —— YWW?

IR logo

Pin 1
Identifier

?XXXX

Lot Code
(Prod mode - 4 digit SPN code)

?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

Assembly site code
Per SCOP 200-002
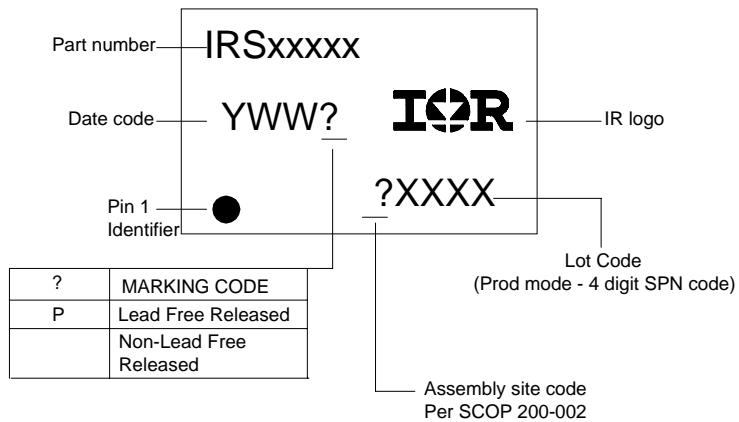
ORDER INFORMATION

8-Lead PDIP IRS2106PbF
8-Lead SOIC IRS2106SPbF
8-Lead SOIC Tape & Reel IRS2106STRPbF

14-Lead PDIP IRS21064PbF
14-Lead SOIC IRS21064SPbF
14-Lead SOIC Tape & Reel IRS21064STRPbF

International
IGR Rectifier

SOIC8 & 14 are MSL2 qualified.
This product has been designed and qualified for the industrial level.
Qualification standards can be found at www.irf.com
IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
Data and specifications subject to change without notice. 12/4/2006