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LEVETOP

LT768x

High Performance TFT-LCD Graphics Controller

Introduction

LT768x are an series high-performance TFT-LCD graphics accelerated display chip. Its main function is to assist MCU to display the contents of the TFT screen to the TFT Driver. It provides graphics acceleration, PIP (picture-in-picture), geometry graphics and other functions, in addition to enhance the display efficiency, Also greatly reduces the MCU processing graphics display time spent. LT768x also supports a very broad display resolution, can be from 320*240(QVGA) to 1280*1024(SXGA), the display is supported 16/18/24bits RGB interface.

LT768x supports a variety of MCU interface, including SPI, I2C serial port, or 8-bit, 16-bit parallel interface. In order to achieve multi-layers high-resolution display effect, LT768x embedded a 64MB or 128MB Display RAM. This Display Memory can support 16M color display from 2 gray to 1bit per pixel to up to 24bits per pixel. At the same time to reduce the animation display MCU in the software operation burden. LT768x built-in geometry drawing engine, supporting the painting point, drawing Line, drawing curve, ellipse, triangle, rectangle, rounded rectangle and other functions. The embedded hardware graphics Acceleration Engine (BTE) provides the command type of graphics operations, such as display rotation, mirror shot, The painting (PIP/Master-Sub Screen) and graphics mixed transparent display and other functions, enhance the display of the product performance, so can greatly reduce the MCU software operating burden. if use the high-speed SPI interface, then it can reduce the MCU I/O port needs, without to upgrade the MCU for TFT display. LT768x powerful display function is very suitable for the electronic products with TFT-LCD screen, such as home appliances, multi-functional business machines, industrial equipment, industrial control, electronic equipment, medical equipment, human-computer interface, testing equipment and other products.

Internal Block Diagram

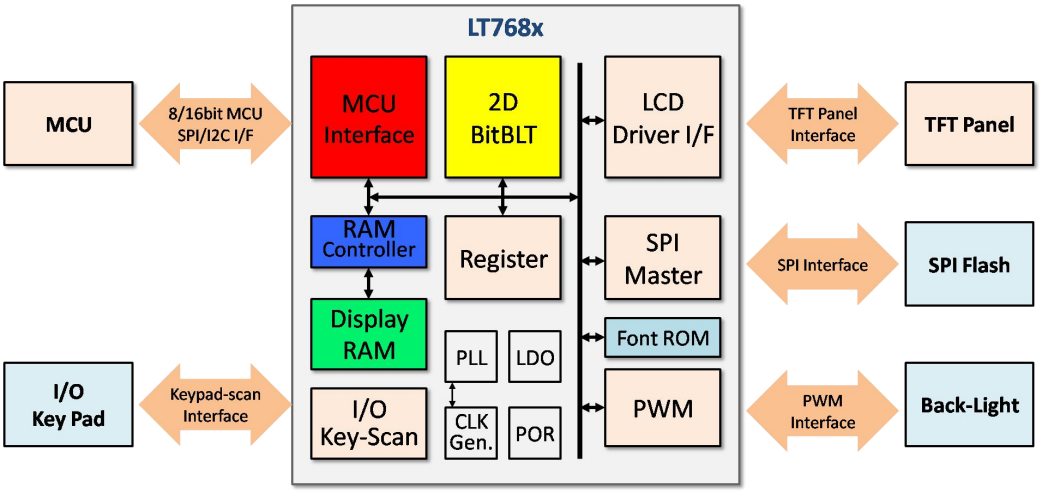

Figure A-1: Internal Block Diagram

System Block Diagram

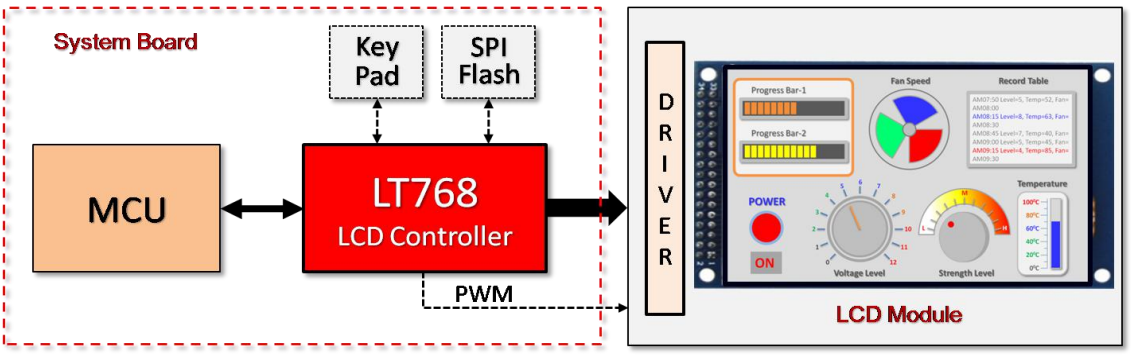

Figure A-2: LT768x Designed on System Board

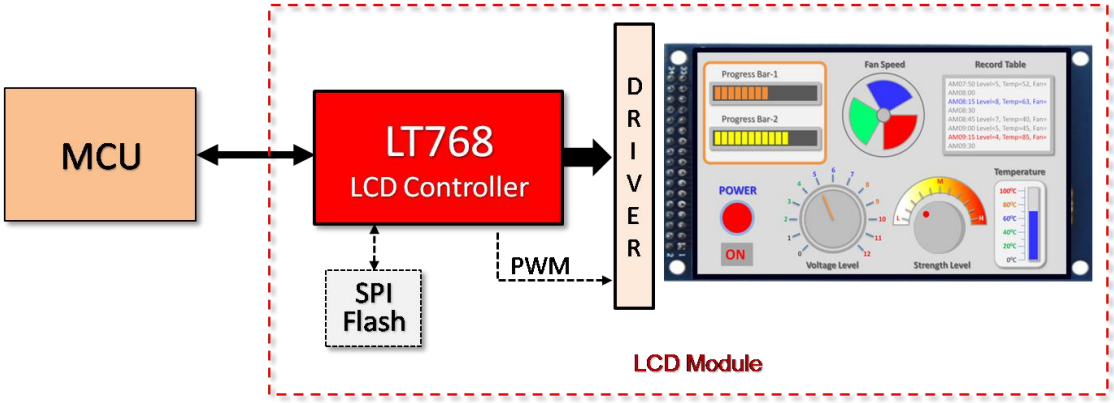

Figure A-3: LT768x Designed on TFT-LCD Module

Model Name

Table A-1: Model Selection

Model Name	Package	Embedded Display RAM	Resolution (Max.)	Colors
LT7681	LQFP-128	128Mb	640*480	16.7M
LT7683	LQFP-128	128Mb	800*600	16.7M
LT7686	LQFP-128	128Mb	1280*1024	16.7M
LT7680A	QFN-68 (8*8)	64Mb	800*600	262K
LT7680B	QFN-68 (8*8)	64Mb	480*320	262K

Features

Host Interface

- Support Three Types 8/16bits Asynchronous Bus Register Interface (or Memory Data)
  - Indirect Intel-80 Bus Interface
  - Indirect Motorola-6800 Bus Interface
- Provides Insert Wait State Mechanism on Parallel Host Cycle
- Support I²C Bus Interface
- Support Various SPI Protocol. Ex. 3 or 4-wire SPI

Display Data Formats

- 1bpp: Monochrome Data (1-bit/Pixel)
- 8bpp: RGB 3:3:2 (1-byte/Pixel)
- 16bpp: RGB 5:6:5 (2-byte/Pixel)
- 24bpp: RGB 8:8:8 (3-byte/Pixel or 4-byte/Pixel)
- Index 2:6 (64 Index Colors/Pixel with Opacity Attribute)
- αRGB 4:4:4:4 (4096 Colors/Pixel with Opacity Attribute)

Support Panel and Resolution

- Support 16/18/24-bits RGB Interface Type Panel
- Supported Resolution:
  - QVGA : 320*240, 16/18/24-bit LCD Panel
  - WQVGA: 480*272, 16/18/24-bit LCD Panel
  - VGA : 640*480, 16/18/24-bit LCD Panel
  - WVGA : 800*480, 16/18/24-bit LCD Panel
  - SVGA : 800*600, 16/18/24-bit LCD Panel
  - QHD : 960*540, 16/18/24-bit LCD Panel
  - WSVGA : 1024*600, 16/18/24-bit LCD Panel
  - XGA : 1024*768, 16/18/24-bit LCD Panel
  - SXGA : 1280*1024, 16/18/24-bit LCD Panel

Display Functions

- Multiple Display Buffer: Multi buffering allows the main display window to be switched among buffers. Multi buffering allows a simple animation display to be performed by switching the buffers
- Horizontal/Vertical Flip Display: Vertical Flip display functions are available for image data reads. PIP window will be disabled if flip display function enable
- Mirror and Rotation Functions are Available for Image Data Writes
- Provide four User-defined 32*32 Pixels Graphic Cursor
- Virtual Display: Virtual display is available to show an image which is larger than LCD panel size. The image may scroll easily in any direction
- Picture-in-Picture (PIP) Display: Supported two PIP windows area: Enabled PIP windows are always displayed on top of Main window. The PIP1 window is always on top of PIP2 window
- Wake-up Display: Wake-up Display is available to show the display data quickly which data is stored in Display RAM. This feature is used when returning from the Standby mode or Suspend mode
- Initial Display: Embedded a tiny processor with 12 instructions and use to show display data which stored in the serial flash and need not external MPU participate. It will auto execute after power-on, until program execute complete then handover control rights to external MCU
- Color Bar: It could display color bar on panel directly. Default resolution is 640 dots by 480 dots

Bit Block Transfer Engine (BTE)

- 2D BTE Engine
- Copy Image with Raster Operators
- Color Depth Conversion
- Solid Fill & Pattern Fill
- Provide User-defined Patterns with 8*8 Pixels or 16*16 Pixels
- Opacity (Alpha-Blend) Control: It blends two images and then generates a new image
  - Chroma-Keying Function: Mixes images with applying the specified RGB color according to transparency rate
  - Window Alpha-Blending Function: Mixes two images according to transparency rate in the specified region (fade-in and fade-out functions are available)
  - Dot Alpha-Blending Function: Mixes images according to transparency rate when the target is a graphics image in the RGB format

Display RAM (Frame Buffer)

- LT7680A/76860B: Embedded 64Mb Display RAM
- LT7681/7683/7686: Embedded 128Mb Display RAM

Shape Drawing Engine

- Provide Smart Drawing Features: Line, Rectangle, Triangle, Polygon, Poly-Line, Circle, Ellipse, Arc, Rounded-Rectangle and Circle-Rectangle

Text Features

- Embedded 8*16, 12*24, 16*32 Character Sets of ISO/IEC 8859-1/2/4/5
- User-defined Characters Support Half Size & Full Size for 8*16, 12*24 and 16*32
- Programmable Text Cursor for Writing with Character
- Character Enlargement Function *1, *2, *3, *4 for Horizontal/Vertical Direction
- Support Character Rotates 90 Degree

PWM Interface

- Embedded Two 16bits Timers
- One 8-bit Pre-Scalars & One 4bits Divider
- Programmable Duty Control of Output Waveform (PWM)
- Auto Reload Mode or One-Shot Pulse Mode
- Dead-Zone Generator

SPI Master Interface

- Provide DMA Function: Support Direct Data Transfer from External Serial Flash to Frame Buffer
- Compatible with Standard SPI Specifications
- Provides 16bytes Read FIFO and 16bytes Write FIFO
- Provide Interrupt when Tx FIFO was Empty and SPI Tx/Rx Engine Idle

I2C Interface

- Support Standard Mode (100kbps) and Fast Mode (400kbps)

Key-Matrix Interface

- Support up to 5*5 key matrix
- Programmable Scan Period
- Support Long Key & Repeat Key
- Support up to Two Keys Pressed Simultaneously
- Support Keypad-Scan Wakeup function

Power Saving

- Support Three Kind of Power Saving Mode: Standby, Suspend and Sleep Mode
- Support Wakeup Function by Host and External Event

Clock Source

- Embedded Programmable PLL for Core Clock, LCD Panel's Pixel Clock and Frame Buffer Clock

Reset

- Provide Power On Reset Automatically
- Accept External Hardware Reset to Synchronize with System
- Software Command Reset

Power Supply

- VDD: 3.3V +/- 0.3V
- Embedded 1.8V LDO

Package

- LQFP-128Pins, QFN-68Pins

Temperature

- -40℃~85℃

Pin Assignment

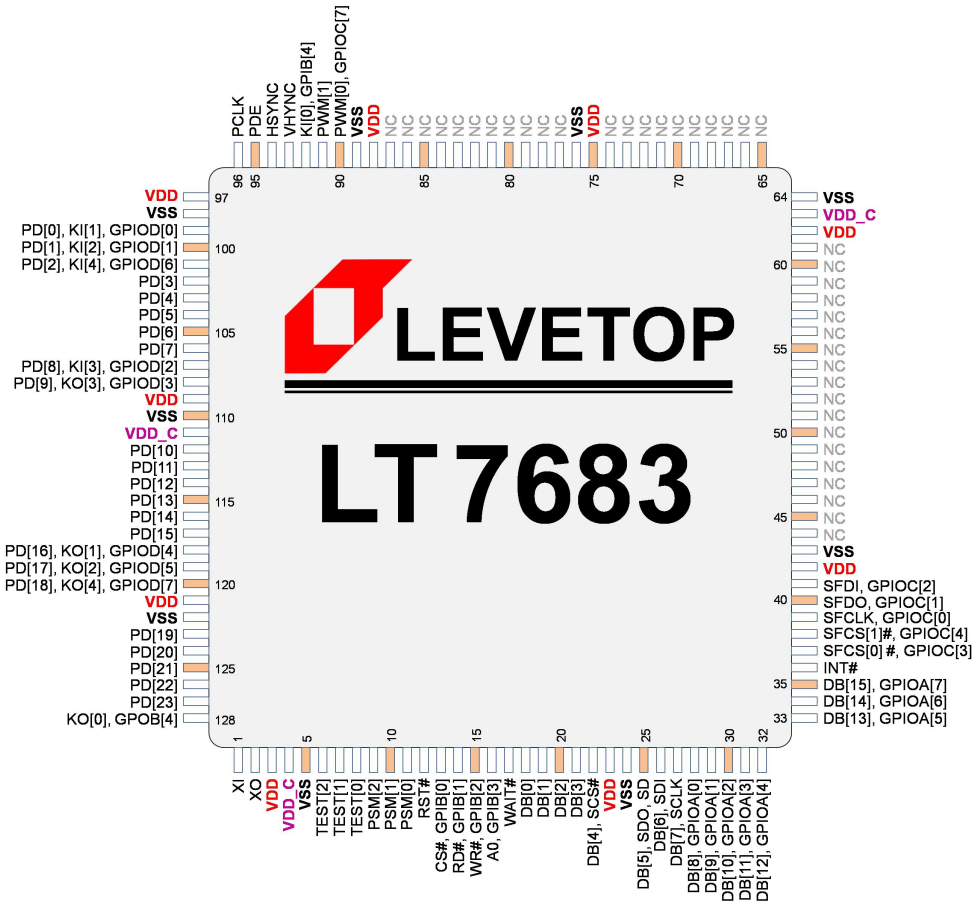

Figure A-4: LT7681/LT7683/LT7686 Pin Assignment (LQFP-128Pin)

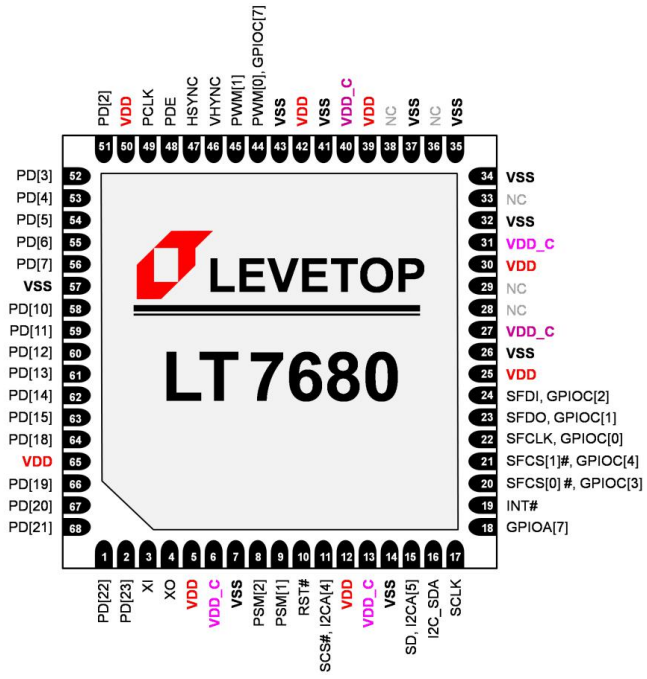

Figure A-5: LT7680 Pin Assignment (QFN-68Pin)

Pin Description -1 (LT7681/LT7683/LT7686/128Pin-LQFP)

LT7681/7683/7686 are 128Pin LQFP type package. The following tables are pin description of these chips.

Host Interface Select Signals (3 Pins)

Table A-2: Host I/F Select Signals

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>I/O</th><th>Pin Description</th></tr>
<tr><td>9~11</td><td>PSM[2:0]</td><td>I</td><td>Host Interface Selection
<table>
<tr><th>PSM[2:0]</th><th>Host I/F Mode</th></tr>
<tr><td>0 0 X</td><td>8bits or 16bits 8080 Parallel Interface Mode</td></tr>
<tr><td>0 1 X</td><td>8bits or 16bits 6800 Parallel Interface Mode</td></tr>
<tr><td>1 0 0</td><td>3-Wire SPI Mode</td></tr>
<tr><td>1 0 1</td><td>4-Wire SPI Mode</td></tr>
<tr><td>1 1 X</td><td>I2C Mode</td></tr>
</table>
If Host interface set as parallel mode, then PSM[0] pin is external interrupt input pin.</td></tr>
</table>

Host Parallel I/F Signals (22 Pins)

Table A-3: Host Parallel I/F Signals

Pin #	Pin Name	I/O	Pin Description
35~25, 22~18	DB[15:0]	IO	**Host Data Bus** These are data bus for data transfer between Host and LT768x. DB[15:8] will become GPIO (GPIOA[7:0]) when parallel Host 8080/6800 16-bits data bus mode doesn't set. DB[7:0] are multiplex pins that share with Serial Host control pins. When serial host mode set then DB[7:0] are defined as the control pins of serial host. Please refer to Host Interface section.
13	CS# GPIB[0]	I	**Chip Select Input** Low active chip select pin from Host. If host interface set as serial host mode, then this pin can be set as GPIB[0]. This pin with an internal pull-high resistor.
14	RD# EN GPIB[1]	I	**Read / Enable Input** **RD#**: When host interface is 8080 mode then this is a Read input signal, active low. **EN**: When interface is 6800 mode then this is a Enable input signal, active high. If host interface set as serial host mode then this pin can be set as GPIB[1]. This pin with an internal pull-high resistor.

Table A-3: Host MCU Parallel I/F Signals (Continued)

Pin #	Pin Name	I/O	Pin Description
15	WR# RW# GPIB[2]	I	**Write / Read-Write Input** **WR#**: When host interface is 8080 mode then this is a Write input signal, active low. **RW#**: When interface is 6800 mode then this is a Read-Write input signal. It active high in 'Host's read cycle, and active low in Host's write cycle. If host interface set as serial host mode then this pin will be set as GPIB[2]. This pin with an internal pull-high resistor.
16	A0 GPIB[3]	I	**Command / Data Select Input** The pin is used to select Command or Data cycle. A0 = 0, Status Read or Command Write cycle is selected. A0 = 1, Data Read or Data Write cycle is selected. If host interface set as serial host mode then this pin will be set as GPIB[3]. This pin with an internal pull-high resistor.
36	INT#	O	**Interrupt Output Signal** The interrupt output for host to indicate the status.
17	WAIT#	O	**Wait Output Signal** When high, it indicates that the LT768x is ready to transfer data. When low, then microprocessor is in wait state.

MCU Serial I/F Signals (8 Pins)

Table A-4: Host Serial I/F Signals

Pin #	Pin Name	I/O	Pin Description
27	SCLK (DB[7])	I	**SPI or I2C Clock** **SCLK**: Clock of 3-wire, 4-wire Serial or I2C interface. This is a multiplex pin that share with Parallel Host Data Bus DB[7].
26	SDI I2C_SDA (DB[6])	I	**I2C Data / 4-wire SPI Data Input** **SDI**: Data input pin of 4-wire SPI I/F. Connect to MCU's MOSI. **I2C_SDA**: Bi-direction data pin of I2C I/F. This pin is not used In 3-Wire serial I/F. Please connect it to GND. This is a multiplex pin that share with Parallel Host Data Bus DB[6].
25	SD SDO I2CA[5] (DB[5])	IO	**3-wire SPI Data / 4-wire SPI Data Output / I2C Slave Address Select** **SD**: Bi-direction data pin of 3-wire SPI I/F. **SDO**: Data output pin of 4-wire SPI I/F. Connect to MCU's MISO. **I2CA[5]**: I2C device address bit[5] of I2C I/F. This is a multiplex pin that share with Parallel Host Data Bus DB[5].

Table A-4: Host Serial I/F Signals (Continued)

Pin #	Pin Name	I/O	Pin Description
22	SCS# I2CA[4] (DB[4])	I	**SPI Chip Select / I2C Slave Address Select** **SCS#**: Chip select pin for 3-wire or 4-wire serial I/F. **I2CA[4]**: I2C device address bit[4]. This is a multiplex pin that share with Parallel Host Data Bus DB[4].
21~18	I2CA[3:0] (DB[3:0])	I	**I2C Slave Address Select** **I2CA[3:0]**: I2C device address bit [3:0]. These pins are not used In 3-Wire or 4-Wire I/F. Please connect them to GND. These are multiplex pins that share with Parallel Host Data Bus DB[3:0].

External Serial Flash / SPI Master Signals (5 Pins)

Table A-5: External Serial Flash Signals

Pin #	Pin Name	I/O	Pin Description
37	SFCS[0]# GPIOC[3]	IO	**Chip Select 0 for External Serial Flash or SPI device** SPI Chip select pin #0 for serial Flash or SPI device. If SPI master I/F is disabled then it can be programmed as GPIOC[3], and default is input function.
38	SFCS[1]# GPIOC[4]	IO	**Chip Select 1 for External Serial Flash or SPI device** SPI Chip select pin #1 for serial Flash or SPI device. If SPI master I/F is disabled then it can be programmed as GPIOC[4], and default is input function.
39	SFCLK GPIOC[0]	IO	**SPI Serial Clock** Serial clock output for serial Flash/ROM or SPI device. If SPI master I/F is disabled then it can be programmed as GPIO C[0], and default is input function.
40	SFDO GPIOC[1]	IO	**Master Output Slave Input** **Single Mode**: Data input of serial Flash or SPI device. For LT768, it is output. **Dual Mode**: The signal is used as bi-direction data #0(SIO0). Only valid in serial flash DMA mode. If SPI master I/F is disabled then it can be programmed as GPIO C[1], and default is input function.
41	SFDI GPIOC[2]	IO	**Master Input Slave Output** **Single Mode**: Data output of serial Flash or SPI device. For LT768, it is input. **Dual Mode**: The signal is used as bi-direction data #1(SIO1). Only valid in serial flash DMA mode. If SPI master I/F is disabled then it can be programmed as GPIOC[2], and default is input function.

LCD Driver Signals (28 Pins)

Table A-6: LCD Driver Signals

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>I/O</th><th>Pin Description</th></tr>
<tr><td>127~123,
120~112,
108~99</td><td>PD[23:0]</td><td>IO</td><td>
LCD Panel Data Bus
TFT LCD data bus output for source driver. LT76x supports 64K/256K/16.7M color depth by register setting; user can connect corresponding RGB bus for different setting.
<table>
<tr><th rowspan="2">Pin Name</th><th colspan="4">TFT-LCD Interface</th></tr>
<tr><th>11b (GPIO)</th><th>10b (16bits)</th><th>01b (18bits)</th><th>00b (24bits)</th></tr>
<tr><td>PD[0]</td><td colspan="3">GPIOD[0] / KI[1]</td><td>B0</td></tr>
<tr><td>PD[1]</td><td colspan="3">GPIOD[1] / KI[2]</td><td>B1</td></tr>
<tr><td>PD[2]</td><td colspan="2">GPIOD[6] / KI[4]</td><td>B0</td><td>B2</td></tr>
<tr><td>PD[3]</td><td>GPIOE[0]</td><td>B0</td><td>B1</td><td>B3</td></tr>
<tr><td>PD[4]</td><td>GPIOE[1]</td><td>B1</td><td>B2</td><td>B4</td></tr>
<tr><td>PD[5]</td><td>GPIOE[2]</td><td>B2</td><td>B3</td><td>B5</td></tr>
<tr><td>PD[6]</td><td>GPIOE[3]</td><td>B3</td><td>B4</td><td>B6</td></tr>
<tr><td>PD[7]</td><td>GPIOE[4]</td><td>B4</td><td>B5</td><td>B7</td></tr>
<tr><td>PD[8]</td><td colspan="3">GPIOD[2] / KI[3]</td><td>G0</td></tr>
<tr><td>PD[9]</td><td colspan="3">GPIOD[3] / KO[3]</td><td>G1</td></tr>
<tr><td>PD[10]</td><td>GPIOE[5]</td><td>G0</td><td>G0</td><td>G2</td></tr>
<tr><td>PD[11]</td><td>GPIOE[6]</td><td>G1</td><td>G1</td><td>G3</td></tr>
<tr><td>PD[12]</td><td>GPIOE[7]</td><td>G2</td><td>G2</td><td>G4</td></tr>
<tr><td>PD[13]</td><td>GPIOF[0]</td><td>G3</td><td>G3</td><td>G5</td></tr>
<tr><td>PD[14]</td><td>GPIOF[1]</td><td>G4</td><td>G4</td><td>G6</td></tr>
<tr><td>PD[15]</td><td>GPIOF[2]</td><td>G5</td><td>G5</td><td>G7</td></tr>
<tr><td>PD[16]</td><td colspan="3">GPIOD[4] / KO[1]</td><td>R0</td></tr>
<tr><td>PD[17]</td><td colspan="3">GPIOD[5] / KOI[2]</td><td>R1</td></tr>
<tr><td>PD[18]</td><td colspan="2">GPIOD[7] / KO[4]</td><td>R0</td><td>R2</td></tr>
<tr><td>PD[19]</td><td>GPIOF[3]</td><td>R0</td><td>R1</td><td>R3</td></tr>
<tr><td>PD[20]</td><td>GPIOF[4]</td><td>R1</td><td>R2</td><td>R4</td></tr>
<tr><td>PD[21]</td><td>GPIOF[5]</td><td>R2</td><td>R3</td><td>R5</td></tr>
<tr><td>PD[22]</td><td>GPIOF[6]</td><td>R3</td><td>R4</td><td>R6</td></tr>
<tr><td>PD[23]</td><td>GPIOF[7]</td><td>R4</td><td>R5</td><td>R7</td></tr>
</table>
These are multiplex pins that share with GPIO and Key-Matrix pins. The Default setting of LCD I/F is 18bpp function mode, so PD[17:16 / 8:9 /1:0] are defined as GPIO pins.
</td></tr>
</table>

Table A-6: LCD Driver Signals (Continued)

Pin #	Pin Name	I/O	Pin Description
96	PCLK	O	**Panel Scan Clock** Generic TFT interface signal for panel scan clock. It derives from internal PLL.
93	VSYNC	O	**VSYNC Pulse** Generic TFT interface signal for vertical synchronous pulse.
94	HSYNC	O	**HSYNC Pulse** Generic TFT interface signal for horizontal synchronous pulse.
95	PDE	O	**Data Enable** Generic TFT interface signal for data valid or data enable.

PWM Output Signals (2 Pins)

Table A-7: PWM Output Signals

Pin #	Pin Name	I/O	Pin Description
90	PWM[0] INITDIS GPIOC[7] CCLK	IO	**PWM Output 0 / Initial Display Enable** **PWM[0]**: PWM's output signal. The output mode is decided by configuration register. This pin can be used as the control signal of TFT panel's back light. **INITDIS**: Pull-high this pin will enable Initial Display function. This pin has internal pull-down in reset period to disable Initial Display function by default. i.e. after reset complete, internal pull-down resistor will be disabled. If PWM function disabled then it can be programmed as GPIO C[7], and default is GPIOC[7] input function, or output Core Clock - CCLK.
91	PWM[1]	IO	**PWM Output 1** PWM's output signal. The output mode and output function is decided by configuration register. This pin also can be used as the control signal of TFT panel's back light. When TEST[0] set high, then PWM[1] pin is external panel scan clock input

GPIO Signals (28 Pins)

Table A-8: General Purpose I/O Signals

Pin #	Pin Name	I/O	Pin Description
35~28	GPIOA[7:0]	IO	**GPIO A Group** These are general purpose I/O. These are multiplex pins that share with DB[15:8]. They are available when 8bits parallel host mode and serial Host mode.
92, 128, 16~13	GPIB[4], GPOB[4], GPIB[3:0]	IO	**GPIO B Group** These are general purpose I/O. GPIB[3:0] are read only and available in serial host mode. GPIB[4] is same pin with KI[0]. GPOB[4] is same pin with KO[0]. GPIB[3:0] are multiplex pins that share with {A0, WR#, RD#, CS#}.
90, 38, 37, 41~39	GPIOC[7], GPIOC[4:0]	IO	**GPIO C Group** These are general purpose I/O. GPIOC are available when PWM and SPI Master functions disabled. GPIOC[7] is same pin with PWM[0]. GPIOC[4:0] are multiplex pins that share with {SFCS1#, SFCS0#, SFDI, SFDO, SFCLK}
120, 101 119, 118 108, 107 100, 99	GPIOD[7:0]	IO	**GPIO D Group** These are general purpose I/O. GPIOD[7:0] are multiplex pins that share with PD[18, 2, 17, 16, 9, 8, 1, 0]. GPIOD[5,4,3,2,1,0] are available when LCD Panel interface is set 16bits or 18bits. GPIOD[7,6] are available when LCD Panel interface is set 16bits.

Key-Matrix Signals (10 Pins)

Table A-9: Key-Matrix Signals

Pin #	Pin Name	I/O	Pin Description
101, 107, 100, 99, 92	KI[4:0]	I	**Key-Matrix Data Pins** Keypad data inputs with internal pull-up resister. KI[4:1] are multiplex pins that share with PD[8] and PD[2:0]. The Key-matrix function will be disable when LCD I/F are set as 24bits. XKIN[0] also provide the I2CMCK function of I2C Master.
120,108, 119,118, 128	KO[4:0]	O	**Key-Matrix Strobe Pins** Keypad strobe data outputs with Open-Drain. KO[4:1] are multiplex pins that share with PD[9] and PD[18:16]. KO[0] also provide the I2CMDA function of I2C Master.

Power and Clock Signals (23 Pins)

Table A-10: Power and Clock Signals

Pin #	Pin Name	I/O	Pin Description
1	XI	I	**Crystal / External Clock Input** This input pin is used for internal crystal circuit or external clock that generate clock source for PLL. It should be connected to external crystal and suggested frequency is 10.0MHz.
2	XO	O	**Crystal Output** This is an output pin for internal crystal circuit. It should be connected to external crystal circuit.
4, 63, 111	VDD_C	PWR	**Internal LDO Output** These pins must connect 1uF and 0.1uF capacitor to ground.
3, 23, 42, 62, 75, 88, 97, 109, 121	VDD	PWR	**3.3V Power Pins**
5, 24, 43, 64, 76, 89 98, 110, 122	VSS	PWR	**Ground(GND) Pins**

Reset and Test Signals (4 Pins)

Table A-11: Reset and Test Signals

Pin #	Pin Name	I/O	Pin Description
12	RST#	I/O	**Reset Signal Input** This is a active low Reset pin for LT768x. To avoid noise interfere and cause fake reset behavior, this pin is active at least 256 OSC clocks.
6~8	TEST[2:0]	I	**Test Input** These pins are used for testing and normally connect to GND. If TEST[0] keep high, the internal PLL will be disable and the system clock is supply by external. If TEST[2:1] keep 01b, then the SPI Master signals will keep floating. This feature allow external device to program Serial Flash directly. (i.e. ISP, In-System-Programming)

Pin Description -2 (LT7680/68Pin-QFN)

LT7680 is a 68Pin QFN type package chip. The following tables are their pins function list. For detail pins description, please refer to the previous section - Pin Description -1.

Host Interface Select Signals (2 Pins)

Table A-12: Host I/F Select Signals

Pin #	Pin Name	I/O	Pin Description
8~9	PSM[2:1]	I	**Host Interface Selection** LT7680 only supports 3-Wires SPI and I2C mode. Its PSM[0] pin already connected to GND within the IC, while PSM[2] must pull-up to VDD. When PSM[1] = 0, select serial 3-line SPI mode. When PSM[1] = 1, select serial I2C mode.

Host Serial I/F Signals (5 Pins)

Table A-13: Host Serial I/F Signals

Pin #	Pin Name	I/O	Pin Description
17	SCLK	I	**SPI or I2C Clock**
16	I2C_SDA	I	**I2C Data / 4-wire SPI Data Input**
15	SD I2CA[5]	IO	**3-wire SPI Data / 4-wire SPI Data Output / I2C Slave Address Select**
11	SCS# I2CA[4]	I	**SPI Chip Select / I2C Slave Address Select**
19	INT#	O	**Interrupt Output Signal**

LCD Driver Signals (22 Pins)

Table A-14: LCD Driver Signals

Pin #	Pin Name	I/O	Pin Description
2~1, 68~66, 64, 63~58, 56~51	PD[23:18], PD[15:10], PD[7:2],	IO	**LCD Panel Data Bus**
49	PCLK	O	**Panel Scan Clock**
46	VSYNC	O	**VSYNC Pulse**
47	HSYNC	O	**HSYNC Pulse**
48	PDE	O	**Data Enable**

External Serial Flash / SPI Master Signals (5 Pins)

Table A-15: External Serial Flash Signals

Pin #	Pin Name	I/O	Pin Description
21~20	SFCS[1:0]#	IO	**Chip Select 0 for External Serial Flash or SPI device**
22	SFCLK	IO	**SPI Serial Clock**
23	SFDO	IO	**Master Output Slave Input**
24	SFDI	IO	**Master Input Slave Output**

PWM Output Signals (2 Pins)

Table A-16: PWM Output Signals

Pin #	Pin Name	I/O	Pin Description
45	PWM[0]	IO	**PWM Output 0 / Initial Display Enable**
44	PWM[1]	IO	**PWM Output 1**

GPIO Signals (7 Pins)

Table A-17: General Purpose I/O Signals

Pin #	Pin Name	I/O	Pin Description
18	GPIOA[7]	IO	**GPIO A Group**
44, 21, 20, 24, 23, 22	GPIOC[7] GPIOC[4:0]	IO	**GPIO C Group**

Reset (1 Pins)

Table A-18: Reset Signal

Pin #	Pin Name	I/O	Pin Description
10	RST#	I/O	**Reset Signal Input**

Power and Clock Signals (26 Pins)

Table A-19: Power and Clock Signals

Pin #	Pin Name	I/O	Pin Description
2	XI	I	**Crystal / External Clock Input**
3	XO	O	**Crystal Output**
36, 13, 27, 31, 40	VDD_C	PWR	**Internal LDO Output**
5, 12, 25, 30, 39, 42, 50, 65	VDD	PWR	**3.3V Power Pins**
7, 14, 26, 32, 34, 35, 37, 41, 43, 57,	VSS	PWR	**Ground(GND) Pins**
	Thermal Pad	-	The back of LT7680 Heat sink pad must tied to ground.

The LT768x series support different Host interfaces. For example, the LT7680 is a 68pin QFN chip , which only supports serial SPI and I2C mode. The following table is Host interface supporting list for LT768x series:

Table A-20: Host Interface Supporting List of LT768x Series

No.	Host Interface Mode	LT7681 LT7683 LT7686	LT7680A LT7680B
1	8bits 8080 Parallel Interface Mode	v	
2	16bits 8080 Parallel Interface Mode	v	
3	8bits 6800 Parallel Interface Mode	v	
4	16bits 6800 Parallel Interface Mode	v	
5	3-Wire SPI Mode	v	v
6	4-Wire SPI Mode	v	
7	I2C Mode	v	v

Package Information

■ LT7681/LT7683/LT7686 (LQFP-128pin)

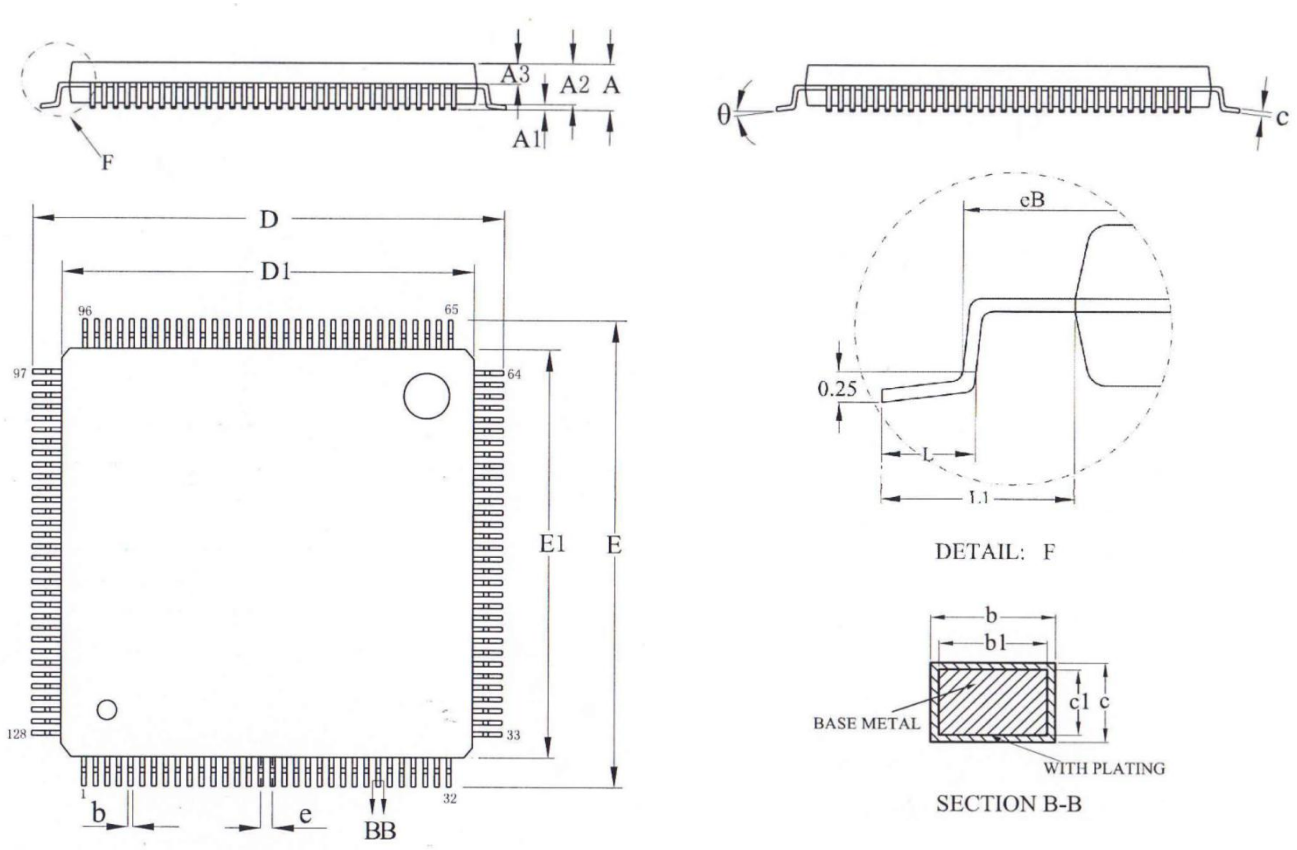

Figure B-1: 128Pin LQFP Outline

Table B-1: 128Pin LQFP Dimension

Symbol	Millimeter			Symbol	Millimeter		
	Min.	Nom.	Max		Min.	Nom.	Max
A	-	-	1.60	D1	13.9	14.0	14.1
A1	0.05	-	0.15	E	15.8	16.0	16.2
A2	1.35	1.40	1.45	E1	13.9	14.0	14.1
A3	0.59	0.64	0.69	eB	15.05	-	15.35
b	0.14	-	0.22	e	0.40BSC		
b1	0.13	0.16	0.19	L	0.45	-	0.75
c	0.13	-	0.17	L1	1.00REF		
c1	0.12	0.13	0.14	θ	0		7
D	15.8	16.00	16.2				

■ LT7680 (QFN-68pin)

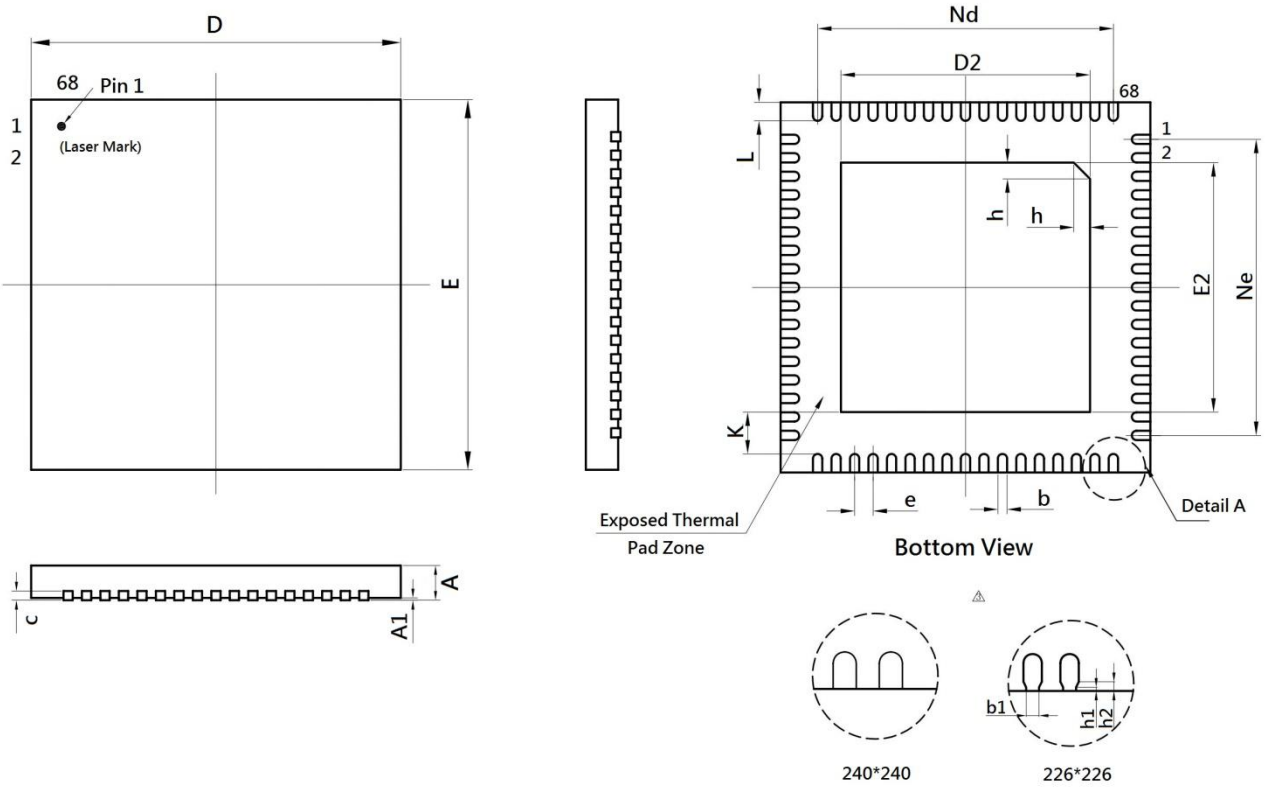

Figure B-2: 68Pin QFN Outline

Note: When PCB layout, the heat pad of LT7680's back (thermal Pad Zone) must be directly grounded.

Table B-2: 68Pin QFN Dimenstion

Symbol	Millimeter			Symbol	Millimeter		
	Min.	Nom.	Max		Min.	Nom.	Max
A	0.70	0.75	0.8	E	7.9	8.0	8.10
A1	-	0.02	0.05	Ne	6.40BSC		
b	0.15	0.20	0.25	L	0.35	0.40	0.45
b1	0.14REF			K	0.20	-	-
c	0.18	0.20	0.25	h	0.30	0.35	0.40
D	7.90	8.00	8.10	h1	0.04REF		
e	0.40BSC			h2	0.10REF		
Nd	6.40BSC						

Table B-3: Lead Frame Dimension

L/F 载体尺寸	Symbol	Millimeter	L/F Dimension	Symbol	Millimeter
240*240	D2	5.49+/- 0.10	226*226	D2	5.39+/- 0.10
	E2	5.49+/- 0.10		E2	5.39+/- 0.10