



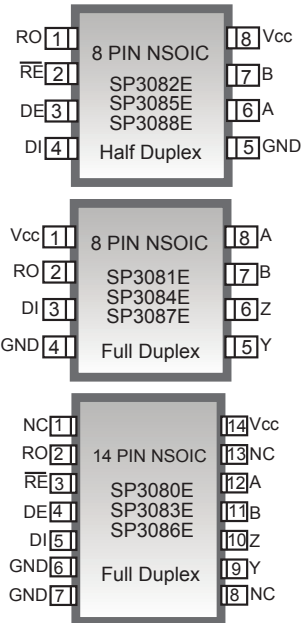
## Advanced-Failsafe RS-485/RS-422 Transceivers 1/8th Unit Load, Slew-Rate Limited, ±15kV ESD-Protected

### FEATURES

- 5.0V single supply operation
- Receiver failsafe on open, shorted or terminated lines
- 1/8th Unit Load, 256 transceivers on bus
- Robust ESD protection for RS-485 pins
  - ±15kV Air-Gap Discharge
  - ±15kV Human Body Model
  - ±8kV Contact Discharge
- Controlled driver slew rates
  - 115kbps, Low EMI (SP3080E, SP3081E, SP3082E)
  - 500kbps, Low EMI (SP3083E, SP3084E, SP3085E)
  - High Speed, 20Mbps (SP3086E, SP3087E, SP3088E)
- Hot Swap glitch protection on control inputs
- Driver short circuit current limit and thermal shutdown for overload protection
- Ultra-low 400µA quiescent current
- 1µA shutdown mode (except SP3081E, SP3084E, SP3087E)
- Industry standard package footprints

### APPLICATIONS

- Motor Control
- Building Automation
- Security Systems
- Remote Meter Reading
- Long or un-terminated transmission lines



### DESCRIPTION

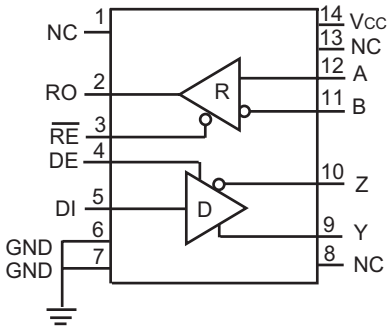
The SP3080E-SP3088E family of RS-485 devices are designed for reliable, bidirectional communication on multipoint bus transmission lines. Each device contains one differential driver and one differential receiver. The SP3082E, SP3085E and SP3088E are half-duplex devices; other part numbers are full-duplex. All devices comply with TIA/EIA-485 and TIA/EIA-422 standards. Lead-free and RoHS compliant packages are available for all models.

These devices are ruggedized for use in harsh operating conditions over the entire common-mode voltage range from -7V to +12V. Receivers are specially designed to fail-safe to a logic high output state if the inputs are left un-driven or shorted. All RS-485 bus-pins are protected against severe ESD events up to ±15kV (Air-Gap and Human Body Model) and up to ±8kV Contact Discharge (IEC 61000-4-2). Drivers are protected from excess current flow caused by bus contention or output short-circuits by both an internal current limit and a thermal-overload shutdown. Devices are rated for industrial (-40 to +85°C) operating temperatures. Receivers have exceptionally high input impedance, which places only 1/8th the standard load on a shared bus. Up to 256 transceivers may coexist while preserving full signal margin.

All devices operate from a single 5.0V power supply and draw negligible quiescent power. All versions except the SP3081E, SP3084E, and SP3087E may independently enable and disable their driver and receiver and enter a low power shutdown mode if both driver and receiver are disabled. All outputs maintain high impedance in shutdown or when powered-off.

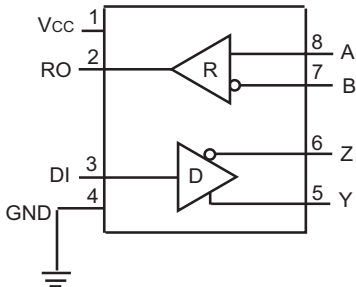
## DEVICE ARCHITECTURE AND BLOCK DIAGRAMS

Devices are available in three industry standard architectures and footprints. In each footprint there are three speed grades available.



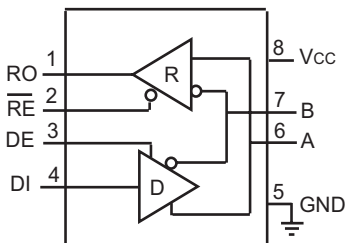
### 14-Pin Full Duplex

SP3080E, 115kbps slew rate limited  
 SP3083E, 500kbps slew rate limited  
 SP3086E, 20Mbps



### 8-Pin Full Duplex

SP3081E, 115kbps slew rate limited  
 SP3084E, 500kbps slew rate limited  
 SP3087E, 20Mbps



### 8-Pin Half Duplex

SP3082E, 115kbps slew rate limited  
 SP3085E, 500kbps slew rate limited  
 SP3088E, 20Mbps

**PIN ASSIGNMENTS**

Pin Number			Pin Name	Pin Function
Full-Duplex		Half - Duplex		
SP3080E	SP3081E	SP3082E		
SP3083E	SP3084E	SP3085E		
SP3086E	SP3087E	SP3088E		
2	2	1	RO	Receiver Output. When $\overline{RE}$ is low and if $(A - B) \geq -40\text{mV}$ , RO is high. If $(A - B) \leq -200\text{mV}$ , RO is low.
3	-	2	$\overline{RE}$	Receiver Output Enable. When $\overline{RE}$ is low, RO is enabled. When $\overline{RE}$ is high, RO is high impedance. Drive $\overline{RE}$ high and DE low to enter shutdown mode. $\overline{RE}$ is a hot-swap input.
4	-	3	DE	Driver Output Enable. When DE is high, outputs are enabled. When DE is low, outputs are high impedance. Drive DE low and $\overline{RE}$ high to enter shutdown mode. DE is a hot-swap input.
5	3	4	DI	Driver Input. With DE high, a low level on DI forces non-inverting output low and inverting output high. A high level on DI forces non-inverting output high and inverting output low.
6, 7	4	5	GND	Ground
9	5	-	Y	Non-inverting Driver Output
10	6	-	Z	Inverting Driver Output
11	7	-	B	Inverting Receiver Input
-	-	7	B	Inverting Receiver Input and Inverting Driver Output
12	8	-	A	Non-inverting Receiver Input
-	-	6	A	Non-inverting Receiver Input and Non-inverting Driver Output
14	1	8	V <sub>CC</sub>	Positive Supply V <sub>CC</sub> . Bypass to GND with a 0.1uF capacitor.
1, 8, 13	-	-	NC	No Connect, not internally connected

Note: On 14-pin packages connect both pins 6 and 7 to Ground.

## ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Supply Voltage ( $V_{CC}$ ).....+ 7.0V  
 Input voltage at control input pins ( $\overline{RE}$ , DE)... -0.3V to  $V_{CC}+0.3V$   
 Driver input voltage (DI) .....-0.3V to  $V_{CC}+0.3V$   
 Driver output voltage (A, B, Y, and Z) .....+/-13V  
 Receiver output voltage (RO) .....-0.3V to ( $V_{CC} + 0.3V$ )  
 Receiver input voltage (A, B) .....+/-13V  
 Voltage input range, transient pulse, A, B, Y and Z through 100 $\Omega$ , see Figure 11 .....+/-65.0V  
 Package Power Dissipation:  
     Maximum Junction Temperature 150°C  
     8-Pin SO  $\Theta_{JA} = 128.4^{\circ}C/W$   
     14-Pin SO  $\Theta_{JA} = 86^{\circ}C/W$   
 Storage Temperature.....-65°C to +150°C  
 Lead Temperature (soldering, 10s)..... +300°C

## RECOMMENDED OPERATING CONDITIONS

$V_{CC}=5V \pm 10\%$ ,  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted, Typical values are  $V_{CC}=5V$  and  $T_A=25^{\circ}C$

Recommended Operating Conditions		Min.	Nom.	Max.	Unit
Supply Voltage, $V_{CC}$		4.5	5	5.5	v
Input Voltage on A and B pins		-7		12	v
High-level input voltage (DI, DE or $\overline{RE}$ ), $V_{IH}$		2		$V_{CC}$	v
Low-level input voltage (DI, DE or $\overline{RE}$ ), $V_{IL}$		0		0.8	v
Output Current	Driver	-60		60	mA
	Receiver	-8		8	
Signaling Rate, 1/ $t_{UI}$	SP3080E, SP3081E, SP3082E			0.115	Mbps
	SP3083E, SP3084E, SP3085E			0.5	
	SP3086E, SP3087E, SP3088E			20	
Operating Free Air Temperature, $T_A$	Industrial Grade (E)	-40		85	$^{\circ}C$

Note: The least positive (most negative) limit is designated as the maximum value.

## ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>Digital Input Signals: DI, DE, RE</b>							
Logic input thresholds	High, $V_{IH}$		2.0			V	
	Low, $V_{IL}$				0.8		
Logic Input Current	$T_A = 25^\circ\text{C}$ , after first transition				$\pm 1$	$\mu\text{A}$	
Input Hysteresis	$T_A = 25^\circ\text{C}$			100		mV	
<b>Driver</b>							
Differential Driver Output ( $V_{OD}$ )	No Load				$V_{CC}$	V	
Differential Driver Output, Test 1	$R_L=100\Omega$ (RS-422)		2		$V_{CC}$	V	
	$R_L=54\Omega$ (RS-485)		1.5	2.7	$V_{CC}$		
Differential Driver Output, Test 2	$V_{CM} = -7$ to $+12\text{V}$		1.5		$V_{CC}$		
Change in Magnitude of Differential Output Voltage ( $\Delta V_{OD}$ ) (Note 1)	$R_L=54$ or $100\Omega$				$\pm 0.2$	V	
Driver Common Mode Output Voltage ( $V_{CC}$ )	$R_L=54$ or $100\Omega$		1		3	V	
Change in Common Mode Output Voltage ( $\Delta V_{OC}$ )	$R_L=54$ or $100\Omega$				$\pm 0.2$	V	
Driver Short Circuit Current Limit	$-7\text{V} \leq V_{OUT} \leq +12\text{V}$ (Note 5)				$\pm 250$	mA	
Output Leakage Current (Full-duplex versions, Y & Z pins) Note 2	DE=0, RE=0, $V_{CC}=0$ or 5.5V	$V_{OUT}=12\text{V}$			125	$\mu\text{A}$	
		$V_{OUT}=-7\text{V}$	-100				
<b>Receiver</b>							
Receiver Input Resistance	$-7\text{V} \leq V_{CM} \leq 12\text{V}$		96			K $\Omega$	
Input Current (A, B pins)	DE=0, RE=0, $V_{CC}=0$ or 5.5V	$V_{IN}=12\text{V}$			125	$\mu\text{A}$	
		$V_{IN}=-7\text{V}$	-100				
Receiver Differential Threshold ( $V_A-V_B$ )	$-7\text{V} \leq V_{CM} \leq 12\text{V}$		-200	-125	-40	mV	
Receiver Input Hysteresis				25		mV	
Receiver Output Voltage	$V_{OH}$	$I_{OUT} = -8\text{mA}$ , $V_{ID} = -40\text{mV}$	$V_{CC}-1.5$			V	
	$V_{OL}$	$I_{OUT} = 8\text{mA}$ , $V_{ID} = -200\text{mV}$			0.4		
High-Z Receiver Output Current	$V_{CC} = 5.5\text{V}$ , $0 \leq V_{OUT} \leq V_{CC}$				$\pm 1$	$\mu\text{A}$	
Receiver Output Short Circuit Current	$0\text{V} \leq V_{RO} \leq V_{CC}$				$\pm 95$	mA	
<b>Supply and Protection</b>							
Supply Current	IQ, Active Mode		No load, DI=0 or $V_{CC}$		400	900	$\mu\text{A}$
	Shutdown Mode		DE=0, RE= $V_{CC}$ , DI= $V_{CC}$			1	$\mu\text{A}$
Thermal Shutdown Temperature	Junction temperature			165		$^\circ\text{C}$	
Thermal Shutdown Hysteresis				15			

**Notes:**

- Change in Magnitude of Differential Output Voltage and Change in Magnitude of Common Mode Output Voltage are the changes in output voltage when DI input changes state.
- Except devices which don't have DE or RE inputs.
- The transceivers are put into shutdown by bringing RE high and DE low. If the inputs are in this state for less than 50ns the device does not enter shutdown. If the enable inputs are held in this state for at least 600ns the device is assured to be in shutdown. In this low power mode most circuitry is disabled and supply current is typically 1nA.
- Characterized, not 100% tested.
- See Driver Short Circuit Limit Test Circuit.

## TIMING CHARACTERISTICS

Unless otherwise noted V<sub>cc</sub>= +5.0±0.5V, ambient temperature T<sub>A</sub> from -40 to +85°C

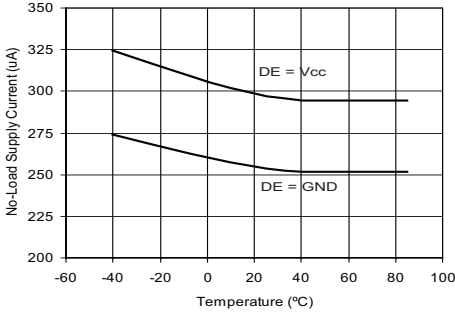
SP3080E, SP3081E, SP3082E DRIVER CHARACTERISTICS:	Conditions	Min.	Typ.	Max.	Unit
Data Signaling Rate (1 / t <sub>UI</sub> )	Duty Cycle 40 to 60%	115			Kbps
Driver Propagation Delay (t <sub>PHL</sub> , t <sub>PLH</sub> )	R <sub>L</sub> = 54Ω, C <sub>L</sub> = 50pF,	500		2600	ns
Driver Output Rise/Fall Time (t <sub>R</sub> , t <sub>F</sub> )		667	1200	2500	ns
Driver Differential Skew (t <sub>PLH</sub> - t <sub>PHL</sub> )				±200	ns
Driver Enable to Output High (t <sub>DZH</sub> )		SP3080E, SP3081E			3500
Driver Enable to Output Low (t <sub>DZL</sub> )				3500	ns
Driver Disable from Output High (t <sub>DHZ</sub> )				100	ns
Driver Disable from Output Low (t <sub>D LZ</sub> )				100	ns
Shutdown to Driver Output Valid (t <sub>DZV</sub> )				6000	ns

SP3083E, SP3084E, SP3085E DRIVER CHARACTERISTICS:	Conditions	Min.	Typ.	Max.	Unit
Data Signaling Rate (1 / t <sub>UI</sub> )	Duty Cycle 40 to 60%	500			Kbps
Driver Propagation Delay (t <sub>PHL</sub> , t <sub>PLH</sub> )	R <sub>L</sub> = 54Ω, C <sub>L</sub> = 50pF,	250		1000	ns
Driver Output Rise/Fall Time (t <sub>R</sub> , t <sub>F</sub> )		200	530	750	ns
Driver Differential Skew (t <sub>PLH</sub> - t <sub>PHL</sub> )				±100	ns
Driver Enable to Output High (t <sub>DZH</sub> )	SP3083E, SP3084E			2500	ns
Driver Enable to Output Low (t <sub>DZL</sub> )				2500	ns
Driver Disable from Output High (t <sub>DHZ</sub> )				100	ns
Driver Disable from Output Low (t <sub>D LZ</sub> )				100	ns
Shutdown to Driver Output Valid (t <sub>DZV</sub> )				4500	ns

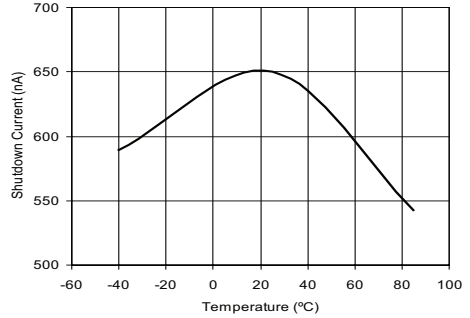
SP3086E, SP3087E, SP3088E DRIVER CHARACTERISTICS:	Conditions	Min.	Typ.	Max.	Unit
Data Signaling Rate (1 / t <sub>UI</sub> )	Duty Cycle 40 to 60%	20			Mbps
Driver Propagation Delay (t <sub>PHL</sub> , t <sub>PLH</sub> )	R <sub>L</sub> = 54Ω, C <sub>L</sub> = 50pF,		12	20	ns
Driver Output Rise/Fall Time (t <sub>R</sub> , t <sub>F</sub> )			6	10	ns
Driver Differential Skew (t <sub>PLH</sub> - t <sub>PHL</sub> )				±5	ns
Driver Enable to Output High (t <sub>DZH</sub> )	SP3086E, SP3087E			150	ns
Driver Enable to Output Low (t <sub>DZL</sub> )				150	ns
Driver Disable from Output High (t <sub>DHZ</sub> )				50	ns
Driver Disable from Output Low (t <sub>D LZ</sub> )				50	ns
Shutdown to Driver Output Valid (t <sub>DZV</sub> )				250	ns

Receiver CHARACTERISTICS:	Conditions	Min.	Typ.	Max.	Unit
Receiver Prop. Delay SP3080E - SP3085E	C <sub>L</sub> = 15pF, V <sub>IO</sub> = ±2V,		75	200	ns
Receiver Prop. Delay SP3086E - SP3088E				75	ns
Prop. Delay Skew SP3080E-SP3085E				±30	ns
Prop. Delay Skew SP3086E-SP3088E				±5	ns
Receiver Output Rise/Fall Time	C <sub>L</sub> = 15pf			15	ns
Receiver Enable to Output High (t <sub>ZH</sub> )				50	ns
Receiver Enable to Output Low (t <sub>ZL</sub> )				50	ns
Receiver Disable from High (t <sub>HZ</sub> )				50	ns
Receiver Disable from Low (t <sub>LZ</sub> )				50	ns
Shutdown to Receiver Output Valid (t <sub>ROV</sub> )				3500	ns
Time to Shutdown (Note 2,3,4)		50	200	600	ns

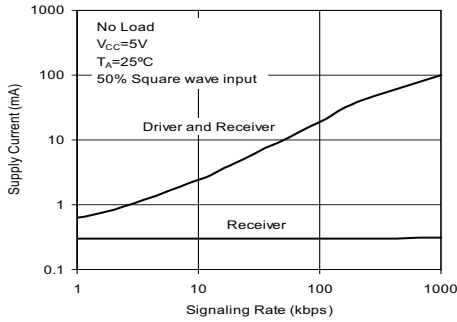
# TYPICAL PERFORMANCE CHARACTERISTICS



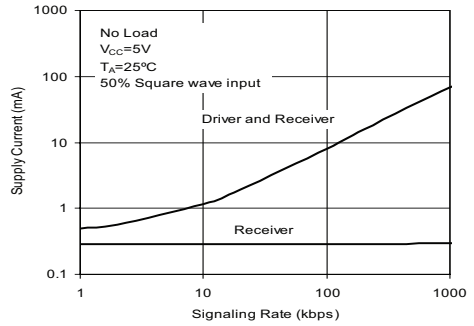
No-Load Supply Current vs Temperature



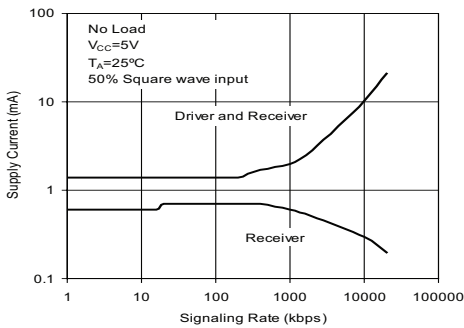
Shutdown Current vs Temperature



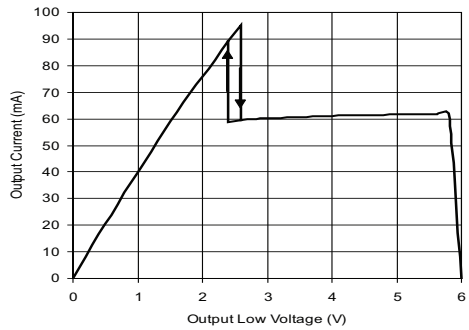
Supply Current vs Signaling Rate (SP3080E-SP3082E)



Supply Current vs Signaling Rate (SP3083E-SP3085E)

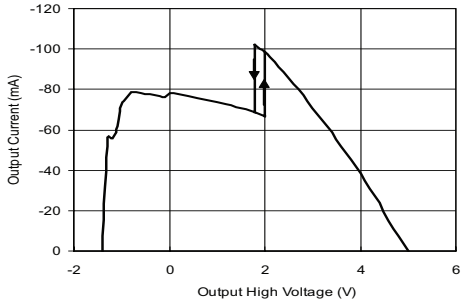


Supply Current vs Signaling Rate (SP3086E-SP3088E)

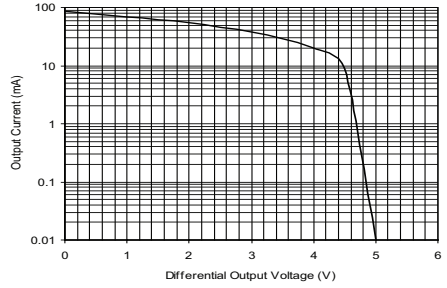


Output Current vs Driver Output Low Voltage

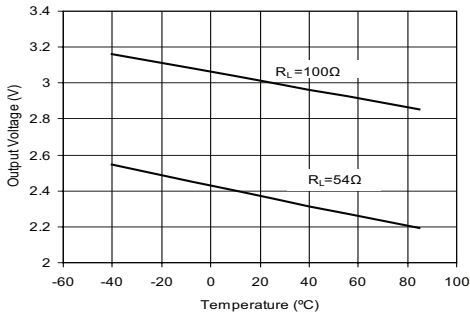
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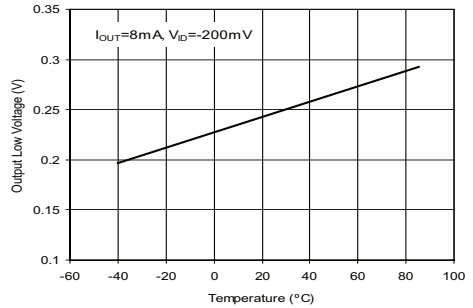
Output Current vs Driver Output High Voltage



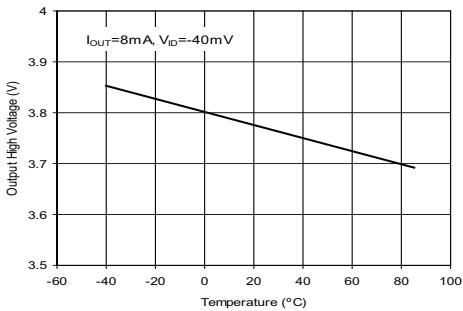
Driver Output Current vs Differential Output Voltage



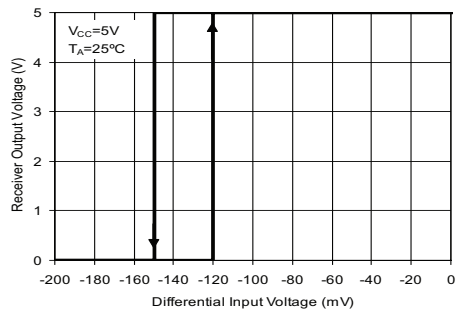
Driver Differential Output Voltage vs Temperature



Receiver Output Low Voltage vs Temperature



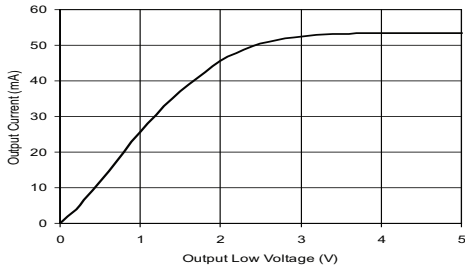
Receiver Output High Voltage vs Temperature



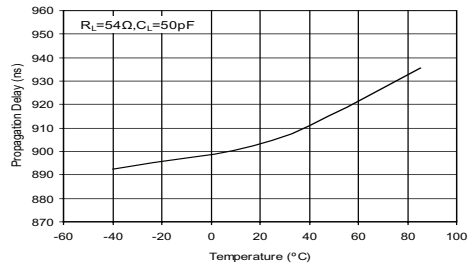
Receiver Output Voltage vs Differential Input Voltage



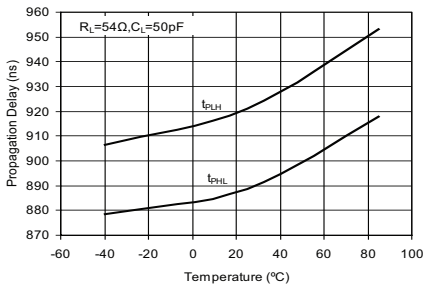
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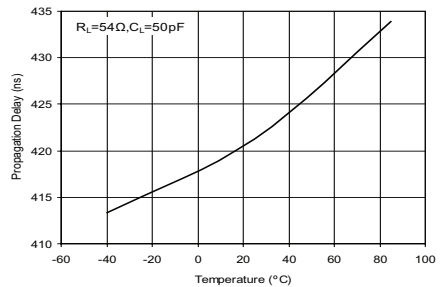
Output Current vs Receiver Output Low Voltage



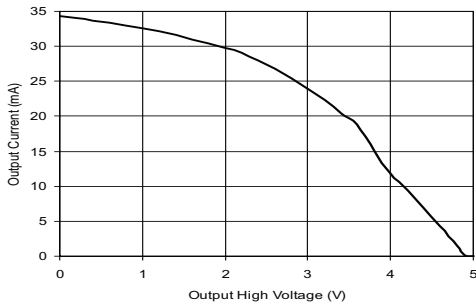
Driver Average Propagation Delay vs Temperature (SP3080E-SP3082E)



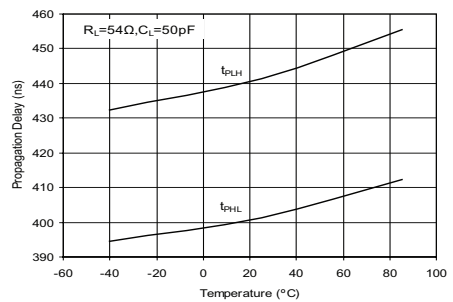
Driver Propagation Delay vs Temperature (SP3080E-SP3082E)



Driver Average Propagation Delay vs Temperature (SP3083E-SP3085E)

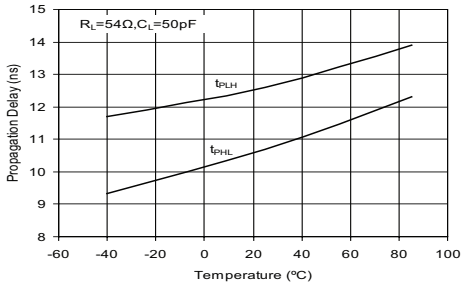


Output Current vs Receiver Output High Voltage

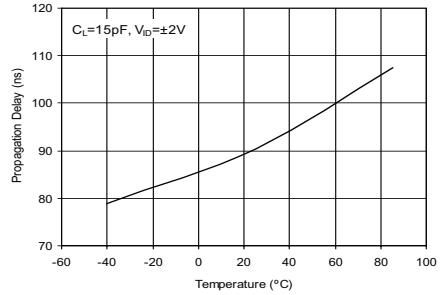


Driver Propagation Delay vs Temperature (SP3083E-SP3085E)

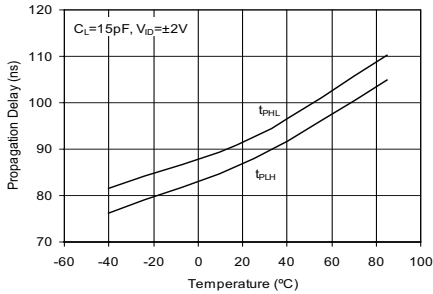
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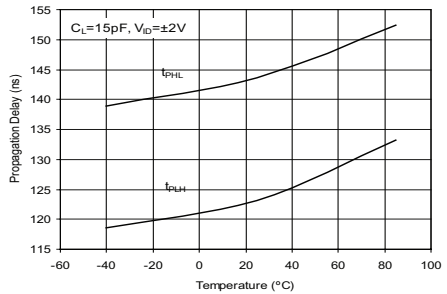
Driver Propagation Delay vs Temperature (SP3086E-SP3088E)



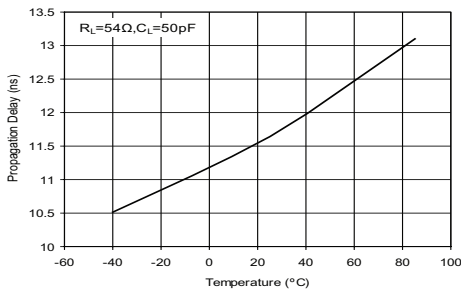
Receiver Average Propagation Delay vs Temperature (SP3080E-SP3082E)



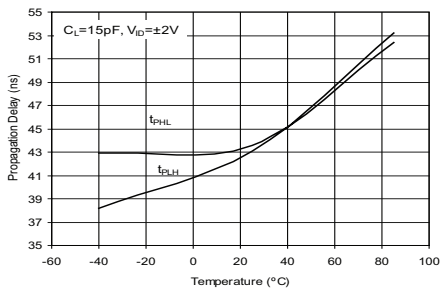
Receiver Propagation Delay vs Temperature (SP3080E-SP3082E)



Receiver Propagation Delay vs Temperature (SP3083E-SP3085E)

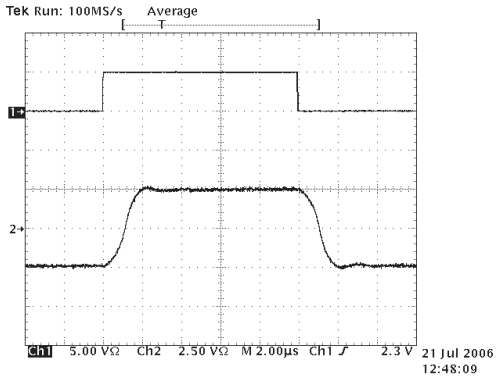


Driver Average Propagation Delay vs Temperature (SP3086E-SP3088E)

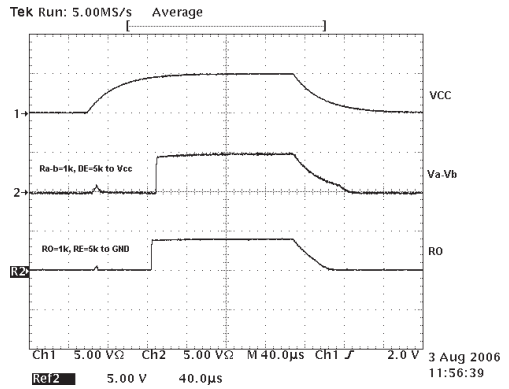


Receiver Propagation Delay vs Temperature (SP3086E-SP3088E)

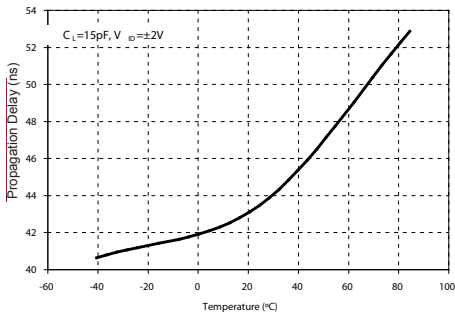
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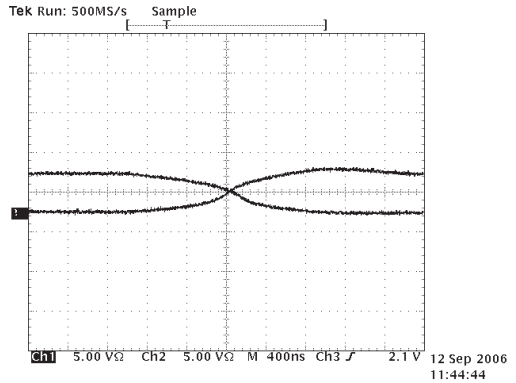
Driver Propagation Delay  
(SP3080E-SP3082E)



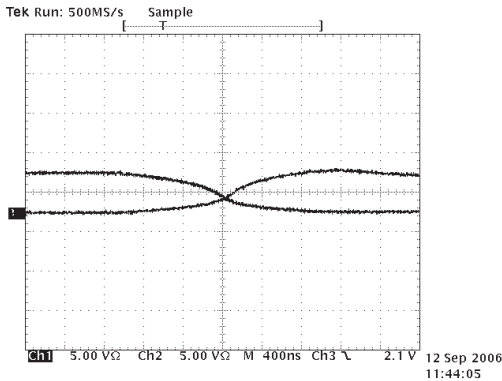
Driver and Receiver Hot Swap  
Performance vs. Vcc



Receiver Average Propagation Delay vs  
Temperature (SP3086E-SP3088E)

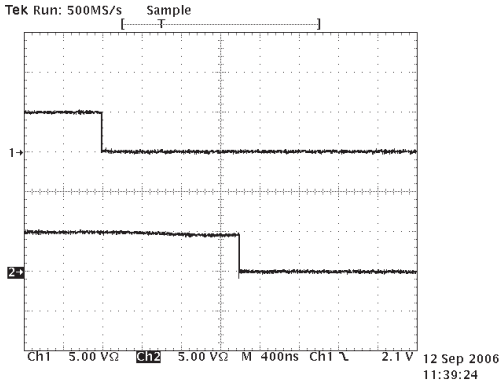


Driver output Waveform  
Low to High (SP3080E-SP3082E)

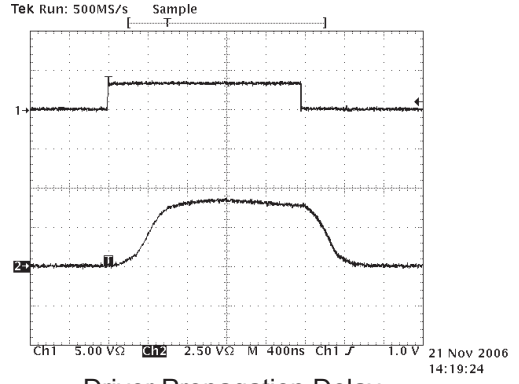


Driver output Waveform  
High to Low (SP3080E-SP3082E)

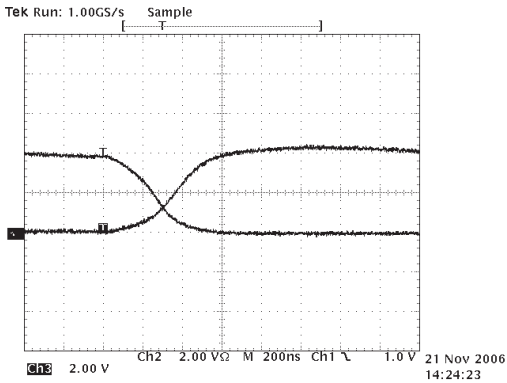
# TYPICAL PERFORMANCE CHARACTERISTICS



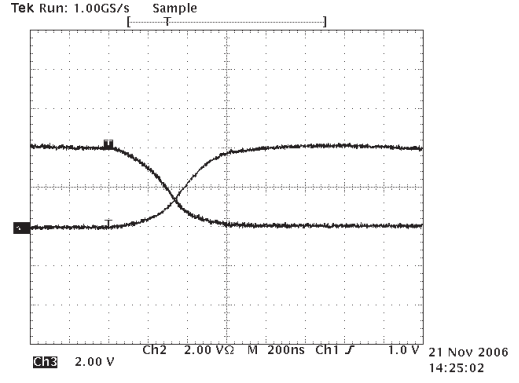
Driver and Receiver Waveform  
High to Low (SP3080E-SP3082E)



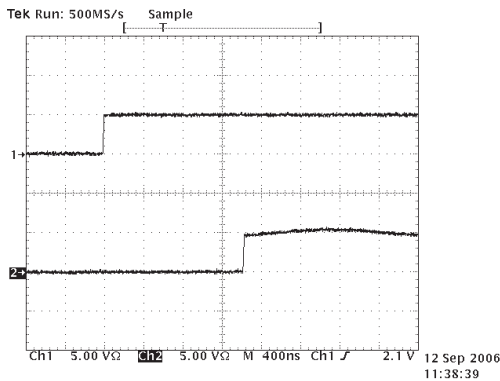
Driver Propagation Delay  
(SP3083E-SP3085E)



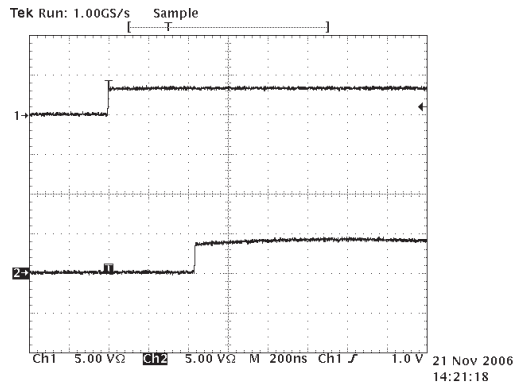
Driver Output Waveform  
Low to High (SP3083E-SP3085E)



Driver Output Waveform  
High to Low (SP3083E-SP3085E)

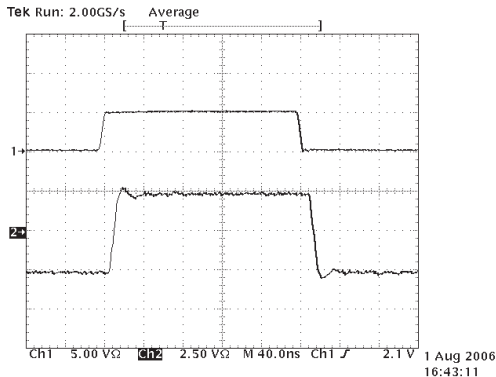


Driver and Receiver Waveform  
Low to High (SP3080E-SP3082E)

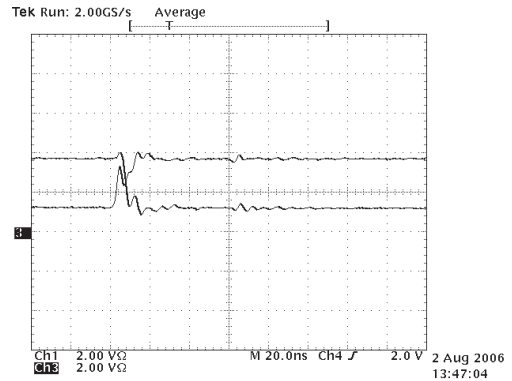


Driver and Receiver Waveform  
Low to High (SP3083E-SP3085E)

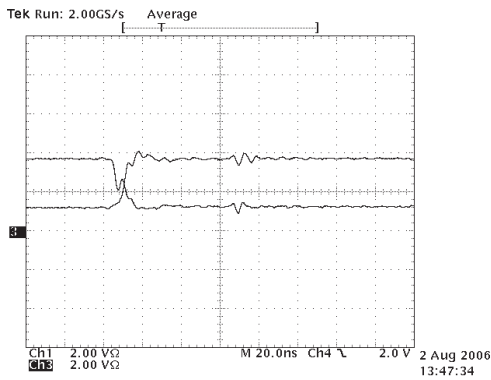
# TYPICAL PERFORMANCE CHARACTERISTICS



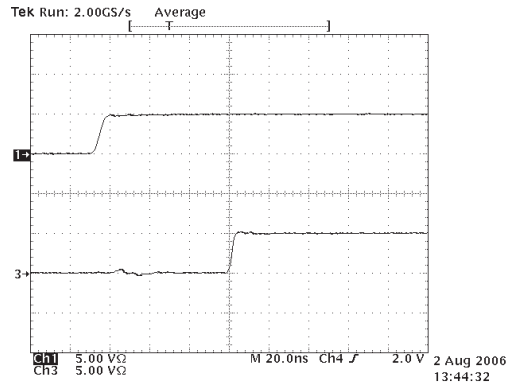
Driver Propagation Delay  
(SP3086E-SP3088E)



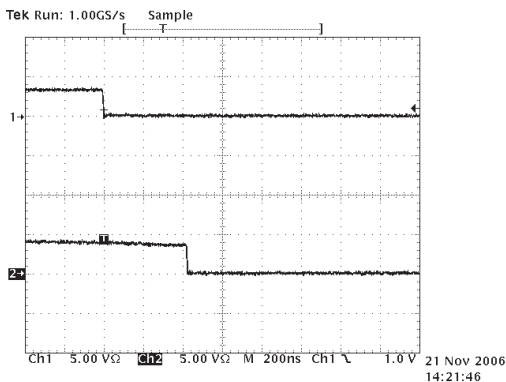
Driver Output Waveform  
Low to High (SP3086E-SP3088E)



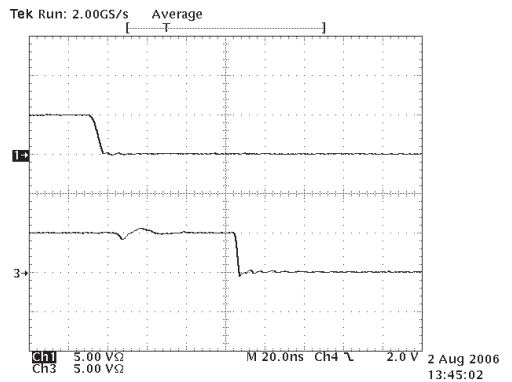
Driver Output Waveforms  
High to Low (SP3086E-SP3088E)



Driver and Receiver Waveform  
Low to High (SP3086E-SP3088E)

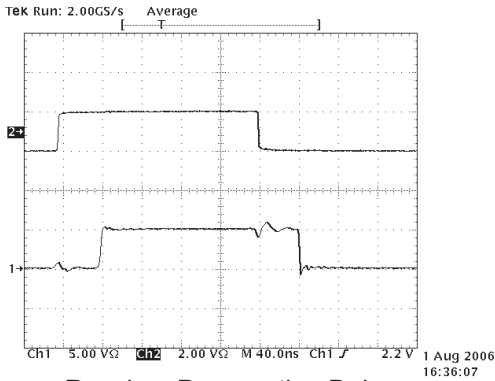


Driver and Receiver Waveform  
High to Low (SP3083E-SP3085E)

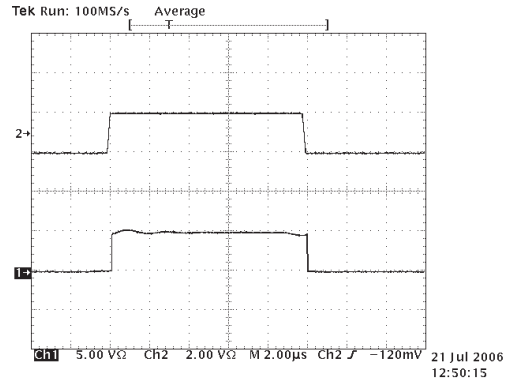


Driver and Receiver Waveform  
High to Low (SP3086E-SP3088E)

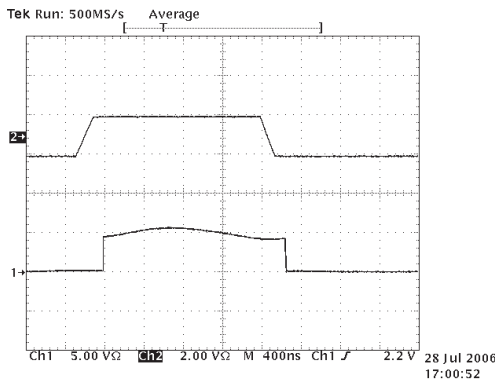
# TYPICAL PERFORMANCE CHARACTERISTICS



Receiver Propagation Delay  
(SP3086E-SP3088E)



Receiver Propagation Delay  
(SP3080E-SP3082E)



Receiver Propagation Delay  
(SP3083E-SP3085E)

## TEST CIRCUITS

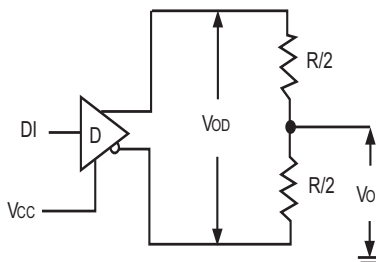


Figure 1. Driver DC Test Circuit

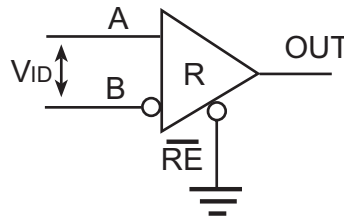


Figure 2. Receiver DC Test Circuit

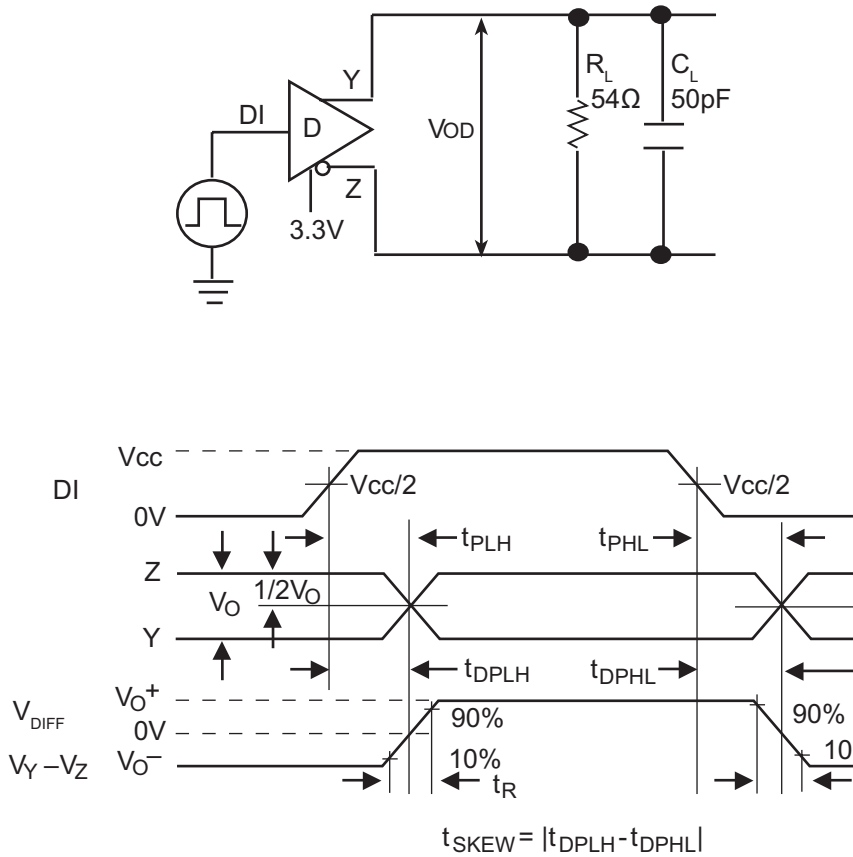


Figure 3. Driver Propagation Delay Time Test Circuit and Timing Diagram

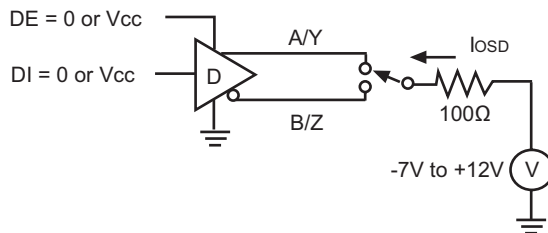


Figure 4. Driver Short Circuit Current Limit Test Circuit

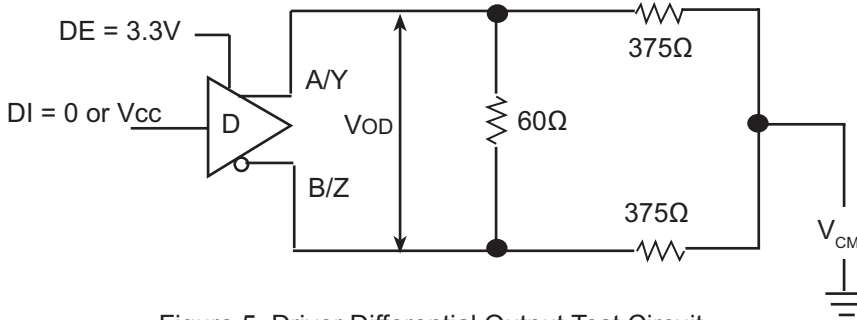


Figure 5. Driver Differential Output Test Circuit

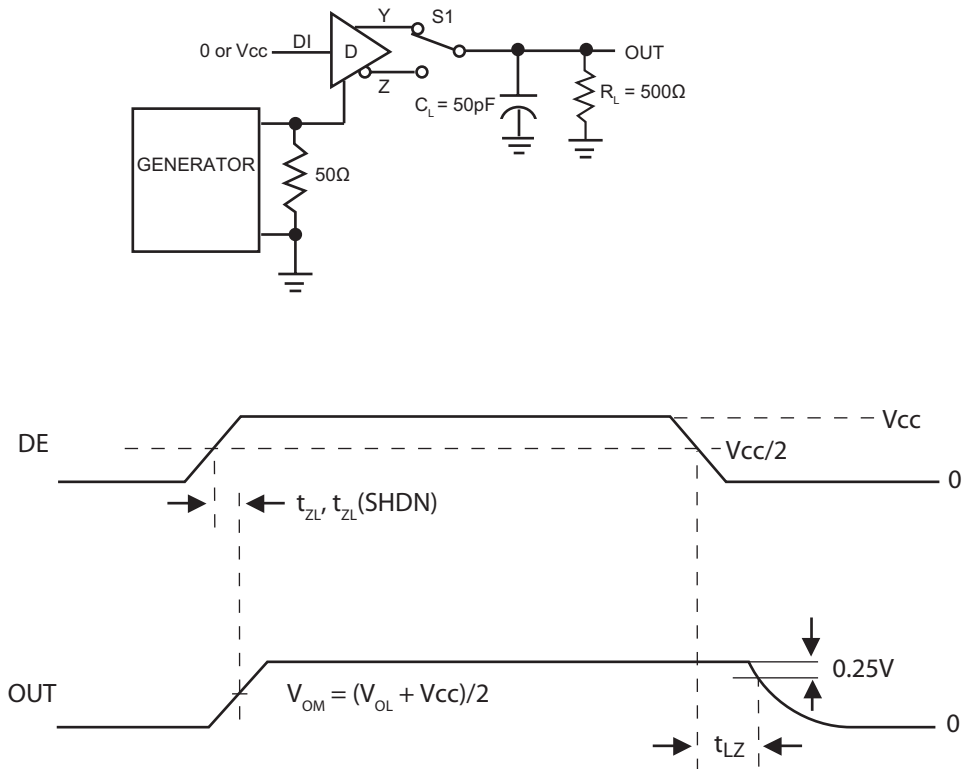
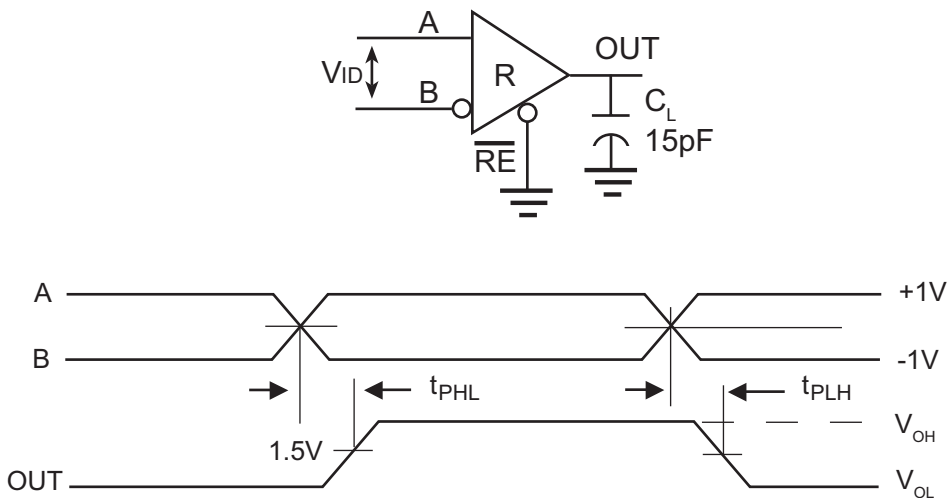
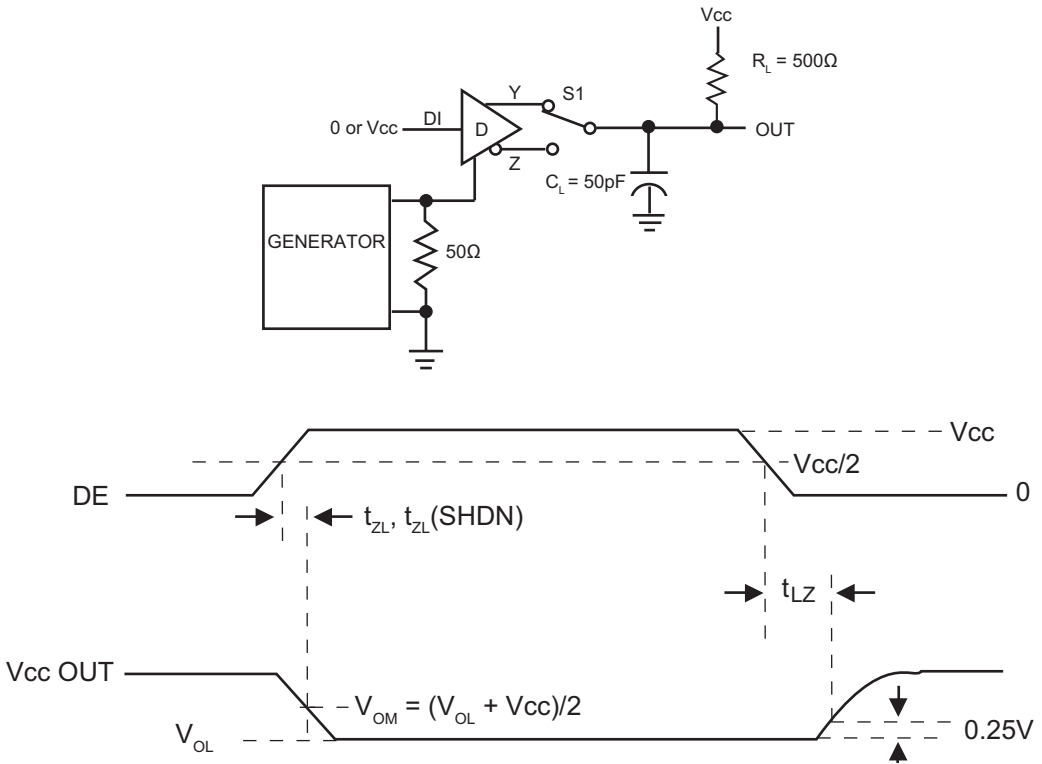


Figure 6. Driver Enable and Disable Times Test Circuit and Timing Diagram





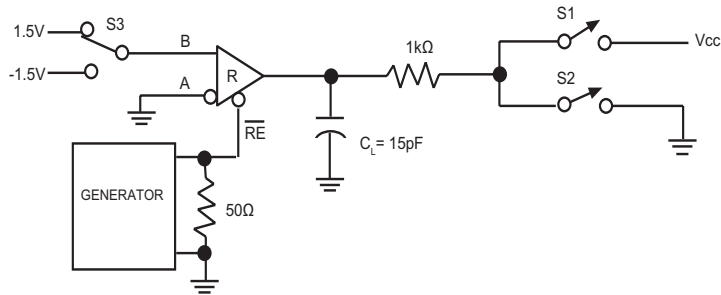
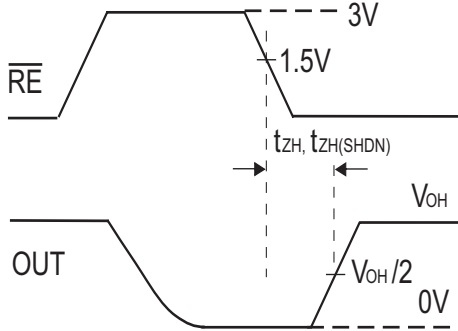
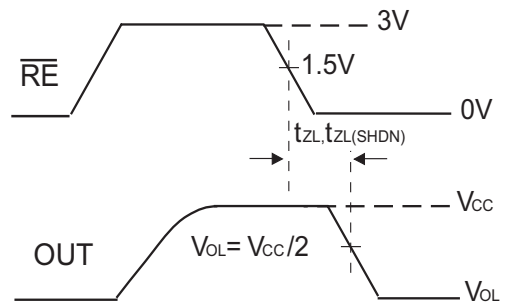


Figure 9. Receiver Enable and Disable Times Test Circuit

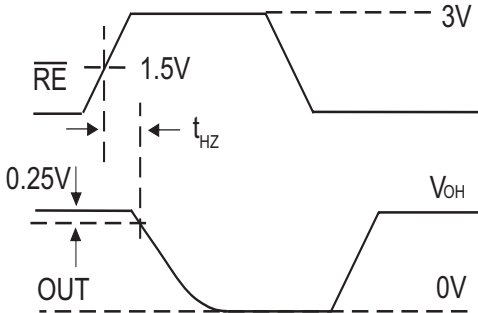
S1 is open, S2 is closed, S3 = 1.5V



S1 is closed, S2 is open, S3 = -1.5V



S1 is open, S2 is closed, S3 = 1.5V



S1 is closed, S2 is open, S3 = -1.5V

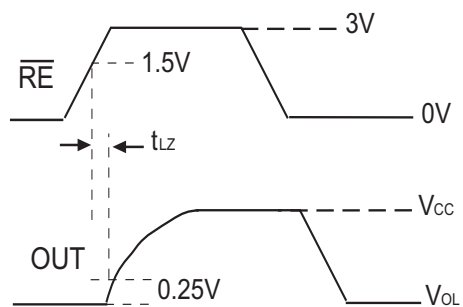
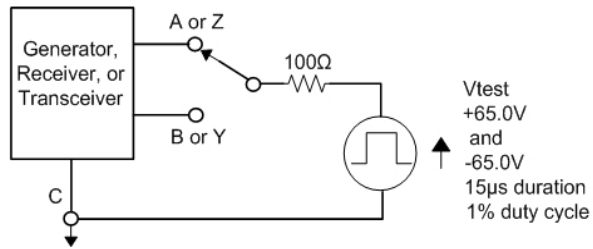


Figure 10. Receiver Enable and Disable Timing Diagram

Power-on or Power-off



Note: Test is performed to ensure survivability only. Normal operation during transient is not specified.

Figure 11. Transient Over Voltage Tolerance Test Circuit

SP3080E, SP3083E, SP3086E (Full Duplex)

Transmitting				
Inputs			Outputs	
$\overline{RE}$	DE	DI	Y	Z
X	1	1	1	0
X	1	0	0	1
0	0	X	High-Z	
1	0	X	Shutdown	

Receiving			
Inputs			Output
$\overline{RE}$	DE	$V_A - V_B$	RO
0	X	$\geq -40mV$	1
0	X	$\leq -200mV$	0
0	X	Open/shorted	1
1	1	X	High-Z
1	0	X	Shutdown

SP3081E SP3084E, SP3087E (Full Duplex)

Transmitting		
Input	Outputs	
DI	Y	Z
1	1	0
0	0	1
Open	1	0

Receiving	
Inputs	Output
$V_A - V_B$	RO
$\geq -40mV$	1
$\leq -200mV$	0
Open/shorted	1

SP3082E SP3085E, SP3088E (Half Duplex)

Transmitting				
Inputs			Outputs	
$\overline{RE}$	DE	DI	A	B
X	1	1	1	0
X	1	0	0	1
0	0	X	High-Z	
1	0	X	Shutdown	

Receiving			
Inputs			Output
$\overline{RE}$	DE	$V_A - V_B$	RO
0	X	$\geq -40mV$	1
0	X	$\leq -200mV$	0
0	X	Open/shorted	1
1	1	X	High-Z
1	0	X	Shutdown

Note: Receiver inputs  $-200mV < V_A - V_B < -40mV$ , should be considered indeterminate

PRODUCT SELECTOR GUIDE

Part Number	Duplex	Data Rate (Mbps)	Shut-down	Receiver & Driver Enable	Trans on Bus	Foot-print	pin-compatible upgrade from:
SP3080E	Full	0.115	Yes	Yes	256	SN75180	MAX3080
SP3081E	Full	0.115	No	No	256	SN75179	MAX3081
SP3082E	Half	0.115	Yes	Yes	256	SN75176	SP483, MAX3082
SP3083E	Full	0.5	Yes	Yes	256	SN75180	MAX3083
SP3084E	Full	0.5	No	No	256	SN75179	MAX3084
SP3085E	Half	0.5	Yes	Yes	256	SN75176	MAX3085
SP3086E	Full	20	Yes	Yes	256	SN75180	SP1491, MAX3086
SP3087E	Full	20	No	No	256	SN75179	SP1490, MAX3087
SP3088E	Half	20	Yes	Yes	256	SN75176	SP1481, MAX3088

**DETAILED DESCRIPTION**

SP3080E-SP3088E is a family of advanced RS-485/RS-422 transceivers. Each contains one driver and one receiver. These devices feature fail-safe circuitry that guarantees a logic-high receiver output when the receiver inputs are open or shorted, or when they are connected to a terminated transmission line with all drivers disabled. SP3080E, SP3082E, SP3083E, SP3085E, SP3086E and SP3088E also feature a hot-swap capability allowing live insertion without error data transfer.

The SP3080E, SP3081E and SP3082E feature reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission up to 115kbps. The SP3083E, SP3084E and SP3085E also offer slew-rate limits allowing transmit speeds up to 500kbps. The SP3086E, SP3087E, SP3088E driver slew rates are not limited, making transmit speeds up to 20Mbps possible.

The SP3082E, SP3085E and SP3088E are half-duplex transceivers, while the SP3080E, SP3081E, SP3083E, SP3084E, SP3086E, and SP3087E are full duplex transceivers.

All devices operate from a single 5.0V supply. Drivers are output short-circuit current limited. Thermal-shutdown circuitry protects drivers against excessive power dissipation. When activated, the thermal-shutdown circuitry places the driver outputs into a high-impedance state.

**RECEIVER INPUT FILTERING**

SP3080E-SP3085E receivers incorporate input filtering in addition to input hysteresis. This filtering enhances noise immunity with differential signals that have very slow rise and fall times. Receiver propagation delay increases due to this filtering.

**ADVANCED FAIL SAFE**

Ordinary RS485 differential receivers will be in an indeterminate state whenever A - B is less than  $\pm 200\text{mV}$ . This situation can occur whenever the data bus is not being actively driven. The Advanced Failsafe feature of the SP3080E family guarantees a logic-high receiver output if the receiver's differential inputs are shorted, open-circuit, or if they are shunted by a termination resistor.

The receiver thresholds of the SP3080E family, are very precise and offset by at least a 40mV noise margin from ground. This results in a logic-high receiver output at zero volts input differential while maintaining compliance with the EIA/TIA-485 standard of  $\pm 200\text{mV}$ .

**HOT-SWAP CAPABILITY**

When a micro-processor or other logic device undergoes its power-up sequence its logic-outputs are typically at high impedance. In this state they are unable to drive the DE and signals to a defined logic level. During this period, noise, parasitic coupling or leakage from other devices could cause standard CMOS enable inputs to drift to an incorrect logic level.

If circuit boards are inserted into an energized backplane (commonly called "live insertion" or "hot-swap") power may be suddenly applied to all circuits. Without the hot-swap capability, this situation could improperly enable the transceiver's driver or receiver, driving invalid data onto shared busses and possibly causing driver contention or device damage.

The SP3080E family contains a special power-on-reset circuit that holds DE low and RE high for approximately 10 microseconds. After this initial power-up sequence the hot-swap circuit becomes transparent, allowing for normal, unskewed enable and disable timings.

 **$\pm 15\text{KV}$  ESD PROTECTION**

ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver output and receiver inputs of the SP3080E family have extra protection against static electricity. Exar uses state of the art structures to protect these pins against ESD of  $\pm 15\text{kV}$  without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, the SP3080E - SP3088E keeps working without latch-up or damage.

ESD protection can be tested in various ways. The transmitter outputs and receiver inputs of

the SP3080E - SP3088E are characterized for protection to the following limits:

- ±15kV using the Human Body Model
- ±8kV using the Contact Discharge method specified in IEC 61000-4-2
- ±15kV Air-gap

### ESD TEST CONDITIONS

ESD performance depends on a variety of conditions. Contact Exar for a reliability report that documents test setup, methodology and results.

### IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The SP3080E family helps you design equipment to meet IEC 61000-4-2, without sacrificing board space and cost for external ESD-protection components.

The major difference between tests done using the Human Body Model and IEC 61000-4-2 is a higher peak current in IEC 61000-4-2 series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the human body model.

The air-gap test involves approaching the device with a charged probe. The contact discharge method connects the probe to the device before the probe is energized.

### MACHINE MODEL

The machine model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. The objective is to emulate the stress caused when I/O pins are contacted by handling equipment during test and assembly.

### 256 TRANSCEIVERS ON THE BUS

The standard RS-485 receiver input impedance is 12k $\Omega$  (1 unit load). A standard driver can drive up to 32 unit loads. The SP3080E family of transceivers has only a 1/8th unit load receiver input impedance (96k $\Omega$ ), thereby allowing eight times as many, up to 256, transceivers to be connected in parallel on a communication line. Any combination of these devices and other RS-485 transceivers up to a total of 32 unit loads may be connected to the line.

### LOW POWER SHUTDOWN MODE

Low-power shutdown mode is initiated by bringing both RE high and DE low simultaneously. While in shutdown devices typically draw only 50nA of supply current. DE and RE may be tied together and driven by a single control signal. Devices are guaranteed not to enter shutdown if RE is high and DE is low for less than 50ns. If the inputs are in this state for at least 600ns, the parts are shutdown.

Enable times  $t_{ZH}$  and  $t_{ZL}$  apply when the part is not in low-power shutdown state. Enable times  $t_{ZH}(SHDN)$  and  $t_{ZL}(SHDN)$  apply when the parts are shut down. The drivers and receivers take longer to become enabled from low power shutdown mode  $t_{ZL}(SHDN)$  and  $t_{ZL}(SHDN)$  than from driver/receiver-disable mode ( $t_{ZH}$ ,  $t_{ZL}$ ).

### DRIVER OUTPUT PROTECTION

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. First, a driver-current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range. Second, a thermal-shutdown circuit forces the driver outputs into a high-impedance state if junction temperature becomes excessive.

### LINE LENGTH, EMI, AND REFLECTIONS

SP3080E - SP3085E feature controlled slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables.

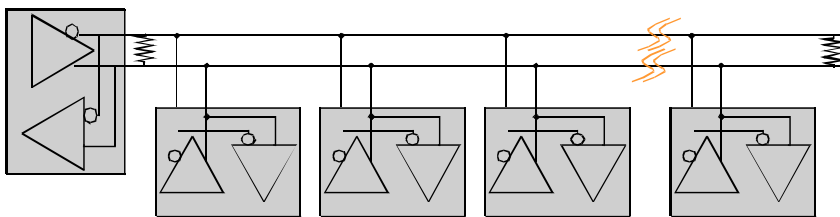
SP3080E - SP3083E driver rise and fall times are limited to no faster than 667ns, allowing error-free data transmission up to 115kbps. The SP3083E, SP3084E and SP3085E offer somewhat higher driver output slew-rate limits, allowing transmit speeds up to 500kbps.

The RS-485/RS-422 standard covers line lengths up to 4,000ft. Maximum achievable line length is a function of signal attenuation and noise. Use of slew-controlled drivers such as the SP3080E-SP3086E may help to reduce crosstalk interference and permit communication over longer transmission lines.

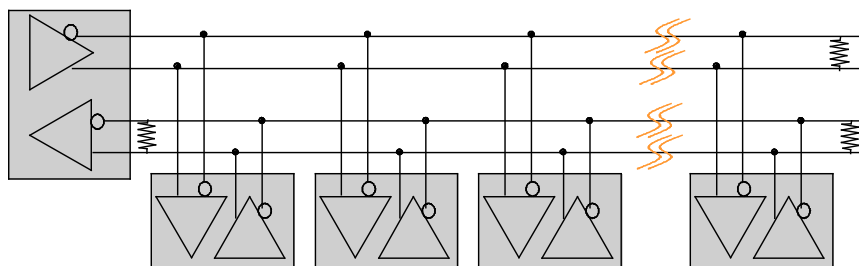
Termination prevents reflections by eliminating the impedance mismatches on a transmission line. Line termination is typically used if rise and fall times are shorter than the round-trip signal propagation time. Slew-limited drivers may reduce or eliminate the need for cable termination in many applications.

#### TYPICAL APPLICATIONS:

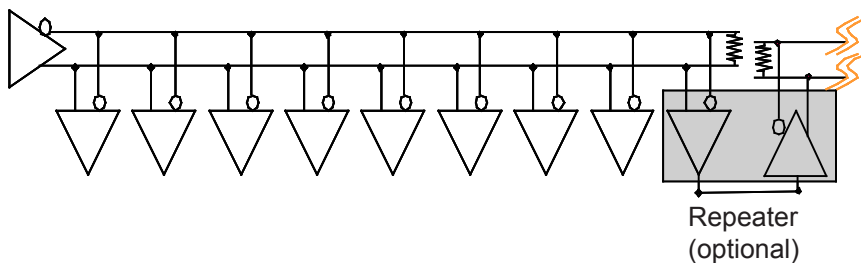
##### Half-Duplex Network



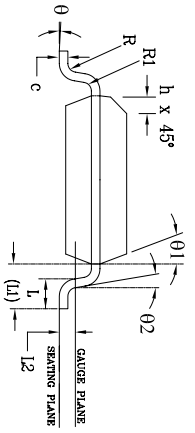
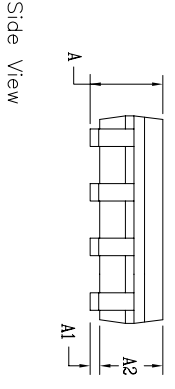
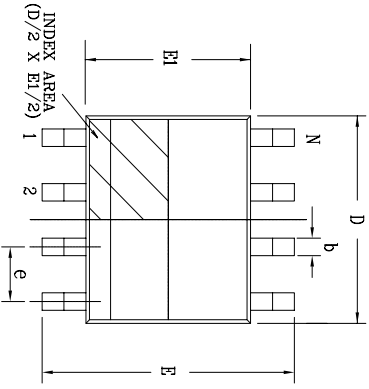
##### Bi-Directional Full-Duplex Network



##### Point to Multi-Point Repeater



REVISION HISTORY			
REV.	DESCRIPTION	DATE	APP'D
A	DRAWING ORIGINATOR	08/16/05	JL
B	DRAWING FORMAT MODIFICATION	07/19/06	JL
C	CHANGE DRAWING LOGO AND COMPANY NAME	11/16/07	JL

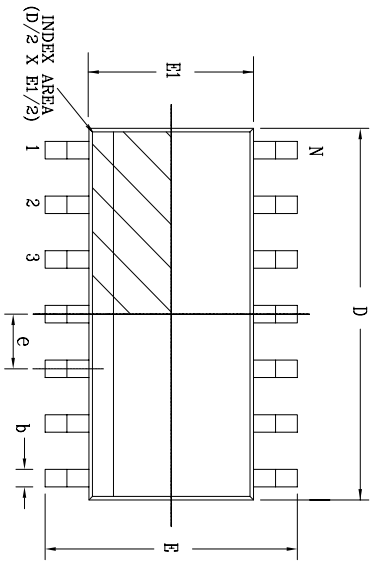


SYMBOLS	8 Pin SOICN JEDEC MS-012 Variation AA			DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	—	1.75	0.053	—	0.069	—	—	—
A1	0.10	—	0.25	0.004	—	0.010	—	—	—
A2	1.25	—	1.65	0.049	—	0.065	—	—	—
b	0.31	—	0.51	0.012	—	0.020	—	—	—
c	0.17	—	0.25	0.007	—	0.010	—	—	—
E	6.00	BSC	—	0.236	BSC	—	—	—	—
E1	3.90	BSC	—	0.154	BSC	—	—	—	—
e	1.27	BSC	—	0.050	BSC	—	—	—	—
h	0.25	—	0.50	0.010	—	0.020	—	—	—
L	0.40	—	1.27	0.016	—	0.050	—	—	—
L1	—	1.04	REF	—	0.041	REF	—	—	—
L2	—	0.25	BSC	—	0.010	BSC	—	—	—
R	0.07	—	—	0.003	—	—	—	—	—
R1	0.07	—	—	0.003	—	—	—	—	—
$\theta$	0°	—	8°	0°	—	8°	—	—	—
$\theta1$	5°	—	15°	5°	—	15°	—	—	—
$\theta2$	0°	—	—	0°	—	—	—	—	—
D	—	4.90	BSC	—	0.193	BSC	—	—	—
N	—	8	—	—	8	—	—	—	—

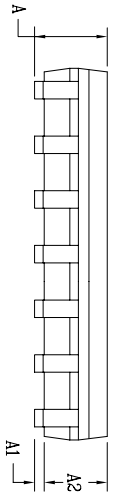
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				8 PIN SOICN PACKAGE OUTLINE
Packaging Approver:	Drawing No:	8-PIN SOICN	Revision:	C
By: JL	Date: 11/16/07	Sheet:	1 OF 1	



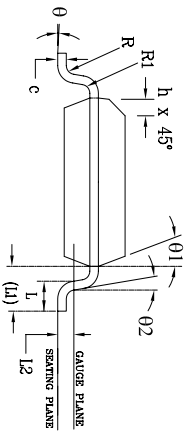
REVISION HISTORY			
REV.	DESCRIPTION	DATE	APP'D
A	DRAWING ORIGINATOR	04/17/06	JL
B	CHANGE DRAWING LOGO AND COMPANY NAME	11/21/07	JL



Top View




Side View



Front View

14 Pin SOICN		JEDEC MS-012		Variation AB		
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	—	1.75	0.053	—	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	1.25	—	1.65	0.049	—	0.065
b	0.31	—	0.51	0.012	—	0.020
c	0.17	—	0.25	0.007	—	0.010
E	6.00	BSC	—	0.236	BSC	—
E1	3.90	BSC	—	0.154	BSC	—
e	1.27	BSC	—	0.050	BSC	—
h	0.25	—	0.50	0.010	—	0.020
L	0.40	—	1.27	0.016	—	0.050
L1	—	1.04	REF	—	0.041	REF
L2	—	0.25	BSC	—	0.010	BSC
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
θ2	0°	—	—	0°	—	—
D	8.65	BSC	—	0.341	BSC	—
N	14	—	—	14	—	—

		<b>EXAR CORPORATION</b> <small>Advanced Connectivity</small>	
Packaging Approval:	14 PIN SOICN PACKAGE OUTLINE	Drawing No.:	14-PIN SOICN
By: JL	Date: 11/21/07	Revision: B	Sheet: 1 OF 1

Part number	LEAD FREE	Tape & Reel	Temperature range	Package Type
SP3080EEN	-L	/TR	From -40 to +85°C	14 pin nSOIC
SP3081EEN	-L	/TR	From -40 to +85°C	8 pin nSOIC
SP3082EEN	-L	/TR	From -40 to +85°C	8 pin nSOIC
SP3083EEN	-L	/TR	From -40 to +85°C	14 pin nSOIC
SP3084EEN	-L	/TR	From -40 to +85°C	8 pin nSOIC
SP3085EEN	-L	/TR	From -40 to +85°C	8 pin nSOIC
SP3086EEN	-L	/TR	From -40 to +85°C	14 pin nSOIC
SP3087EEN	-L	/TR	From -40 to +85°C	8 pin nSOIC
SP3088EEN	-L	/TR	From -40 to +85°C	8 pin nSOIC

All packages are available as lead free (RoHS compliant). To order add “-L” suffix to part number. For Tape and Reel add “/TR”. Reel quantity is 2,500 for nSOIC.

Example: SP3082EEN-L/TR = lead free and Tape and Reel. SP3082EEN/TR = standard with Tape and Reel.

### REVISION HISTORY

DATE	REVISION	DESCRIPTION
2/22/07	M	Legacy Sipex Datasheet
06/23/09	1.0.0	Convert to Exar Format and change revision to 1.0.0.
08/26/11	1.0.1	Correct type error to Vcc range on page 4 from Vcc = 5.0V +/-5% to Vcc = 5.0V +/-10%. Add +/-65V transient over voltage tolerance to ABS Maximum Ratings and add Figure 11 test circuit.

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