RTL8306G-GR

SINGLE-CHIP 6-PORT 10/100MBPS ETHERNET SWITCH CONTROLLER WITH DUAL MII/RMII INTERFACES

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for use by the software engineer when programming for Realtek RTL8306G controller chips. Information pertaining to the hardware design of products using these chips is contained in a separate document.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2008/07/09	First release.
1.1	2008/07/22	Revised section 8.3 Lookup Table Function, page 51.

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1. General Description

The RTL8306G is a 6-port Fast Ethernet switch controller that integrates memory, six MACs, and five physical layer transceivers for 10Base-T and 100Base-TX operation into a single chip.

The RTL8306G support a Dual MII/RMII interface for external devices to connect to the 6th MAC, 5th MAC, and 5th PHY. The external device could be a routing engine, HomePNA, HomePlug, or VDSL transceiver depending on the application. In order to accomplish diagnostics in complex network systems, the RTL8306G provides a loopback feature in each port.

The RTL8306G supports several advanced QoS functions with four-level priority queues to improve multimedia or real-time networking applications, including:

- Multi priority assignment
- Differential queue weight
- Port-based and queue-based rate limitation

For multicast applications, the RTL8306G supports IGMPv1/v2/v3 and MLDv1/v2 snooping.

To meet security and management requirements, the RTL8306G supports IEEE 802.1x Port-based/MAC-based Access Control, provides a Port Mirroring function, and also supports five 32-bit MIB Counters on each port.

The RTL8306G supports 16 VLAN groups. These can be configured as port-based VLANs and/or 802.1Q tag-based VLANs. The RTL8306G also supports advanced VLAN setting method for external processor to maintain more than 16 VLAN groups. A VLAN tag or a Realtek proprietary tag can be inserted or removed at the output port. The inserted tag can carry useful information for Router and Gateway applications, such as the source port and the priority of the packet.

The RTL8306G contains a 2K-entry address lookup table and a 16-entry CAM. A 4-way associative hash algorithm avoids hash collisions and maintains forwarding performance. The 2K-entry table provides read/write access from the SMI interface, and each of the entries can be configured as a static entry that does not automatically age out and can only be controlled by the external management processor. For IGMP/MLD snooping application, each of the 2K entries can be configured as a multicast entry that indicates the matched packets will be forwarded to specific multi ports. For IEEE 802.1x application, each of the 2K entries can be configured as an authorized or unauthorized entry.

Maximum packet length can be 1536 or 1552 bytes according to the initial configuration (strapping upon reset). Three types of independent storm filter are provided to filter packet storms, and an intelligent switch engine prevents Head-of-Line blocking problems. The filtering function is supported for IEEE 802.1D specified reserved multicast addresses (01-80-C2-00-00-02 and 01-80-C2-00-00-04 to 01-80-C2-00-00-0F).

The RTL8306G provides flexible LED functions for diagnostics, with four combination modes. An externally managed processor can control the LEDs via SMI.

GreenEthernet Features include:

Link-On and Cable Length Power Saving

The RTL8306G provides link-on and dynamic detection of cable length and dynamic adjustment of power required for the detected cable length. This feature provides high performance with minimum power consumption.

Link-Down Power Saving

The RTL8306G implements link-down power saving on a per-port basis, greatly cutting power consumption when the network cable is disconnected.

To simplify the peripheral circuit, the RTL8306G can use a low-cost PNP transistor to generate 1.8V from a 3.3V power supply.

2. Features

- 6-port switch controller with memory and transceiver for 10Base-T and 100Base-TX with:
  - 5-port 10/100M UTP
  - 5-port 10/100M UTP + 1-port MII/RMII
  - 4-port 10/100M UTP + 2-port MII/RMII
- Supports Dual MII/RMII for router applications, HomePNA, HomePlug, or VDSL solutions.
  - The 6th MAC provides MII or RMII
  - The 5th MAC provides MII or RMII
  - The 5th PHY provides MII or RMII
- Non-blocking wire-speed reception and transmission and non-head-of-line-blocking forwarding
- Complies with IEEE 802.3/802.3u auto-negotiation
- Built-in high efficiency SRAM for packet buffer, with 2K-entry lookup table, 16-entry CAM, and 4-way associative hash algorithm.
- Supports high performance QoS function on each port:
  - Supports 4-level priority queues
  - Weighted round robin service
  - Input/Output port bandwidth control
- Supports IGMP v1/v2/v3 and MLD v1/v2 snooping
- Supports IEEE 802.1x
- Supports IEEE 802.1D
- Supports IEEE 802.1p Traffic Re-marking
- Lookup Table is accessible via SMI
- Supports 32-bit smart counter for per port RX/TX byte/packet count, collision counter, and error counter
- Supports reserved control frame filtering (DID=01-80-C2-00-00-04 ~ 01-80-C2-00-00-0F)
- Supports advanced storm filtering
- Supports Port Mirroring
- Supports interrupt for CPU application
- Supports SMI (Serial Management Interface) for programming and diagnostics
- Optional EEPROM interface for configuration
- Supports MAC and PHY loopback function for diagnosis
- Supports up to 16 VLAN groups
- Flexible 802.1Q port/tag-based VLAN
- Supports special VLAN tag insert or remove function on per-port basis (egress) to separate WAN traffic from LAN traffic
  - VLAN priority tag Insert/Remove function
  - ARP VLAN for broadcast packets
  - Leaky VLAN for unicast packets
- Supports external processor to maintain greater than 16 VLAN groups
- Flexible LED indicators for link, activity, speed, full/half duplex, and collision, as well as user defined LED output

- LEDs blink upon reset for LED diagnostics
- Supports loop detection function with one LED to indicate the existence of a loop
- Optional 1552 byte maximum packet length
- Flow control fully supported:
  - Half duplex: Back pressure flow control
  - Full duplex: IEEE 802.3x flow control
- Optional MDI/MDIX auto crossover for plug-and-play
- Physical layer port Polarity Detection and Correction function
- GreenEthernet Features
  - Link-On and Cable Length Power Saving
  - Link-Down Power Saving
- Robust baseline wander correction for improved 100Base-TX performance
- 25MHz crystal or 3.3V/1.8V OSC input
- Single 3.3V power input can be transformed to 1.8V via a low-cost external BJT transistor
- Low power, 1.8/3.3V, 0.18µm CMOS technology
- 128-pin PQFP package

3. System Applications

- 5-port switches (10Base-T & 100Base-TX)
- xDSL/cable modem router or home gateway applications
- HomePlug bridge solutions

4. Block Diagram

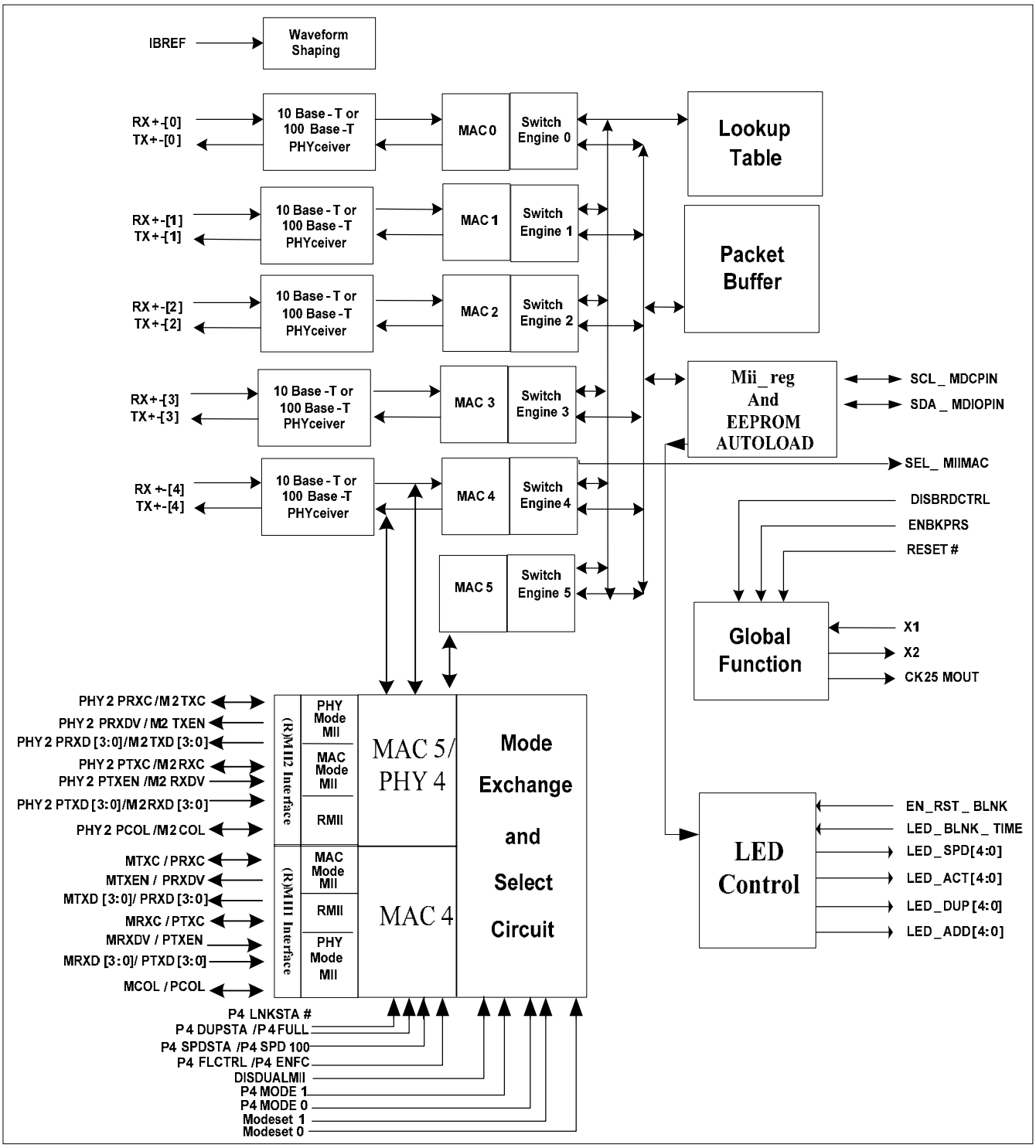


Figure 1. Block Diagram

5. Pin Assignments

5.1. Pin Assignments Diagram

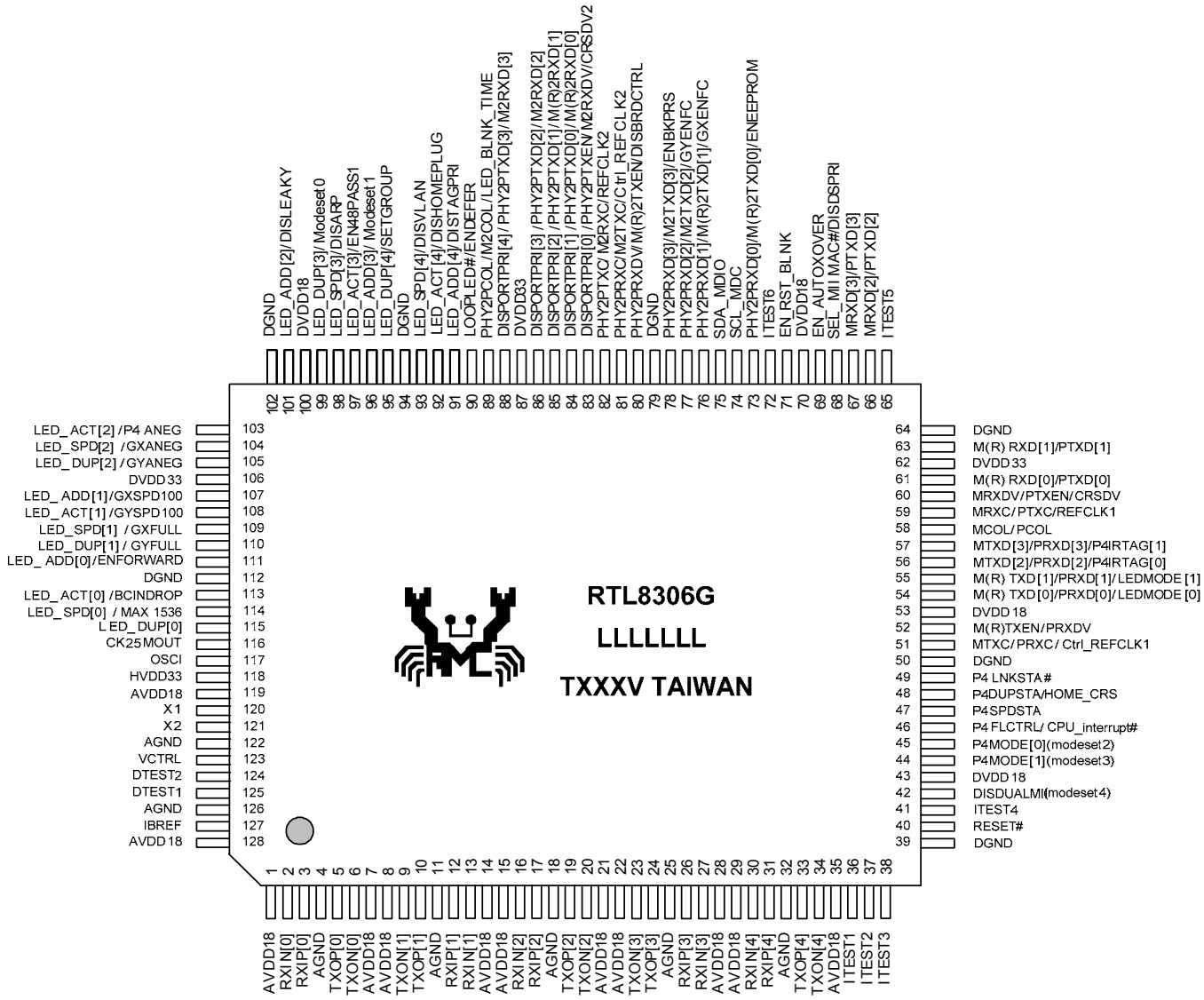


Figure 2. Pin Assignments

5.2. Package Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure 2. The version number is shown in the location marked 'V'.

5.3. Pin Assignments Table

'Type' codes used in the following table: A=Analog, D=Digital, I=Input, O=Output, I/O=Input/Output, I_{PU}=Internal pull-up, I_{PD} =Internal pull-down.

All internal pull-up and pull-down resistors are 75K ohm resistors.

Table 1. Pin Assignments Table

Name	Pin No.	Type
AVDD18	1	AVDD
RXIN[0]	2	AI/O
RXIP[0]	3	AI/O
AGND	4	AGND
TXOP[0]	5	AI/O
TXON[0]	6	AI/O
AVDD18	7	AVDD
AVDD18	8	AVDD
TXON[1]	9	AI/O
TXOP[1]	10	AI/O
AGND	11	AGND
RXIP[1]	12	AI/O
RXIN[1]	13	AI/O
AVDD18	14	AVDD
AVDD18	15	AVDD
RXIN[2]	16	AI/O
RXIP[2]	17	AI/O
AGND	18	AGND
TXOP[2]	19	AI/O
TXON[2]	20	AI/O
AVDD18	21	AVDD
AVDD18	22	AVDD
TXON[3]	23	AI/O
TXOP[3]	24	AI/O
AGND	25	AGND
RXIP[3]	26	AI/O
RXIN[3]	27	AI/O
AVDD18	28	AVDD
AVDD18	29	AVDD
RXIN[4]	30	AI/O
RXIP[4]	31	AI/O
AGND	32	AGND
TXOP[4]	33	AI/O
TXON[4]	34	AI/O
AVDD18	35	AVDD
ITEST1	36	-
ITEST2	37	-

Name	Pin No.	Type
ITEST3	38	-
DGND	39	DGND
RESET#	40	I
ITEST4	41	-
DISDUALMII(modeset4)	42	I (I_{PU})
DVDD18	43	DVDD
P4MODE[1] (modeset3)	44	I (I_{PU})
P4MODE[0] (modeset2)	45	I (I_{PU})
P4FLCTRL/CPU_interrupt#	46	I/O (I_{PU})
P4SPDSTA	47	I (I_{PU})
P4DUPSTA/HOME_CRS	48	I (I_{PU})
P4LNKSTA#	49	I (I_{PU})
DGND	50	DGND
MTXC/PRXC/Ctrl_REFCLK1	51	I/O(I_{PU})
M(R)TXEN/PRXDV	52	I/O(I_{PD})
DVDD18	53	DVDD
M(R)TXD[0]/PRXD[0]/ LEDMODE[0]	54	I/O(I_{PU})
M(R)TXD[1]/PRXD[1]/ LEDMODE[1]	55	I/O(I_{PU})
MTXD[2]/PRXD[2]/ P4IRTAG[0]	56	I/O(I_{PU})
MTXD[3]/PRXD[3]/ P4IRTAG[1]	57	I/O(I_{PU})
MCOL/PCOL	58	I/O(I_{PD})
MRXC/PTXC/REFCLK1	59	I/O(I_{PU})
MRXDV/PTXEN/CRSDV	60	I (I_{PD})
M(R)RXD[0]/PTXD[0]	61	I (I_{PU})
DVDD33	62	DVDD
M(R)RXD[1]/PTXD[1]	63	I (I_{PU})
DGND	64	DGND
ITEST5	65	-
MRXD[2]/PTXD[2]	66	I (I_{PU})
MRXD[3]/PTXD[3]	67	I (I_{PU})
SEL_MIIMAC#/DISDSPRI	68	I/O(I_{PU})
EN_AUTOXOVER	69	I (I_{PU})
DVDD18	70	DVDD
EN_RST_BLNK	71	I (I_{PU})

Name	Pin No.	Type
ITEST6	72	-
PHY2PRXD[0]/M(R)2TXD[0]/ ENEEPROM	73	I/O(I_{PU})
SCL_MDC	74	I/O(I_{PU})
SDA_MDIO	75	I/O(I_{PU})
PHY2PRXD[1]/M(R)2TXD[1]/ GXENFC	76	I/O(I_{PU})
PHY2PRXD[2]/M2TXD[2]/ GYENFC	77	I/O(I_{PU})
PHY2PRXD[3]/M2TXD[3]/ ENBKPRS	78	I/O(I_{PU})
DGND	79	DGND
PHY2PRXDV/M(R)2TXEN/ DISBRDCTRL	80	I/O(I_{PU})
PHY2PRXC/M2TXC/ Ctrl_REFCLK2	81	I/O(I_{PU})
PHY2PTXC/M2RXC/ REFCLK2	82	I/O(I_{PU})
DISPORTPRI[0]/PHY2PTXEN/ M2RXDV/CRSDV2	83	I (I_{PU})
DISPORTPRI[1]/ PHY2PTXD[0]/M(R)2RXD[0]	84	I (I_{PU})
DISPORTPRI[2]/ PHY2PTXD[1]/M(R)2RXD[1]	85	I (I_{PU})
DISPORTPRI[3]/ PHY2PTXD[2]/M2RXD[2]	86	I (I_{PU})
DVDD33	87	DVDD
DISPORTPRI[4]/ PHY2PTXD[3]/M2RXD[3]	88	I (I_{PU})
PHY2PCOL/M2COL/ LED_BLNK_TIME	89	I/O(I_{PU})
LOOPLED#/ENDEFER	90	I/O(I_{PU})
LED_ADD[4]/DISTAGPRI	91	I/O(I_{PU})
LED_ACT[4]/DISHOMEPLUG	92	I/O(I_{PU})
LED_SPD[4]/DISVLAN	93	I/O(I_{PU})
DGND	94	DGND
LED_DUP[4]/SETGROUP	95	I/O(I_{PU})

Name	Pin No.	Type
LED_ADD[3]/Modeset1	96	I/O(I_{PU})
LED_ACT[3]/EN48PASS1	97	I/O(I_{PU})
LED_SPD[3]/DISARP	98	I/O(I_{PU})
LED_DUP[3]/Modeset0	99	I/O(I_{PU})
DVDD18	100	DVDD
LED_ADD[2]/DISLEAKY	101	I/O(I_{PU})
DGND	102	DGND
LED_ACT[2]/P4ANEG	103	I/O(I_{PU})
LED_SPD[2]/GXANEG	104	I/O(I_{PU})
LED_DUP[2]/GYANEG	105	I/O(I_{PU})
DVDD33	106	DVDD
LED_ADD[1]/GXSPD100	107	I/O(I_{PU})
LED_ACT[1]/GYSPD100	108	I/O(I_{PU})
LED_SPD[1]/GXFULL	109	I/O(I_{PU})
LED_DUP[1]/GYFULL	110	I/O(I_{PU})
LED_ADD[0]/ENFORWARD	111	I/O(I_{PU})
DGND	112	DGND
LED_ACT[0]/BCINDROP	113	I/O(I_{PU})
LED_SPD[0]/MAX1536	114	I/O(I_{PU})
LED_DUP[0]	115	I/O(I_{PU})
CK25MOUT	116	I/O
OSCI	117	I/O
HVDD33	118	AVDD
AVDD18	119	AVDD
X1	120	I
X2	121	O
AGND	122	AGND
VCTRL	123	O
DTEST2	124	-
DTEST1	125	-
AGND	126	AGND
IBREF	127	A
AVDD18	128	AVDD

Note 1: 'MII/RMII 1' means MAC 4's MII or RMII; 'MII/RMII 2' means MAC 5/PHY 4's MII or RMII.

Note 2: When 'MII/RMII 2' is not enabled to connect to an external device, pin 83~86 and pin 88 are strapping pins: DISPORTPRI [0:4]. When 'MII/RMII 2' is enabled, these pins are input pins with no strapping function.

6. Pin Descriptions

'Type' codes used in the following tables: A=Analog, D=Digital, I=Input, O=Output, I/O=Input/Output, I_{PU}=Internal pull-up, I_{PD} =Internal pull-down.

All internal pull-up and pull-down resistors are 75K ohm resistors.

Upon Reset

Defined as a short time after the end of a hardware reset.

After Reset

Defined as the time after the specified 'Upon Reset' time.

6.1. Media Connection Pins

Table 2. Media Connection Pins

Pin Name	Pin No.	Type	Drive (mA)	Description	Default
RXIN[0:4]/ RXIP[0:4]	2, 13, 16, 27, 30/ 3, 12, 17, 26, 31	AI	-	Differential Receive Data Input. Port0-4 support 100Base-TX, 10Base-T	UTP
TXOP[0:4]/ TXON[0:4]	5, 10, 19, 24, 33/ 6, 9, 20, 23, 34	AO	-	Differential Transmit Data Output. Port0-4 support 100Base-TX, 10Base-T	UTP

6.2. Mode Configuration Pins

Table 3. Mode Configuration Pin Definitions

Pin Name	Pin No.	Type	Drive (mA)	Description	Default Value
DISDUALMII (modeset4)	42	I (I_{PU})	-	Input Upon Reset. These 5 pins are used together to select the operating modes of Dual MII/RMII: MII/RMII 1 for MAC 4 MII/RMII 2 for MAC 5 or PHY 4 The following sequence is Modeset[4:0] 111xx: MII/RMII 2 not used; MII/RMII 1 not used. Port 4 in UTP (consists of MAC 4/PHY4) Or: MII/RMII 2 not used; MII/RMII 1 is used by MAC 4 in MAC Mode. 110xx: Reserved.	1
P4MODE[1] (modeset3)	44	I (I_{PU})	-		1

Pin Name	Pin No.	Type	Drive (mA)	Description	Default Value
P4MODE[0] (modeset2)	45	I (I_{PU})	-	101xx: MII/RMII 2 not used; MII/RMII 1 is used by MAC 4 in PHY Mode. 10011: MII/RMII 2 not used; MII/RMII 1 is used by MAC 4 in RMII Mode. 011xx: MII/RMII 1 is used by MAC 4 in MAC Mode; MII/RMII 2 used by PHY 4 in PHY Mode. 001xx: MII/RMII 1 is used by MAC 4 in PHY Mode; MII/RMII 2 used by PHY 4 in PHY Mode. 00011: MII/RMII 1 is used by MAC 4 in RMII Mode; MII/RMII 2 used by PHY 4 in RMII Mode. 00010: MII/RMII 1 is used by MAC 4 in PHY Mode; MII/RMII 2 used by MAC 5 in PHY Mode. 00001: MII/RMII 1 is used by MAC 4 in RMII Mode; MII/RMII 2 used by MAC 5 in PHY Mode. 00000: MII/RMII 1 is used by MAC 4 in RMII Mode; MII/RMII 2 used by MAC 5 in RMII Mode. 01011: MII/RMII 2 used by MAC 5 in MAC Mode; Port 4 in UTP (consists of MAC 4/PHY4). Or: MII/RMII 2 used by MAC 5 in MAC Mode. 01001: MII/RMII 2 used by MAC 5 in PHY Mode; Port 4 in UTP (consists of MAC 4/PHY4). Or: MII/RMII 2 used by MAC 5 in PHY Mode Or: MII/RMII 2 used by MAC 5 in PHY Mode; MII/RMII 1 is used by MAC 4 in MAC Mode. 01000: MII/RMII 2 used by MAC 5 in RMII Mode; Port 4 in UTP (consists of MAC 4/PHY4) Or: MII/RMII 2 used by MAC 5 in RMII Mode. 01010: Reserved. 10001: Reserved. 10000: Reserved. 10010: Reserved. After Reset: Pin 96 Modeset1/LED_ADD[3] and Pin 99 Modeset0/LED_DUP [3] used for LED (see Table 7, page 20).	1
LED_ADD[3]/ Modeset1	96	I/O (I_{PU})	4		1
LED_DUP[3]/ Modeset0	99	I/O (I_{PU})	4		-

Pin Name	Pin No.	Type	Drive (mA)	Description	Default Value
SEL_MIIMAC#/ DISDSPRI	68	I/O (I_{PU})	4	Output after reset is SEL_MIIMAC# used for LED: When P4MODE[1:0]=11 and DISDUALMII=1, this pin indicates whether the UTP path or the MII MAC path is selected. Otherwise, this pin is irrelevant. *Note: When P4MODE[1:0]=11 and DISDUALMII=1, the RTL8306G supports UTP/ MAC 4 auto-detection function via the link status of Port4 UTP and the P4LNKSTA# pin. UTP has higher priority than MAC mode MII.* LED On: MII MAC path is selected. LED Off: UTP path is selected. Input upon reset when mode select[4:0]= 00010/00001/00000/1xxxx. This pin is a strapping pin. DisDSPri: Disable Differentiated Service Priority. 1: Disable DS priority 0: Enable DS priority When in other modes, this pin is a strapping pin: P4UTP. To set the operating mode of Port 4 differential pair. 1: UTP mode 0: Reserved	1
P4LNKSTA#	49	I (I_{PU})	-	Port4 Link Status for MAC. This pin determines the link status of Port4 MAC in real-time when Port4 MAC works in MAC mode MII / PHY mode MII/RMII regardless of Port4 PHY circuit interface is disabled or worked in PHY mode MII/RMII. This pin is low active. Pulling this pin down sets the link status of PHY 5 MII register 1.2. 1: No Link 0: Link Regardless of whether DISDUALMII=1 or =0, this pin provides real-time link status to Port4 MAC part in PHY 5 MII register 1.2 when Port4 MAC part is configured in MAC mode MII / PHY mode MII/RMII Mode. When Port4 operates in UTP mode only, the MII/RMII 1 interface is disabled and this pin has no function. It should be left floating.	1
P4DUPSTA/ HOME_CRS	48	I (I_{PU})	-	When HOMEPNA or HOMEPLUG mode is disabled (see Table 9, page 22, pin 92), this is a strapping pin. Upon reset. Port4 Duplex Status: Port4 initial configuration pin for duplex upon reset for PHY in UTP mode, and strap duplex status for MAC of other modes upon reset. 1: Full duplex 0: Half duplex When enabling HOMEPNA or HOMEPLUG mode, this pin is the CRS signal pin of MII.	1

Pin Name	Pin No.	Type	Drive (mA)	Description	Default Value
P4SPDSTA	47	I (I_{PU})	-	Input Upon Reset. Port4 Speed Status: Port4 initial configuration pin for speed status upon reset for PHY of UTP mode only, and strap speed status for MAC of other modes upon reset. 1: 100Mbps 0: 10Mbps	1
P4FLCTRL/ CPU_interrupt#	46	I/O (I_{PU})	-	Input Upon Reset. Port4 Flow Control: Port4 initial configuration pin for flow control upon reset for PHY of UTP mode, and strap flow control status for MAC of other modes upon reset. 1: Enable Flow Control ability 0: Disable Flow Control ability Output After Reset: Provide interrupt signal to CPU when interrupt events occur.	1

6.3. Port4 MAC Circuit Interface Pins

The external device must be 3.3V compatible as the digital output of the RTL8306G is 3.3V.

Table 4. Port4 MAC Circuit Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description	Default
MRXD[3]/ PTXD[3]	67	I (I_{PU})	-	When MII/RMII 1 is used by MAC 4 in MAC mode, this pin is input pin MRXD[3]. When MII/RMII 1 is used by MAC 4 in PHY mode, this pin is input pin PTXD[3]. When MII/RMII 1 is used by MAC 4 in RMII mode, this pin is not used.	-
MRXD[2]/ PTXD[2]	66	I (I_{PU})	-	When MII/RMII 1 is used by MAC 4 in MAC mode; this pin is input pin MRXD[2]. When MII/RMII 1 is used by MAC 4 in PHY mode; this pin is input pin PTXD[2]. When MII/RMII 1 is used by MAC 4 in RMII mode; this pin is not used.	-
M(R)RXD[1]/ PTXD[1]	63	I (I_{PU})	-	When MII/RMII 1 is used by MAC 4 in MAC mode; this pin is input pin MRXD[1]. When MII/RMII 1 is used by MAC 4 in PHY mode; this pin is input pin PTXD[1]. When MII/RMII 1 is used by MAC 4 in RMII mode; this pin is input pin RRXD[1].	-

Pin Name	Pin No.	Type	Drive (mA)	Description	Default
M(R)RXD[0]/ PTXD[0]	61	I (I_{PU})	-	When MII/RMII 1 is used by MAC 4 in MAC mode; this pin is input pin MRXD[0]. When MII/RMII 1 is used by MAC 4 in PHY mode; this pin is input pin PTXD[0]. When MII/RMII 1 is used by MAC 4 in RMII mode; this pin is input pin RRXD[0].	-
MRXDV/ PTXEN/ CRSDV	60	I (I_{PD})	-	When MII/RMII 1 is used by MAC 4 in MAC mode. This pin is input pin MRXDV. When MII/RMII 1 is used by MAC 4 in PHY mode; this pin is input pin PTXEN. When MII/RMII 1 is used by MAC 4 in RMII mode; this pin is input pin CRSDV.	-
MRXC/ PTXC/ REFCLK1	59	I/O (I_{PU})	8	When MII/RMII 1 is used by MAC 4 in MAC mode; this pin is input pin MRXC. When MII/RMII 1 is used by MAC 4 in PHY mode; this pin is output pin PTXC. (When MII/RMII 1 is used by MAC 4 in RMII mode, this pin is bi-directional REFCLK 1). When pin 51 is pulled high in this mode upon reset, this pin is an input pin, and can receive an external clock. When pin 51 is pulled down in this mode upon reset, this pin is an output pin, and can output a 50MHz clock).	-
MCOL/ PCOL	58	I/O (I_{PD})	4	When MII/RMII 1 is used by MAC 4 in MAC mode; this pin is input pin MCOL. When MII/RMII 1 is used by MAC 4 in PHY mode; this pin is output pin PCOL. When MII/RMII 1 is used by MAC 4 in RMII mode; this pin is not used.	-
MTXD[3]/ PRXD[3]/ P4IRTAG[1]	57	I/O (I_{PU})	4	Output After Reset. When MII/RMII 1 is used by MAC 4 in MAC mode; this pin is output pin MTXD[3:2]. When MII/RMII 1 is used by MAC 4 in PHY mode; this pin is output pin PRXD[3:2]. When MII/RMII 1 is used by MAC 4 in RMII mode; this pin is not used. Input Upon Reset. The 2 pins are strapping pin P4IRTAG[1:0]: Insert/Remove Priority Tag of Port4. 11: Do not insert/remove VLAN tags to/from packets. 10: Insert PVID to non-tagged packets. 01: Remove tags from tagged packets. 00: Replace the VID with a PVID for tagged packets and insert a PVID to non-tagged packets. *Note: These pins are used for Port4 only. Use serial EEPROM for other ports.*	11
MTXD[2]/ PRXD[2]/ P4IRTAG[0]	56	I/O (I_{PU})	4		

Pin Name	Pin No.	Type	Drive (mA)	Description	Default
M(R)TXD[1]/ PRXD[1]/ LEDMODE[1]	55	I/O (I_{PU})	4	Output After Reset. When MII/RMII 1 is used by MAC 4 in MAC mode; this pin is output pin MTXD [1:0]. When MII/RMII 1 is used by MAC 4 in PHY mode; this pin is output pin PRXD[1:0]. When MII/RMII 1 is used by MAC 4 in RMII mode; this pin is output pin RTXD [1:0]. Input Upon Reset. The two pins are strapping pin LEDMODE[1:0]. Each port has four LED indicator pins. Each pin has different indicator meanings, set by the pins, LEDMODE[1:0]. LEDMODE[1:0]=11: Duplex/Col + Speed + Link/Act + Link/Act/Spd. LEDMODE[1:0]=10: Duplex/Col + Speed + Act + Bi-color Link/Active. LEDMODE[1:0]=01: TxAct + Speed + RxAct + Link. LEDMODE[1:0]=00: Duplex+Speed+Col+Bi-color Link/Act. All LED statuses are represented as active-low or high depending on input strapping, except Bi-color Link/Act in Bi-color LED mode, whose polarity depends on Spd status. Link/Act/Spd: Link, Activity, and Speed Indicator. On for link established. Blinking every 43ms when the corresponding port is transmitting or receiving at 100Mbps. Blinking every 120ms when the port is transmitting or receiving at 10Mbps.	11
M(R)TXD[0]/ PRXD[0]/ LEDMODE[0]	54	I/O (I_{PU})	4		
M(R)TXEN/ PRXDV	52	I/O (I_{PD})	4	When MII/RMII 1 is used by MAC 4 in MAC mode; this pin is output pin MTXEN. When MII/RMII 1 is used by MAC 4 in PHY mode; this pin is output pin PRXDV. When MII/RMII 1 is used by MAC 4 in RMII mode; this pin is output pin RTXEN.	-
MTXC/PRXC/ Ctrl_REFCLK1	51	I/O (I_{PU})	8	When MII/RMII 1 is used by MAC 4 in MAC mode; this pin is input pin MTXC. When MII/RMII 1 is used by MAC 4 in PHY mode; this pin is output pin PRXC. When MII/RMII 1 is used by MAC 4 in RMII mode; this pin is strapping pin Ctrl_REFCLK1. Input Upon Reset. 1: Pin 59 REFCLK1 is input pin 0: Pin 59 REFCLK1 is output pin	1

6.4. Port 4 PHY Circuit Interface Pins

The external device must be 3.3V compatible as the digital output of the RTL8306G is 3.3V.

Table 5. Port 4 PHY Circuit Interface Pin Definitions

Pin Name	Pin No.	Type	Drive (mA)	Description	Default
DISPORTPRI[4]/ PHY2PTXD[3]/ M2RXD[3]	88	I (I_{PU})	-	When MII/RMII 2 is not enabled, this pin is strapping pin DISPORTPRI[4]. To enable port-based priority QoS function on port 4. Upon Reset: 1: Disable port 4 priority 0: Enable port 4 priority After Reset: Ignore any input signal. When MII/RMII 2 is enabled for PHY 4 or MAC 5. For PHY mode MII, this pin is input pin PHY2PTXD[3]. For MAC mode MII; this pin is input pin M2RXD[3]. For RMII mode; this pin is not used. When under the above modes: DISPORTPRI[4] power on strapping is not supported. Port priority function can be set from the MII register.	1
DISPORTPRI[3]/ PHY2PTXD[2]/ M2RXD[2]	86	I (I_{PU})	-	When MII/RMII 2 is not enabled, this pin is strapping pin DISPORTPRI[3]. To enable port-based priority QoS function of port 3. Upon Reset: 1: Disable port3 priority 0: Enable port 3 priority After Reset: Not used. When MII/RMII 2 is enabled for PHY 4 or MAC 5. For PHY mode MII; this pin is input pin PHY2PTXD[2]. For MAC mode MII; this pin is input pin M2RXD[2]. For RMII mode; this pin is not used. When under the above modes, DISPORTPRI[3] power on strapping is not supported. Port priority function can be set from the MII register.	1
DISPORTPRI[2]/ PHY2PTXD[1]/ M(R)2RXD[1]	85	I (I_{PU})	-	When MII/RMII 2 is not enabled, this pin is strapping pin DISPORTPRI[2]. To enable port-based priority QoS function on port 2. Upon Reset: 1: Disable port 2 priority 0: Enable port 2 priority After Reset: Not used. When MII/RMII 2 is enabled for PHY 4 or MAC 5. For PHY mode MII, this pin is input pin PHY2PTXD[1]. For MAC mode MII, this pin is input pin M2RXD[1]. For RMII mode; this pin is input pin R2RXD[1]. When under the above modes, DISPORTPRI[2] power on strapping is not supported. Port priority function can be set from the MII register.	1

Pin Name	Pin No.	Type	Drive (mA)	Description	Default
DISPORTPRI[1]/ PHY2PTXD[0]/ M(R)2RXD[0]	84	I (I_{PU})	-	When MII/RMII 2 is not enabled, this pin is strapping pin DISPORTPRI[1]. To enable port-based priority QoS function on port 1. Upon Reset: 1: Disable port 1 priority 0: Enable port 1 priority After Reset: Not used. When MII/RMII 2 is enabled for PHY 4 or MAC 5. For PHY mode MII; this pin is input pin PHY2PTXD[0]. For MAC mode MII; this pin is input pin M2RXD[0]. For RMII mode; this pin is input pin R2RXD[0]. When under the above modes, DISPORTPRI[1] power on strapping is not supported. Port priority function can be set from the MII register.	1
DISPORTPRI[0]/ PHY2PTXEN/ M2RXDV/ CRSDV2	83	I (I_{PU})	-	When MII/RMII 2 is not enabled, this pin is strapping pin DISPORTPRI[0]. To enable port-based priority QoS function on port 0. Upon Reset: 1: Disable port 0 priority 0: Enable port 0 priority After Reset: Not used. When MII/RMII 2 is enabled for PHY 4 or MAC 5. For PHY mode MII; this pin is input pin PHY2PTXEN. For MAC mode MII; this pin is input pin M2RXDV. For RMII mode; this pin is input pin CRSDV2. When in the above modes, DISPORTPRI[0] power on strapping is not supported. Port priority function can be set from the MII register.	1
PHY2PCOL/ M2COL/ LED_BLNK_TIME	89	I/O (I_{PU})	4	When MII/RMII 2 is not enabled, this pin is strapping pin LED_BLINK_TIME only. To set the blinking speed of the activity and collision LEDs. Upon Reset: 1: On 43ms, then Off 43ms 0: On 120ms, then Off 120ms After Reset: Not used. When MII/RMII 2 is enabled for PHY 4 or MAC 5. For MAC mode MII, this pin is input pin M2COL. For PHY mode MII, this pin is IO pin PHY2COL/LED_BLNK_TIME. Upon Reset: This pin is strapping pin LED_BLINK_TIME. 1: On 43ms, then Off 43ms 0: On 120ms, then Off 120ms After Reset: This pin is output pin PHY2COL. For RMII mode it is strapping pin LED_BLINK_TIME. Upon Reset: 1: On 43ms, then Off 43ms 0: On 120ms, then Off 120ms After Reset: Not used.	1

Pin Name	Pin No.	Type	Drive (mA)	Description	Default
PHY2PTXC/ M2RXC/REFCLK2	82	I/O (I_{PU})	8	When MII/RMII 2 is enabled for PHY 4 or MAC 5. For MAC mode MII; the 2 pins are input pin M2RXC. For PHY mode MII; the 2 pins are output pin PHY2PTXC. For RMII mode, pin 82 is bi-directional pin REFCLK2, whose direction is controlled by pin 81. Pin 81Ctrl_REFCLK2 is a strapping pin to control the direction of Pin 82 in RMII mode. Upon Reset: If pin 81 is pulled-high, then pin 82 is an input pin to receive an external 50MHz RMIICLOCK. If pin 81 is pulled-low, then pin 82 is an output pin to provide a 50MHz RMIICLOCK.	1
PHY2PRXC/ M2TXC/ Ctrl_REFCLK2	81	I/O (I_{PU})	8		1
PHY2PRXD[3]/ M2TXD[3]/ ENBKPRS	78	I/O (I_{PU})	4	Input Upon Reset in All Modes. The pin is strapping pin ENBKPRS and sets backpressure in half duplex mode on all UTP ports. 1: Enable 0: Disable After Reset: When MII/RMII 2 is not enabled; this pin is not used. When MII/RMII 2 is enabled for PHY4 or MAC5. For MAC mode MII; this is output pin M2TXD[3]. For PHY mode MII; this is output pin PHY2PRXD[3]. For RMII mode: Not used.	1
PHY2PRXD[2]/ M2TXD[2]/ GYENFC	77	I/O (I_{PU})	4	Input Upon Reset in All Modes. The pin is strapping pin GYENFC. To enable Flow Control ability of GROUP Y: 1: Enable Reg4.10 (NWay Full duplex only), or 'Enable Force Full pause ability of Force Mode (UTP Force Mode)', or 'Enable Force Half Back Pressure ability of Force Mode (UTP Force Mode)'. 0: Disable Reg4.10 (NWay Full duplex only), or 'Disable Force Full pause ability of Force Mode (UTP Force Mode)', or 'Disable Force Half Back Pressure ability of Force Mode (UTP Force Mode)'. Strap after reset for initial value of Group Y 'UTP NWay Full', or 'UTP Force Full or Half Mode'. After Reset: When MII/RMII 2 is not enabled; this pin is not used. When MII/RMII 2 is enabled for PHY4 or MAC5. For MAC mode MII; this pin is output pin M2TXD[2]. For PHY mode MII; this pin is output pin PHY2PRXD[2]. For RMII mode: Not used.	1

Pin Name	Pin No.	Type	Drive (mA)	Description	Default
PHY2PRXD[1]/ M(R)2TXD[1]/ GXENFC	76	I/O (I_{PU})	4	Input Upon Reset in All Modes. The pin is strapping pin GYENFC. To enable Flow Control ability of GROUP Y: 1: Enable Reg4.10 (NWay Full duplex only), or 'Enable Force Full pause ability of Force Mode (UTP Force Mode)', or 'Enable Force Half Back Pressure ability of Force Mode (UTP Force Mode)'. 0: Disable Reg4.10 (NWay Full duplex only), or 'Disable Force Full pause ability of Force Mode (UTP Force Mode)', or 'Disable Force Half Back Pressure ability of Force Mode (UTP Force Mode)'.Strap after reset for initial value of Group X 'UTP NWay Full', or 'UTP Force Full or Half Mode'. After Reset: When MII/RMII 2 is not enabled; this pin is not used. When MII/RMII 2 is enabled for PHY4 or MAC5. For MAC mode MII, this pin is output pin M2TXD[1]. For PHY mode MII, this pin is output pin PHY2PRXD[1]. For RMII mode; this pin is output pin R2TXD[1].	1
PHY2PRXD[0]/ M(R)2TXD[0]/ ENEEPROM	73	I/O (I_{PU})	4	Input Upon Reset in All Modes. The pin is strapping pin Enable EEPROM. Sets the RTL8306G to enable loading of the serial EEPROM upon reset. 1: Enable 0: Disable Output After Reset: When MII/RMII 2 is not enabled; this pin is not used. When MII/RMII 2 is enabled for PHY4 or MAC5. For MAC mode MII; this is output pin M2TXD[0]. For PHY mode MII; this is output pin PHY2PRXD[1]. For RMII mode; this is output pin R2TXD[1].	1
PHY2PRXDV/ M(R)2TXEN/ DISBRDCTRL	80	I/O (I_{PU})	4	Input Upon Reset in All Modes. The pin is strapping pin DISBRDCTRL. Sets Broadcast Storm Control. 1: Disable 0: Enable Output After Reset: When MII/RMII 2 is not enabled; this pin is strapping pin only. When MII/RMII 2 is enabled for PHY4 or MAC5. For MAC mode MII; this pin is output pin M2TXEN. For PHY mode MII; this pin is output pin PHY2PRXDV. For RMII mode; this pin is output pin R2TXEN.	1

6.5. Miscellaneous Pins

Table 6. Miscellaneous Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
X1	120	I	-	25MHz Crystal Input. The clock tolerance is ±50ppm. When using an oscillator, this pin should be tied to ground.
X2	121	O	-	For Crystal Input. When using an oscillator, this pin should be left floating.
OSCI	117	I	-	A 25MHz Clock from an Oscillator is Fed to This Pin. X1 should be tied to ground and X2 should be left floating in this application. If the 25MHz clock is from a crystal via X1 and X2, this pin should be left floating.
CK25MOUT	116	O	8	25MHz Clock Output. This pin is used to support an extra 25M clock for an external device (for example: HomePNA PHY). *Note: The default status of the 25MHz clock output is disabled. It can be enabled through a register setting.*
RESET#	40	I	-	Active Low Reset Signal. To complete the reset function, this pin must be asserted for at least 1ms. After reset, about 30ms is needed for the RTL8306G to complete internal test functions and initialization. This pin is a Schmitt input.
IBREF	127	A	-	Control Transmit Output Waveform Vpp. This pin should be grounded through a 1.96K ohm resistor.
VCTRL	123	O	4	Voltage Control to External Regulator. This signal controls a power PNP transistor to generate the 1.8V power supply.
ITEST1	36	-	-	Reserved Pin for Internal Use. Should be left floating.
ITEST2	37	-	-	Reserved Pin for Internal Use. Should be left floating.
ITEST3	38	-	-	Reserved Pin for Internal Use. Should be left floating.
ITEST4	41	-	-	Reserved Pin for Internal Use. Should be left floating.
ITEST5	65	-	-	Reserved Pin for Internal Use. Should be left floating.
ITEST6	72	-	-	Reserved Pin for Internal Use. Should be left floating.
DTEST2	124	-	-	Reserved Pin for Internal Use. Should be left floating.
DTEST1	125	-	-	Reserved Pin for Internal Use. Should be left floating.

6.6. Port LED Pins

Each port has four LED indicator pins. Each pin may have different indicator meanings as set by pins LEDMODE[1:0].

All LED statuses are represented as active-low or high depending on input strapping, except Bi-color Link/Act in Bi-color LED mode, whose polarity depends on Spd status.

Those pins that are dual-function pins are output for LED or input for strapping. Below are LED descriptions only.

Table 7. Port LED Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
LED_DUP[4:0]/…	95, 99, 105, 110, 115	I/O_{PU}	4	Output After Reset = Used for Group A LED. RTL8306G controlling LED: LEDMode[1:0]=11 → Duplex/Col: (On=Full, Off=Half with no collision, Flash=Collision) LEDMode[1:0]=10 → Duplex/Col: (On=Full, Off=Half with no collision, Flash=Collision) LEDMode[1:0]=01 → TxAct: (Off=No activity, Flash=Tx activity) LEDMode[1:0]=00 → Duplex:(On=Full duplex, Off=Half Duplex) CPU Controlling LED: On: Corresponding register 1 Off: Corresponding register 0 Input Upon Reset = Refer to Table 9, on page 22, and Table 10, on page 24.
LED_SPD[4:0]/…	93, 98, 104, 109, 114	I/O_{PU}	4	Output After Reset = Used for Group B LEDs. RTL8306G controlling LED: LEDMode[1:0]=11 → Speed (On=100, Off=10) LEDMode[1:0]=10 → Speed (On=100, Off=10) LEDMode[1:0]=01 → Speed (On=100, Off=10) LEDMode[1:0]=00 → Speed (0n=100, Off=10) CPU Controlled LED. For Single-color LED: On: Corresponding register 1 Off: Corresponding register 0 For Bi-color LED: Displays also depend on pin LED_ADD status. Input Upon Reset = Refer to Table 9, on page 22, and Table 10, on page 24.
LED_ACT[4:0]/…	92, 97, 103, 108, 113	I/O_{PU}	4	Output After Reset = Used for Group C LEDs. RTL8306G controlling LED: LEDMode[1:0]=11 → Link/Act: (On=Link, Off=No Link, Flash=Tx or Rx activity) LEDMode[1:0]=10 → Act: (Off=No activity, Flash=Tx or Rx activity) LEDMode[1:0]=01 → RxAct: (Off=No activity, Flash=Rx activity) LEDMode[1:0]=00 → Col:(On=Collision, Off=No Collision) CPU Controlled LED. On: Corresponding register 1 Off: Corresponding register 0 Input Upon Reset = Refer to Table 9, on page 22, and Table 10, on page 24.

Pin Name	Pin No.	Type	Drive (mA)	Description
LED_ADD[4:0]/...	91, 96, 101, 107, 111	I/O_{PU}	4	Output After Reset = Used for Group D LEDs. RTL8306G controlling LED: LEDMode[1:0]=11 → Link/Act/Spd: On for link established. Blinking every 43ms when the corresponding port is transmitting or receiving at 100Mbps. Blinking every 120ms when the port is transmitting or receiving at 10Mbps. LEDMode[1:0]=10 → Bi-color Link/Active: polarity depends on Spd status. LEDMode[1:0]=01 → Link: (On=Link, Off=No Link) LEDMode[1:0]=00 → Bi-color Link/Active: polarity depends on Spd status. CPU Controlled LED. For Single-color LED, On: Corresponding register 1 Off: Corresponding register 0 For Bi-color LED, displays also depend on pin LED_SPD status. Input Upon Reset = Refer to Table 9, on page 22, and Table 10, on page 24.
LOOPLED#/ ENDEFER	90	I/O_{PU}	4	Output After Reset = LoopLED# used for LED. If the Loop detection function is enabled, this pin indicates whether a Network loop is detected or not. Otherwise, this pin is of no use. The LED statuses are represented as active-low or high depending on input strapping. If Input=1: Output Low active, 0: LED on. Network loop is detected. 1: LED off. No loop. If Input=0: Output High active, 1: LED on. Network loop is detected. 0: LED off. No loop. Input Upon Reset = Enable defer 1: Enable Carrier Sense Deferring function for half duplex back pressure 0: Disable Carrier Sense Deferring function for half duplex back pressure

6.7. Serial EEPROM and SMI Pins

As the output of the RTL8306G is 3.3V, the serial EEPROM and external device must be 3.3V compatible.

Table 8. Serial EEPROM and SMI Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
SCL_MDC	74	I/O (I_{PU})	4	SCL or MDC. This pin is tri state when pin RESET#=0. When pin EnEEPROM=1, this pin becomes SCL (output) to load the serial EEPROM upon reset. After reset this pin changes to MDC (input). When pin EnEEPROM=0, this pin is MDC (input): 0 to 2.5MHz clock, sourced by an external device to sample MDIO.
SDA_MDIO	75	I/O (I_{PU})	4	SDA or MDIO. This pin is tri state when RESET#=0. When pin EnEEPROM=1, this pin becomes SDA (input/output) to load the serial EEPROM upon reset. After reset this pin changes to MDIO (input/output). It should be pulled-high by an external resistor. When pin EnEEPROM=0, this pin is MDIO (input/output). It should be pulled-high by an external resistor.

6.8. Strapping Pins

Pins that are dual function pins are outputs for LED or inputs for strapping. Below are strapping descriptions only.

Table 9. Strapping Pins

Pin Name	Pin No.	Type	Drive (mA)	Description	SMI Accessible	EEPROM Accessible
EN_AUTOXOVER	69	I (I_{PU})	-	Enable Auto Crossover Function. 1: Enable auto crossover detection 0: Disable auto crossover detection. MDI only	√	√
EN_RST_BLNK	71	I (I_{PU})	-	Enable Reset Blink. This enables blinking of the LEDs upon reset for diagnostic purposes. 1: Enable reset LED blinking 0: Disable reset LED blinking	√	√
LED_ADD[4]/ DISTAGPRI	91	I/O (I_{PU})	4	Input Upon Reset = Disable 802.1p VLAN Tag priority based QoS function. 1: Disable 0: Enable Output After Reset = Used for LED.	√	√
LED_ACT[4]/ DISHOMEPLUG	92	I/O (I_{PU})	4	Input Upon Reset =DISHOMEPLUG. 1: Disable HOMEPLUG. Use input RXDV as CRS of Port4MII 0: Enable HOMEPLUG. Use input pin 48 P4FULL as CRS of Port4MII Output After Reset = Used for LED.	√	√

Pin Name	Pin No.	Type	Drive (mA)	Description	SMI Accessible	EEPROM Accessible
LED_SPD[4]/ DISVLAN	93	I/O (I_{PU})	4	Input Upon Reset = Disable VLAN function. 1: Disable VLAN 0: Enable VLAN. The default VLAN membership configuration by internal register is port 4 overlapped with all the other ports, to form 4 individual VLANs. This default membership configuration may be modified by internal registers via the SMI interface or EEPROM Output After Reset = Used for LED.	√	√
LED_ACT[3]/ EN48PASS1	97	I/O (I_{PU})	4	Input Upon Reset = Enable 48 pass 1. 1: 48 pass 1. Continuously collides 48 input packets then passes 1 packet to retain system resources and avoid partition in the repeater when the packet buffer is full 0: Continuously collides to avoid packet loss when the packet buffer is full Output After Reset = Used for LED.	√	√
LED_SPD[3]/ DISARP	98	I/O (I_{PU})	4	Input Upon Reset = Disable ARP broadcast to all VLANs. 1: Disables ability to broadcast ARP broadcast packets to all VLANs 0: Enables ability to broadcast ARP broadcast packets to all VLANs ARP broadcast frame: DID is all F. Output After Reset = Used for LED.	√	√
LED_ADD[2]/ DISLEAKY	101	I/O (I_{PU})	4	Input Upon Reset = Disable Leaky VLAN. 1: Disable forwarding of unicast frames to other VLANs 0: Enable forwarding of unicast frames to other VLANs Broadcast and multicast frames adhere to the VLAN configuration. Output After Reset = Used for LED.	√	√
LED_ADD[0]/ ENFORWARD	111	I/O (I_{PU})	4	Input Upon Reset = Enable to forward 802.1D specified reserved multicast addresses frame. 1: Forward reserved control frames, with DID=01-80-C2-00-00-04 to 01-80-C2-00-00-0F 0: Filter reserved control packets, with DID=01-80-C2-00-00-04 to 01-80-C2-00-00-0F Output After Reset = Used for LED.	√	√
LED_ACT[0]/ BCINDROP	113	I/O (I_{PU})	4	Input Upon Reset = Broadcast Input Drop. 1: Use Broadcast Input drop mechanism 0: Use Broadcast Output drop mechanism Output After Reset = Used for LED.	√	√
LED_SPD[0]/ MAX1536	114	I/O (I_{PU})	4	Input Upon Reset = Maximum Frame Length. 1: 1536 Bytes 0: 1552 Bytes Output After Reset = Used for LED.	√	√
LED_DUP[0]	115	I/O (I_{PU})	4	Input Upon Reset. 1: Port 0 in UTP mode 0: Reserved Output After Reset = Used for LED.	N/A	N/A

6.9. Port Status Strapping Pins

Pins that are dual function pins are outputs for LEDs or inputs for strapping. Below are strapping descriptions only.

Table 10. Port Status Strapping Pins

Pin Name	Pin No.	Type	Drive (mA)	Description	SMI Accessible	EEPROM Accessible
LED_DUP[4]/ SETGROUP	95	I/O_{PU}	4	Input Upon Reset = Set group of port 1. 1: Port 0 is group X. Port 1, 2, and 3 are group Y 0: Port 0, and 1 are group X. Port 2, and 3 are group Y Output After Reset = Used for LED.	N/A	N/A
LED_ADD[3]/ Modeset1	96	I/O_{PU}	4	Input Upon Reset = Modeset1. See Table 3, page 9, for details. Output After Reset = Used for LED.	N/A	N/A
LED_DUP[3]/ Modeset0	99	I/O_{PU}	4	Input Upon Reset = Modeset0. Output After Reset = Used for LED.	N/A	N/A
LED_ACT[2]/ P4ANEG	103	I/O_{PU}	4	Input Upon Reset = Port 4 Auto-Negotiation ability. 1: Enable auto-negotiation (NWay mode) 0: Disable auto-negotiation (Force mode) Upon reset, this pin sets Reg.0.12 of Port 4. Strap after reset for initial value of Port 4 UTP mode only. This pin is not used for MAC mode MII, PHY mode MII. Output After Reset = Used for LED.	√	√
LED_SPD[2]/ GXANEG	104	I/O_{PU}	4	Input Upon Reset = GroupX Auto-Negotiation ability. 1: Enable auto-negotiation (NWay mode) 0: Disable auto-negotiation (Force mode) Upon reset, this pin sets Reg.0.12 of Group X. Strap after reset for initial value of UTP mode only. Output After Reset = Used for LED.	√	√
LED_DUP[2]/ GYANEG	105	I/O_{PU}	4	Input Upon Reset = GroupY Auto-Negotiation ability. 1: Enable auto-negotiation (NWay mode) 0: Disable auto-negotiation (Force mode) Upon reset, this pin sets Reg.0.12 of Group Y. Strap after reset for initial value of UTP mode only. Output After Reset = Used for LED.	√	√
LED_ADD[1]/ GXSPD100	107	I/O_{PU}	4	Input Upon Reset = GroupX 10Base-T/100Base-TX ability. GxSpd100: 1, GxFull=1 => MII Reg0.13=1, 0.8=1, 4.8=1, 4.7=1, 4.6=1, 4.5=1 GxSpd100: 1, GxFull=0 => MII Reg0.13=1, 0.8=0, 4.8=0, 4.7=1, 4.6=1, 4.5=1 GxSpd100: 0, GxFull=1; => MII Reg0.13=0, 0.8=1, 4.8=0, 4.7=0, 4.6=1, 4.5=1 GxSpd100: 0, GxFull=0; => MII Reg0.13=0, 0.8=0, 4.8=0, 4.7=0, 4.6=0, 4.5=1 Upon reset, this pin sets Reg.0.13. In addition, upon reset, this pin and GxFull also sets Reg.4.8/4.7/4.6/4.5. Strap after reset for initial value of Group X UTP mode only. Output After Reset = Used for LED.	√	√

Pin Name	Pin No.	Type	Drive (mA)	Description	SMI Accessible	EEPROM Accessible
LED_ACT[1]/ GYSPD100	108	I/O_{PU}	4	Input Upon Reset = GroupY 10Base-T/100Base-TX ability. GySpd100: 1, GyFull=1 => MII Reg0.13=1, 0.8=1, 4.8=1, 4.7=1, 4.6=1, 4.5=1 GySpd100: 1, GyFull=0 => MII Reg0.13=1, 0.8=0, 4.8=0, 4.7=1, 4.6=1, 4.5=1 GySpd100: 0, GyFull=1 => MII Reg0.13=0, 0.8=1, 4.8=0, 4.7=0, 4.6=1, 4.5=1 GySpd100: 0, GyFull=0 => MII Reg0.13=0, 0.8=0, 4.8=0, 4.7=0, 4.6=0, 4.5=1 Upon reset, this pin sets Reg.0.13. In addition, upon reset, this pin and GyFull also sets Reg.4.8/4.7/4.6/4.5. Strap after reset for initial value of Group Y UTP mode only. Output After Reset = Used for LED.	√	√
LED_SPD[1]/ GXFULL	109	I/O_{PU}	4	Input Upon Reset = GroupX Full Duplex ability. Upon reset, this pin sets the default value of Reg.0.8. In addition, on reset, this pin also sets NWay full-duplex ability on Reg.4.8 and Reg.4.6. Strap after reset for initial value of Group X UTP mode. Output After Reset = Used for LED.	√	√
LED_DUP[1]/ GYFULL	110	I/O_{PU}	4	Input Upon Reset = GroupY Full Duplex ability. Upon reset, this pin sets the default value of Reg.0.8. On reset, this pin also sets NWay full-duplex ability on Reg.4.8 and Reg.4.6. Strap after reset for initial value of Group Y UTP mode. Output After Reset = Used for LED.	√	√

6.10. Power Pins

Table 11. Power Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
AVDD18	1, 7, 8, 14, 15, 21, 22, 28, 29, 35, 119, 128	P	-	1.8V Analog Power.
HVDD33	118	P	-	3.3V Analog Power.
AGND	4, 11, 18, 25, 32, 122, 126	P	-	Analog Ground.
DVDD18	43, 53, 70, 100	P	-	1.8V Digital Power.
DVDD33	62, 87, 106	P	-	3.3V Digital Power.
DGND	39, 50, 64, 79, 94, 102, 112	P	-	Digital Ground.

7. Basic Functional Description

7.1. Switch Core Function Overview

7.1.1. Dual MII/RMII

7.1.1.1 Description

The RTL8306G supports two MII/RMII interfaces to work with various routing engines, and one MII/RMII interface to work with HomePNA, HomePlug, or VDSL transceivers, as shown in Figure 3, page 26.

The RTL8306G support a Dual MII/RMII interface for external devices to connect to the 6th MAC, 5th MAC, and 5th PHY. The external device could be a routing engine, HomePNA, HomePlug, or VDSL transceiver depending on the application.

The 5th PHY also supports external MII or RMII interface pins for connection to an external MAC.

Note: 'MII/RMII 1' signal pins are used only by MAC4. The 'MII/RMII 2' signal pins are used by PHY4 or MAC5.

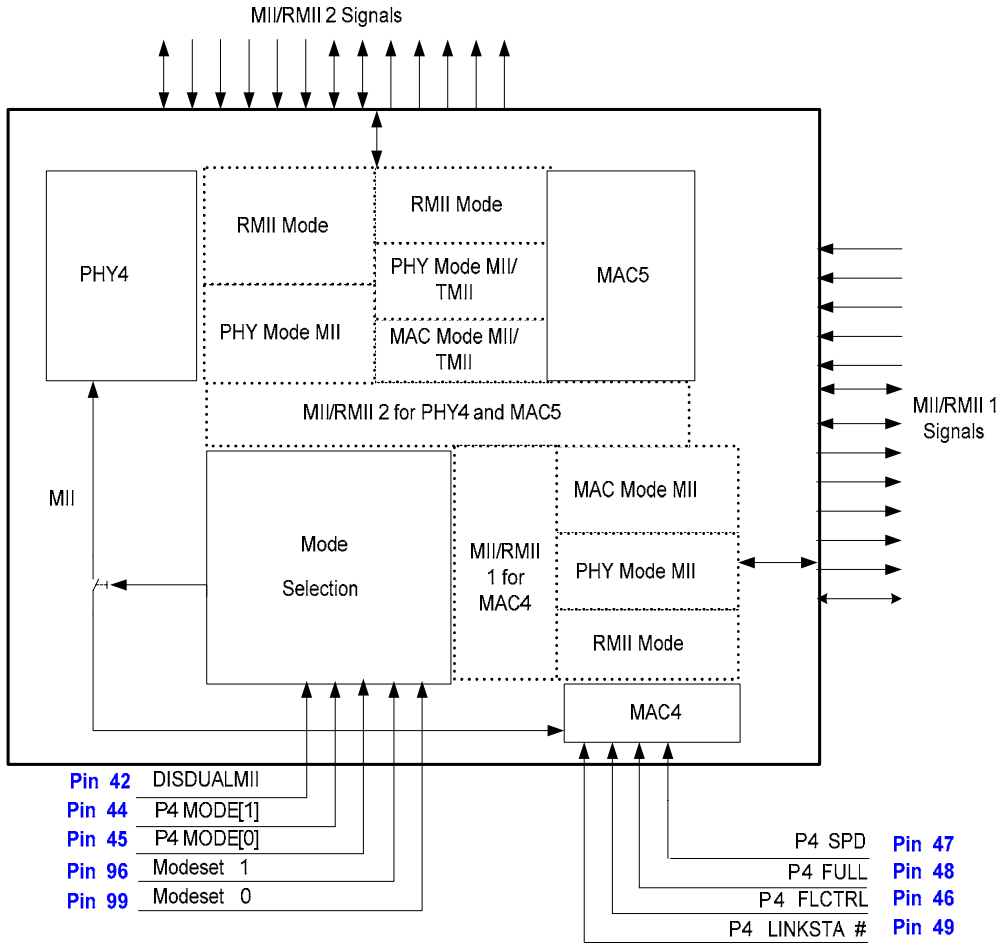


Figure 3. DUAL MII/RMII Diagram

7.1.1.2 Dual MII/RMII Mode Configuration

Dual MII/RMII interfaces of the RTL8306G support various operating modes. Table 12 lists the available modes.

'1' indicates that upon reset this pin is pull-high. '0' indicates that upon reset this pin is pull-down. 'X' indicates not supported.

Table 12. DUALMII/RMII Mode Configuration Table

Pin 42	Pin 44	Pin 45	Pin 96	Pin 99	Operating Mode
DIS DUALMII Default: 1	P4 MODE1 Default: 1	P4 MODE0 Default: 1	Modeset1 Default: 1	Modeset0 Default: 1	
1	1	1	X	X	Port 4 is UTP or MAC4 in MAC Mode MI. MII/RMII2 not used. See Note 1.
1	1	0	X	X	Reserved.
1	0	1	X	X	MAC4 in PHY Mode MII MII/RMII2 not used.
0	0	1	X	X	MAC4 in PHY Mode MII, and PHY4 in PHY Mode MII. See Note 2.
0	1	1	X	X	MAC4 in MAC Mode MII, and PHY4 in PHY Mode MII. See Note 2.
1	0	0	1	1	MAC4 in RMII. MII/RMII 2 not used.
0	0	0	1	1	MAC4 in RMII, and PHY4 in RMII (UTP) See Note 2.
0	0	0	1	0	MAC5 in PHY Mode MII, and MAC4 in PHY Mode MII.
0	0	0	0	1	MAC5 in PHY Mode MII, and MAC4 in RMII.
0	0	0	0	0	MAC5 in RMII, and MAC4 in RMII.
0	1	0	1	1	Port 4 UTP/MAC4 in MAC Mode MII, and MAC5in MAC Mode MII. See Note 3.
0	1	0	0	1	Port 4 UTP/MAC 4 MAC Mode MII; And MAC 5 in PHY Mode MII. See Note 3.
0	1	0	0	0	Port 4 UTP/MAC 4 MAC Mode MII And MAC5 in RMII Mode. See Note 3.

Note 1: When in this mode, if port 4 is connected with UTP, then the operating mode is Port 4UTP; If port 4 is not connected with UTP and P4LINKSTA# tied to ground, then the operating mode is MAC 4 in MAC mode MII.

Note 2: When in these modes, PHY 4 MII is enabled and Pin 68 is used to select the operating mode of the port 4 differential pair: upon reset pin 68 is pulled-high and PHY 4 can be connected with UTP.

Note 3: When in this configuration, 3 modes can be further distinguished by the following rules:

1). If port 4 is connected with UTP, and Pin 68 is pulled-high (default: pulled-high) upon reset, then port 4 is a UTP port.

2). If MAC4 in MAC mode is needed, Pin P4LINKSTA# should be tied to ground and port 4 should not be connected with UTP.

7.1.1.3 Port4 (5th Port) and Port5 (6th MAC) Status Configuration

The RTL8306G supports flexible methods to configure Port4 (5th Port) and MAC5 (6th MAC) NWay/Force mode, 10Mbps/100Mbps, Full/Half duplex, and Enable/Disable Flow control.

- When MAC4 (5th MAC) is in MAC mode MII, PHY mode MII, or RMII mode, these operating abilities can be configured by strapping pins (P4ANEG, P4SPD, P4DUP, and P4FLCTRL) upon reset according to application.
- When MAC5 (6th MAC) is needed in system applications, the operating abilities should be configured by writing the register after setting the correct DUALMII/RMII operating mode.
- When MAC5 is enabled, the default status is: Not linked, 100Mbps, Full duplex, flow control enabled.

7.1.2. Port0, 1, 2, 3 Status Configuration

The 4 ports are separated into 2 groups (GroupX/GroupY) for flexible port configuration using strapping pins upon reset. The SetGroup pin is used to select the port numbers for GroupX and GroupY.

- SetGroup=1: GroupX = Port0; GroupY = Ports 1, 2, and 3.
- SetGroup=0: GroupX = Ports 0 and 1; GroupY = Ports 2 and 3).

Each group has four pins for selecting initial port status upon reset (ANEG/Force, 100/10, Full/Half, Enable/Disable Flow Control). Upon reset, in addition to using strapping pins, the RTL8306G can be configured via an EEPROM, or read/write operation by a CPU via the MDC/MDIO interface.

7.1.3. Flow Control

The RTL8306G supports IEEE 802.3x full duplex flow control, force mode full duplex flow control, and optional half duplex back pressure.

7.1.3.1 IEEE 802.3x Full Duplex Flow Control

For UTP with auto-negotiation ability (GxANeg/GyANeg/P4Aneg set to 1), the pause ability (Reg.4.10) of full duplex flow control is enabled by pins GxEnFC/GyEnFC/P4EnFC on a group basis upon reset, or internal registers via SMI on a per-port basis after reset. For UTP with auto-negotiation ability, IEEE 802.3x flow control's ability is auto-negotiated between the remote device and the RTL8306G. If the auto-negotiation result of the IEEE 802.3x pause ability is 'Enabled' (Reg.4.10: 1 and Reg.5.10: 1), the full duplex 802.3x flow control function is enabled. Otherwise, the full duplex IEEE 802.3x flow control function is disabled.

7.1.3.2 Force Mode Full Duplex Flow Control

For UTP without auto-negotiation ability (GxANeg/GyANeg/P4Aneg is 0), IEEE 802.3x flow control's ability can be set to 'Enabled' by pins GxEnFC/GyEnFC/P4EnFC on a group basis upon reset, or by internal registers (Reg.5.10) via SMI on a per-port basis after reset. For example:

- Port 4 will be forced to '10Full UTP with forced mode full duplex flow control' ability, regardless of the connected device, when P4Mode[1:0]=10, P4Aneg=0, P4Spd100=0, P4Full=1, P4EnFC=1.
- Port 0 will be forced to 'forced mode full duplex flow control' ability, regardless of the connected device, when SetGroup=1, GxFull=1, GxEnFC=1.

Regardless of the flow control mode (IEEE 802.3x full duplex flow control, or forced mode full duplex flow control), when full duplex flow control is enabled, the RTL8306G will only recognize IEEE 802.3x flow control PAUSE ON/OFF frames with DA=01-80-C2-00-00-01, type=0x8808, OP-code=0x01, PAUSE Time = maximum to zero, and with a good CRC.

If a PAUSE frame is received from any PAUSE flow control enabled port set to DA=01-80-C2-00-00-01, the corresponding port of the RTL8306G will stop its packet transmission until the PAUSE timer times out or another PAUSE frame with zero PAUSE time is received. The RTL8306G will not forward any IEEE 802.3x PAUSE frames received from any port.

7.1.3.3 Half Duplex Back Pressure

If pin EnDefer is 1, the RTL8306G will send a preamble to defer the other station's transmission when there is no packet to send. Otherwise, if pin EnDefer is 0, the RTL8306G will force a collision with the other station's transmission when the buffer is full.

- If pin 48pass1 is 0, the RTL8306G will always collide with JAM (Continuous collision).
- If pin 48pass1 is 1, the RTL8306G will try to forward one packet successfully after 48 forced collisions (48pass1), to avoid the connected repeater being partitioned due to excessive collisions.

7.1.3.4 NWay Mode

For UTP with auto-negotiation ability, pins GxEnFC/GyEnFC/P4EnFC are effective only in full duplex mode. Therefore, for UTP in half duplex mode, half duplex back pressure flow control is controlled by the ENBKPRS pin strap upon hardware reset.

7.1.3.5 Force Mode

For UTP without auto-negotiation ability, the operation mode can be forced to half duplex. Half duplex back pressure flow control can be forced to 'enabled' on the RTL8306G side by pin GxEnFC/GyEnFC/P4EnFC on a group basis upon reset.

7.1.4. Address Search, Learning, and Aging

When a packet is received, the RTL8306G will use the bits of the destination MAC address to index the 2048-entry lookup table, and at the same time compare the destination MAC address with the contents of the 16-entry CAM. If the indexed entry is valid, or the CAM comparison is matched, the received packet will be forwarded to the corresponding destination port. Otherwise, the RTL8306G will broadcast the packet. This is the 'Address Search'.

The RTL8306G then extracts the specific bits of the source MAC address to index the 2048-entry lookup table. If the entry is not in the table it will record the source MAC address and add switching information. If this is an occupied entry, it will update the entry with new information. This is called 'Learning'. If the indexed location has been occupied by a different MAC address (hash collision), the new source MAC address will be recorded into the 16-entry CAM. The 16-entry CAM reduces address hash collisions and improves switching performance.

Address aging is used to keep the contents of the address table correct in a dynamic network topology. The lookup engine will update the time stamp information of an entry whenever the corresponding source MAC address appears. An entry will be invalid (aged-out) if its time stamp information is not refreshed by the address learning process during the aging time period. The aging time of the RTL8306G is between 200 and 350 seconds.

7.1.5. Half Duplex Operation

In half duplex mode, the CSMA/CD media access method is the means by which two or more stations share a common transmission medium. To transmit, a station waits (defers) for a quiet period on the medium (that is, no other station is transmitting) and then sends the intended message in bit-serial form. If the message collides with that of another station, then each transmitting station intentionally transmits for an additional predefined period to ensure propagation of the collision throughout the system. The station remains silent for a random amount of time (backoff) before attempting to transmit again.

When a transmission attempt has terminated due to a collision, it is retried until it is successful. A controlled randomization process called 'truncated binary exponential backoff' determines the scheduling of the retransmissions. At the end of enforcing a collision (jamming), the switch delays before attempting to retransmit the frame. The delay is an integer multiple of slotTime (512 bit times). The number of slot times to delay before the n^{th} retransmission attempt is chosen as a uniformly distributed random integer 'r' in the range:

$0 \leq r < 2^k$

where:

k = min (n, backoffLimit). IEEE 802.3 defines the backoffLimit as 10.

7.1.6. InterFrame Gap

The InterFrame Gap is 9.6μs for 10Mbps Ethernet and 960ns for 100Mbps Fast Ethernet.

7.1.7. Illegal Frame

Illegal frames such as CRC error packets, runt packets (length < 64 bytes), and oversize packets (length > maximum length), will be discarded.

7.2. Physical Layer Functional Overview

7.2.1. Auto-Negotiation for UTP

The RTL8306G obtains the states of duplex, speed, and flow control ability for each port in UTP mode through the auto-negotiation mechanism defined in the IEEE 802.3u specifications. During auto-negotiation, each port advertises its ability to its link partner and compares its ability with advertisements received from its link partner. By default, the RTL8306G advertises full capabilities (100Full, 100Half, 10Full, 10Half) together with flow control ability.

7.2.2. 10Base-T Transmit Function

The output 10Base-T waveform is Manchester-encoded before it is driven onto the network media. The internal filter shapes the driven signals to reduce EMI emissions, eliminating the need for an external filter.

7.2.3. 10Base-T Receive Function

The Manchester decoder converts the incoming serial stream to NRZ data when the squelch circuit detects the signal level is above squelch level.

7.2.4. Link Monitor

The 10Base-T link pulse detection circuit continually monitors the RXIP/RXIN pins for the presence of valid link pulses. Auto-polarity is implemented to correct the detected reverse polarity of RXIP/RXIN signal pairs.

7.2.5. 100Base-TX Transmit Function

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ/NRZI conversion, and MLT-3 encoding. The 5-bit serial data stream after 4B/5B coding is then scrambled as defined by the TP-PMD Stream Cipher function to flatten the power spectrum energy such that EMI effects are significantly reduced.

The scrambled seed is based on PHY addresses and is unique for each port. After scrambling, the bit stream is driven into the network media in the form of MLT-3 signaling. The MLT-3 multi-level signaling technology moves the power spectrum energy from high frequency to low frequency, which further reduces EMI emissions.

7.2.6. 100Base-TX Receive Function

The receive path includes a receiver composed of an adaptive equalizer and DC restoration circuits (to compensate for an incoming distorted MLT-3 signal), an MLT-3 to NRZI and NRZI to NRZ converter to convert analog signals to digital bit-stream, and a PLL circuit to clock data bits with minimum bit error rate. A De-scrambler, 5B/4B decoder, and serial-to-parallel conversion circuits are followed by the PLL circuit. Finally, the converted parallel data is fed into the MAC.

7.2.7. Power-Down Mode

The RTL8306G implements power-down mode on a per-port basis. Setting MII Reg.0.11 forces the corresponding port of the RTL8306G to enter power-down mode. This disables all transmit/receive functions, except SMI (Serial Management Interface: MDC/MDIO, also known as MII Management Interface).

7.2.8. Crossover Detection and Auto Correction

During the link setup phase, the RTL8306G checks whether it receives active signals on every port in order to determine if a connection can be established. In cases where the receiver data pin pair is connected to the transmitter data pin pair of the peer device and vice versa, the RTL8306G automatically changes its configuration and swaps receiver/transmitter data pins as required. If a port is connected to a PC or NIC with MDI-X interface with a crossover cable, the RTL8306G will reconfigure the port to ensure proper connection. This replaces the DIP switch commonly used for reconfiguring a port on a hub or switch.

By pulling-up EN_AUTOXOVER, the RTL8306G identifies the type of connected cable and sets the port to MDI or MDIX:

- When switching to MDI mode, the RTL8306G uses TXOP/N as transmit pairs.
- When switching to MDIX mode, the RTL8306G uses RXIP/N as transmit pairs.

This function is port-based. Pulling-down EN_AUTOXOVER disables this function and the RTL8306G operates in MDI mode, in which TXOP/N represents transmit pairs, and RXIP/N represents receive pairs.

Note: IEEE 802.3 compliant forced mode 100M ports with Autoxover have link problems with NWay (Auto-Negotiation) ports. It is recommended to not use Autoxover for forced 100M.

7.2.9. Polarity Detection and Correction

For better noise immunity and lower interference to ambient devices, the Ethernet electrical signal on a twisted-pair cable is transmitted in differential form. That is, the signal is transmitted on two wires in each direction with inverse polarities (+/-). If wiring on the connector is faulty, or a faulty transformer is used, the two inputs to a transceiver may carry signals with opposite but incorrect polarities. As a direct consequence, the transceiver will not work properly.

When the RTL8306G operates in 10Base-T mode, it automatically reverses the polarity of its two receiver input pins if it detects that the polarities of the incoming signals on the pins is incorrect. However, this feature is unnecessary when the RTL8306G is operating in 100Base-TX mode.

7.3. General Function Overview

7.3.1. Reset

Depending on the type of reset, the whole or just part of the RTL8306G is initialized. There are several ways to reset the RTL8306G:

- Hardware reset for the whole chip by pin RESET#
- Soft reset for all except PHY by register SoftReset
- PHY software reset for each PHY by register reset

Hardware Reset: Pull low Pin RESET# for at least 10ms. The RTL8306G resets the whole chip and then gets initial values from pins and serial EEPROM.

Soft Reset: The RTL8306G does not reset the PHY, and does not load EEPROM and Pin Registers with serial EEPROM and Pins. After changing the queue number via SMI (Serial Management Interface), the external device must perform a soft reset in order to update the configuration.

PHY Software Reset: Write bit15 of Reg0 of a PHY as 1. The RTL8306G will then reset this PHY.

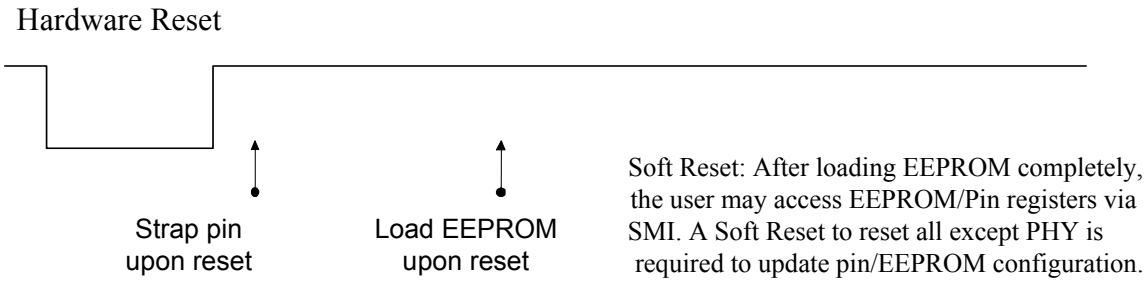


Figure 4. Reset

Some setting values for operation modes are latched from those corresponding mode pins upon hardware reset. 'Upon reset' is defined as a short time after the end of a hardware reset. Other advanced configuration parameters may be latched from serial EEPROM if pin EnEEPROM=1.

7.3.2. Setup and Configuration

The RTL8306G can be configured easily and flexibly by hardware pins upon reset, optional serial EEPROM upon reset (Please contact Realtek to get the detailed EEPROM configuration settings), and internal registers (including PHY registers for each port and global MAC registers) via SMI (Serial Management Interface: MDC/MDIO, also known as MII Management Interface). There are three methods of configuration:

- Only hardware pins for normal switch applications
- Hardware pins and serial EEPROM for advanced switch applications
- Hardware pins and internal registers via SMI for applications with processor

Three types of pins, each with internal pull-high resistors, are used for configuration:

- Input pins used for strapping upon reset (unused after reset)
- Input/Output pins (MTXD[3:2]/PRXD[3:2]/P4IRTag[1:0], MTXD[1:0]/PRXD[1:0]/LEDMode[1:0]) used for strapping upon reset and used as output pins after reset
- Input/Output pins (all LEDs) used for strapping upon reset and used as LED indicator pins after reset. The LED statuses are represented as active-low or high depending on input strapping, except Bi-color Link/Act in Bi-color LED mode, whose polarity depends on Spd status

Pins with default value=1 are internal pull-high and use I/O pads. They can be left floating to set the input value as high, but should not be connected to GND without a pull-down resistor.

The serial EEPROM shares two pins, SCL_MDC and SDA_MDIO, with SMI, and is optional for advanced configuration. SCL_MDC and SDA_MDIO are tri-state during hardware reset (pin RESET#=0). The RTL8306G will try to automatically find the serial EEPROM upon reset only if pin EnEEPROM=1. If the first byte of the serial EEPROM is not 0xFF (NoEEPROM bit of the first byte=0), the RTL8306G will load all contents of the serial EEPROM into internal registers. Otherwise, the RTL8306G will use the default internal values.

Internal registers can still be accessed after reset via SMI (pin SCL_MDC and SDA_MDIO). Serial EEPROM signals and SMI signals must not exist at the same time. In order to use the SMI to flexibly change configuration, internal registers include the contents of some pins and all serial EEPROM. These registers do not work in real time, and a Soft Reset is necessary after changing the EEPROM or pin registers.

7.3.3. Serial EEPROM Example: 24LC01/02/04

The 24LC01/02/04 interface is a 2-wire serial EEPROM interface providing 1K/2K/4K bits of storage space. The 24LC01/02/04 must be 3.3V compatible.

7.3.3.1 24LC02/04 Device Operation

Clock and Data Transitions: The SDA pin is normally pulled high with an external resistor. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a start or stop condition as defined below.

Start Condition

A high-to-low transition of SDA with SCL high is the start condition and must precede any other command.

Stop Condition

A low-to-high transition of SDA with SCL high is a stop condition.

Acknowledge

All addresses and data are transmitted serially to and from the EEPROM in 8-bit words. The 24LC01/02/04 sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

Random Read

A random read requires a ‘dummy’ byte write sequence to load in the data word address.

Sequential Read: For the RTL8306G, the sequential reads are initiated by a random address read. After the 24LC01/02/04 receives a data word, it responds with an acknowledgement. As long as the 24LC01/02/04 receives an acknowledgement, it will continue to increment the data word address and clock out sequential data words in series.

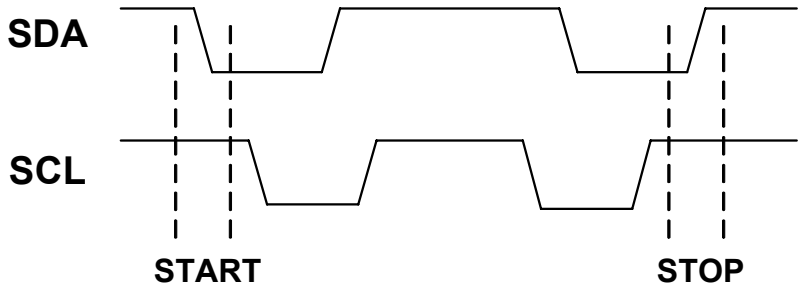


Figure 5. Start and Stop Definition

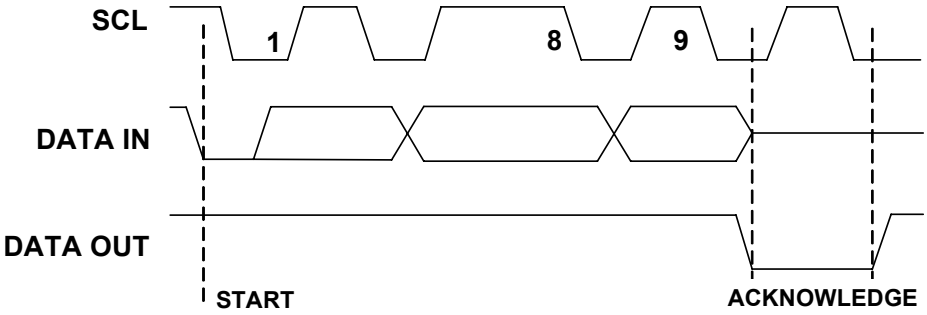


Figure 6. Output Acknowledge

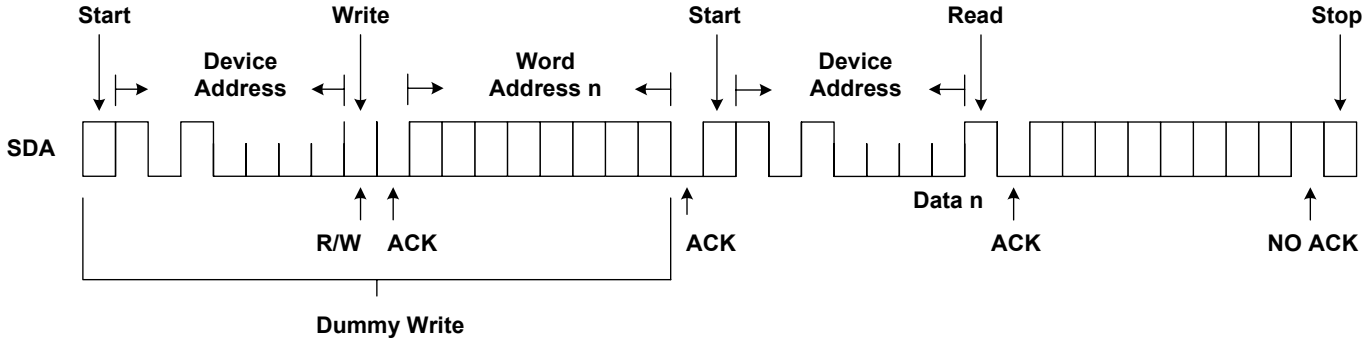


Figure 7. Random Read

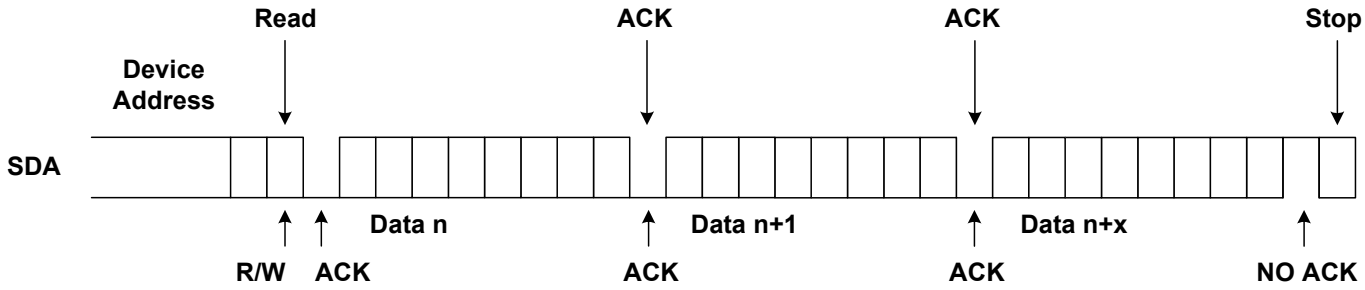


Figure 8. Sequential Read

7.3.3.2 EEPROM Size Selection

The RTL8306G supports three serial EEPROM sizes —1k bits, 2k bits, and 4k bits. Via the auto-download operation, the RTL8306G decides the size of the data downloaded to the RTL8306G from the EEPROM according to the value of bit 4 and bit 3 of the 77th byte data in the serial EEPROM.

If the bits 77 [4:3] = 11, it is reserved mode; if the bits 77 [4:3] = 10, 01, or 00, it means the data size is 4k bits, 2k bits, or 1k bits respectively. The value of the two bits should accord with the actual EEPROM data size. For example, the value of the bits 77 [4:3] cannot be '10' when the 24LC02 is used.

7.3.4. SMI

The SMI (Serial Management Interface) is also known as the MII Management Interface, and consists of two signals (MDIO and MDC). It allows external devices with SMI master mode (MDC is output) to control the state of the PHY and internal registers (SMI slave mode: MDC is input). MDC is an input clock for the RTL8306G to latch MDIO on its rising edge. The clock can run from DC to 2.5MHz. MDIO is a bi-directional connection used to write data to, or read data from the RTL8306G. The PHY address is from 0 to 6.

Table 13. SMI Read/Write Cycles

	Preamble (32 bits)	Start (2 bits)	OP Code (2 bits)	PHYAD (5 bits)	REGAD (5 bits)	Turn Around (2 bits)	Data (16 bits)	Idle
Read	1……..1	01	10	$A_4A_3A_2A_1A_0$	$R_4R_3R_2R_1R_0$	Z0	D_{15}…….D_0	Z*
Write	1……..1	01	01	$A_4A_3A_2A_1A_0$	$R_4R_3R_2R_1R_0$	10	D_{15}…….D_0	Z*

**: High-impedance. During idle time MDIO state is determined by an external 1.5KΩ pull-up resistor.*

The RTL8306G supports Preamble Suppression, which allows the MAC to issue Read/Write Cycles without preamble bits. However, for the first cycle of MII management after power-on reset, a 32-bit preamble is needed.

To guarantee the first successful SMI transaction after power-on reset, the external device should delay at least 1second before issuing the first SMI Read/Write Cycle relative to the rising edge of reset.

7.3.5. Head-Of-Line Blocking

The RTL8306G incorporates an advanced mechanism to prevent Head-Of-Line blocking problems when flow control is disabled. When the flow control function is disabled, the RTL8306G first checks the destination address of the incoming packet. If the destination port is congested, the RTL8306G will discard this packet to avoid blocking the next packet, which is going to a non-congested port.

7.3.6. Filtering/Forwarding Reserved Control Frame

The RTL8306G supports the ability to forward, drop or trap (to the CPU) the frames of the IEEE 802.1 specified reserved Ethernet multicast addresses.

Reserved Ethernet multicast addresses are illustrated in Table 14.

Table 14. Reserved Ethernet Multicast Addresses

D: Drop B: Broadcast (Search the Look-Up Table) C: Trap to CPU

Assignment	Value	Available Action
Bridge Group Address	01-80-C2-00-00-00	B (default), C
IEEE 802.3ad Slow_Protocols-Multicast Address	01-80-C2-00-00-02	D (default), B, C
IEEE 802.1X PAE Address	01-80-C2-00-00-03	B (default), C
All LANs Bridge Management Group Address	01-80-C2-00-00-10	B (default), C
GMRP Address	01-80-C2-00-00-20	B (default), C
GVRP Address	01-80-C2-00-00-21	B (default), C
Other Addresses 1	01-80-C2-00-00-04~0F	D, B (default), C
Other Addresses 2	01-80-C2-00-00-xx (xx≠00,01,02,03,04~0F,10,20,21)	B (default), C

7.3.7. Loop Detection

Loops should be avoided between switch applications. The simplest loop as shown below results in: 1) Unicast frame duplication; 2) Broadcast frame multiplication; 3) Address table non-convergence. Frames are transmitted from Switch1 to Switch 2 via Link 1, then returned to Switch 1 via Link 2.

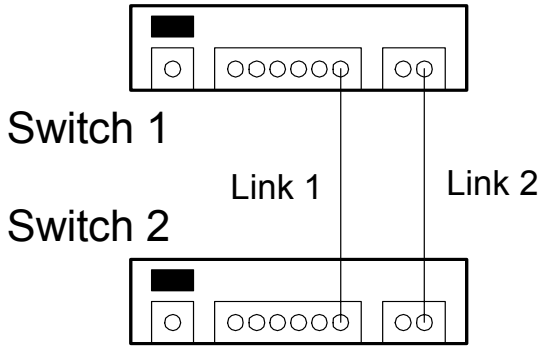


Figure 9. Loop Example

When the loop detection function is enabled, the RTL8306G sends out a broadcast 64-byte packet every 3~5 minutes and automatically detects whether there is a network loop (or bridge loop). If a loop is detected, the LoopLED# will be ON (active low or high). The LED goes out when both RTL8306G ports of the loop are unplugged. The Loop frame length is 64 bytes and its format is shown below.

Table 15. Loop Frame Format

FFFF FFFF FFFF	SID	8899	0300 000…0000	CRC

In order to achieve loop detection, each switch device needs a unique SID (the source MAC address). If the EEPROM is not used, a unique SID should be assigned via SMI after reset, and the default SID (52-54-4C-83-05-C0) should not be used.

7.3.8. MAC Local Loopback Return to External

Each port supports loopback of the MAC (return to external device) for diagnostic purposes.

Example 1: If the internal register, PHY4 (Page 0, 1) Reg.22.13=0 (Local loopback), the RTL8306G will forward local and broadcast packets from the input of Port 4 to the output of Port4, and drop unicast packets from the input of Port4. Other ports can still forward broadcast or unicast packets to Port4.

Example 2: If the internal register, PHY3 (Page 0,1) Reg.22.13=0 (Local loopback), the RTL8306G will forward local and broadcast packets from the input of Port3 to the output of Port3, and drop unicast packets from the input of Port3. Other ports can still forward broadcast or unicast packets to port3.

This is especially useful for router applications performing mass production tests. This function is independent of PHY type and can be done in each mode. Below are two examples: In Example 1 the external device (CPU) is connected to the MII interface of Port 4. In Example 2, the external device (CPU) does not have an MII interface, so it uses the PCI interface to connect an RTL8139 to the UTP port of Port 4.

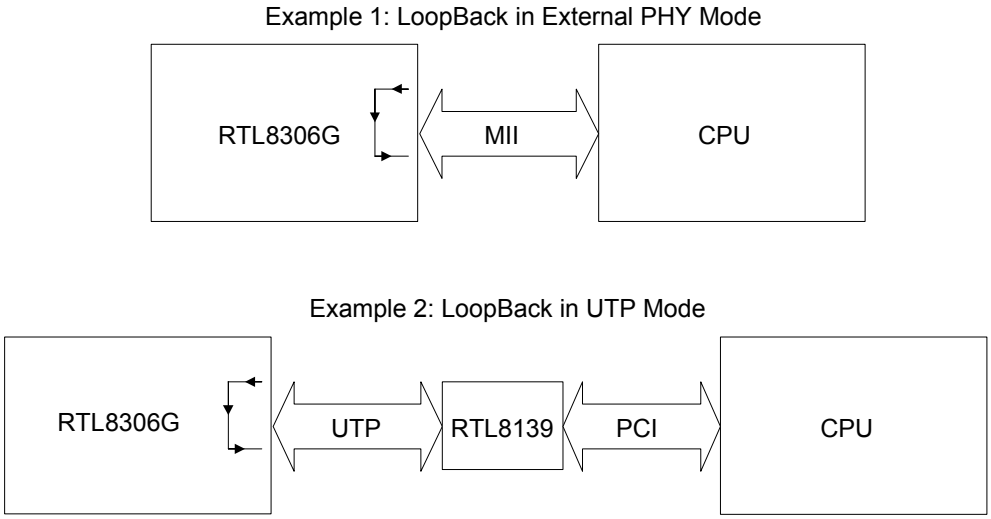


Figure 10. Port 4 Loopback

7.3.9. Reg.0.14 PHY Digital Loopback Return to Internal

The digital loopback mode of the PHY (return to internal MAC) may be enabled on a per-port basis by setting MII Reg.0.14 to 1. In digital loopback mode, the TXD of the PHY is transferred directly to the RXD of the PHY, with TXEN changed to CRS_DV, and returns to the MAC via an internal MII. The data stream coming from the MAC will not egress to the physical medium, and an incoming data stream from the network medium will be blocked in this mode. The packets will be looped back in 10Mbps full duplex or 100Mbps full duplex mode. This function is especially useful for diagnostic purposes. For example, a NIC can be used to send broadcast frames into Port0 of the RTL8306G and set Port1 to Reg0.14 Loopback. The frame will be looped back to Port0, so the received packet count can be checked to verify that the switch device is good. In this example, Port0 can be 10M or 100M, and full or half duplex.

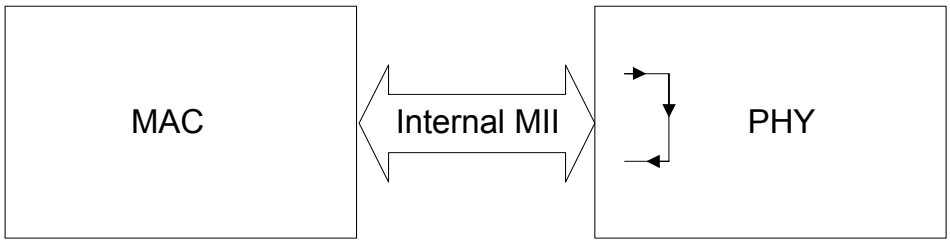


Figure 11. Reg. 0.14 Loopback

As the RTL8306G only supports digital loopback in full duplex mode, PHY Reg.0.8 for each port will always be kept on 1 when digital loopback is enabled. The digital loopback only functions on broadcast packets (DA=FF-FF-FF-FF-FF-FF). In loopback mode, the link LED of the loopback port should always be ON, and the Speed and Duplex LED combined to reflect the link status (100full/10full) correctly, regardless of what the previous status of this loopback port was.

Consider a case where a port is initially unlinked. When we set this port to digital loopback mode, the RTL8306G can get this port linked-up at the configured speed within 100ms, and will block the sending of UTP signals from this port.

7.3.10. 1.8V Power Generation

The RTL8306G can use a PNP transistor to generate 1.8V from a 3.3V power supply. This 1.8V is used for the digital core and analog receiver circuits. Do not use one PNP transistor for more than one RTL8306G chip, even if the rating is enough. Use one transistor for each RTL8306G chip.

Do not connect an inductor (bead) directly between the collector of the PNP transistor and AVDD18. This will adversely affect the stability of the 1.8V power to a significant degree.

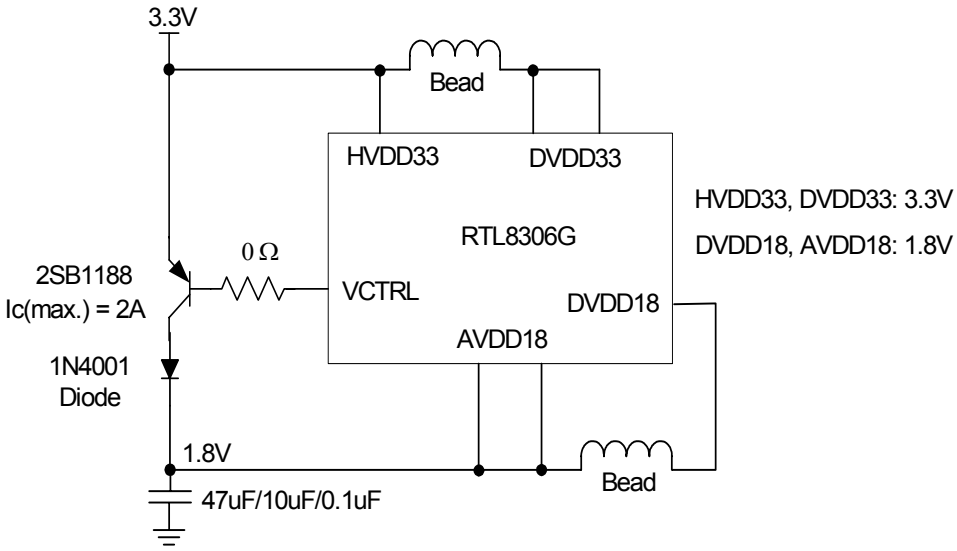


Figure 12. Using a PNP Transistor to Transform 3.3V Into 1.8V

Table 16. An Example Using Power Transistor 2SB1188

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	VCBO	-40	V
Collector-Emitter Voltage	VCEO	-32	V
Emitter-Base Voltage	VEBO	-5	V
Collector Current	IC	-2	A (DC)
Collector Power Dissipation	PC	0.5	W
Junction Temperature	Tj	150	°C
Storage Temperature	Tstg	-55~+150	°C

Note: Absolute maximum ratings (Ta=25°C).
For more information, refer to http://www.rohm.com

7.3.11. Crystal/Oscillator

The frequency is 25MHz. The maximum Frequency Tolerance is ±50ppm. The maximum Jitter is 150ps Peak-to-Peak.

8. Advanced Function Description

8.1. VLAN Function

8.1.1. Description

The RTL8306G supports 16 VLAN groups. These can be configured as port-based VLANs and/or IEEE 802.1Q tag-based VLANs. Two ingress filtering and egress filtering options provide flexible VLAN configuration:

- Ingress filtering option 1: The Acceptable Frame Type of the Ingress Process can be set to 'Admit All' or 'Admit All Tagged'
- Ingress filtering option 2: 'Admit' or 'Discard' frames associated with a VLAN for which that port is not in the member set
- Egress filtering option 1: 'Forward' or 'Discard' ARP broadcast frames
- Egress filtering option 2: 'Forward' or 'Discard' Leaky VLAN frames
- Egress filtering option 3: 'Forward' or 'Discard' multicast VLAN frames

VLAN tags can be inserted or removed at the output port. The RTL8306G will insert a Port VID (PVID) for untagged frames, or remove the tag from tagged frames. The RTL8306G also supports removal or keeping of VLAN tags according to the VID of the tagged frames.

The RTL8306G supports a special insert VLAN tag function to separate traffic from WAN and LAN sides in Router and Gateway applications.

In router applications, the router may want to know which input port this packet came from. The RTL8306G supports Port VID (PVID) for each port and can insert a PVID in the VLAN tag on egress. Using this function, VID information carried in the VLAN tag will be changed to PVID. The RTL8306G also provides an option to admit VLAN tagged packets with a specific PVID only. If this function is enabled, it will drop non-tagged packets and packets with an incorrect PVID.

The main VLAN features of the RTL8306G are as follows:

- Supports up to 16 VLAN groups
- Flexible IEEE 802.1Q port/tag-based VLAN
- Leaky VLAN for ARP broadcast packets
- Leaky VLAN for unicast packets
- Leaky VLAN for multicast packets
- Leaky inter-VLAN mirror function
- VLAN tag Insert/Remove function
- VLAN packet trap to CPU function
- Supports special VLAN tag insert or remove function on per-port basis (egress) to separate WAN traffic from LAN traffic

- VLAN related strapping pin
  - DISARP/LED_SPD[3]: Disable/Enable ARP broadcast to all VLANs
  - DISLEAKY/LED_ADD [2]: Disable/Enable forwarding unicast packets
  - DISVLAN/LED_SPD [4]: Disable/Enable VLAN function

8.1.2. Port-Based VLAN

If the VLAN function is enabled by pulling down the strapping pin DisVLAN, the default VLAN membership configuration by internal register is Port 4 overlapped with all the other ports to form four individual VLANs. This default configuration can be modified via an attached serial EEPROM or SMI interface. The 16 VLAN membership registers designed into the RTL8306G provide full flexibility for users to configure the input ports to associate with different VLAN groups. Each input port can join more than one VLAN group.

Port-based VLAN mapping is the simplest implicit mapping rule. Each ingress packet is assigned to a VLAN group based on the input port. It is not necessary to parse and inspect frames in real-time to determine their VLAN association. All the packets received on a given input port will be forwarded to this port's VLAN members. The RTL8306G supports VLAN indexes for each port to individually index this port to one of the 16 VLAN membership registers. A port that is not included in a VLAN's member set cannot transmit packets to this VLAN.

Figure 13 illustrates a typical application. VLAN indexes and VLAN member definitions are set to form three different VLAN groups.

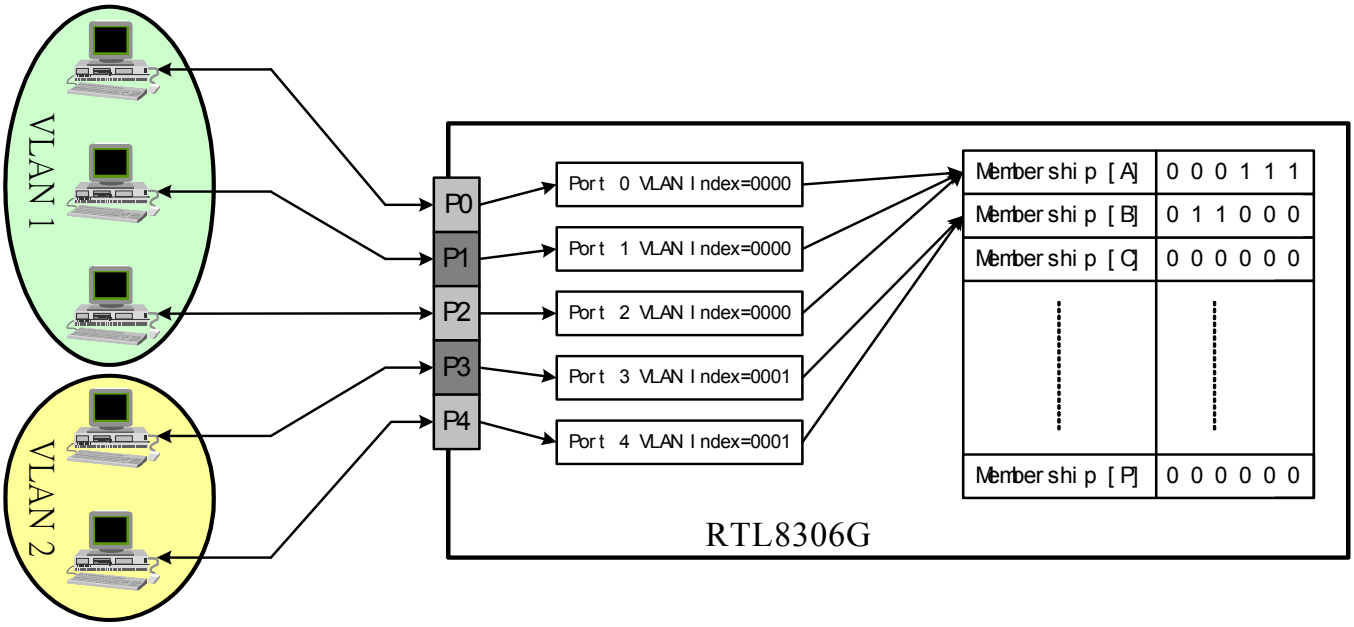


Figure 13. VLAN Grouping Example

The RTL8306G has a Port5 MAC, which can also be a VLAN member. Figure 14 illustrates a typical configuration in a port-based VLAN application that includes the Port5 MAC.

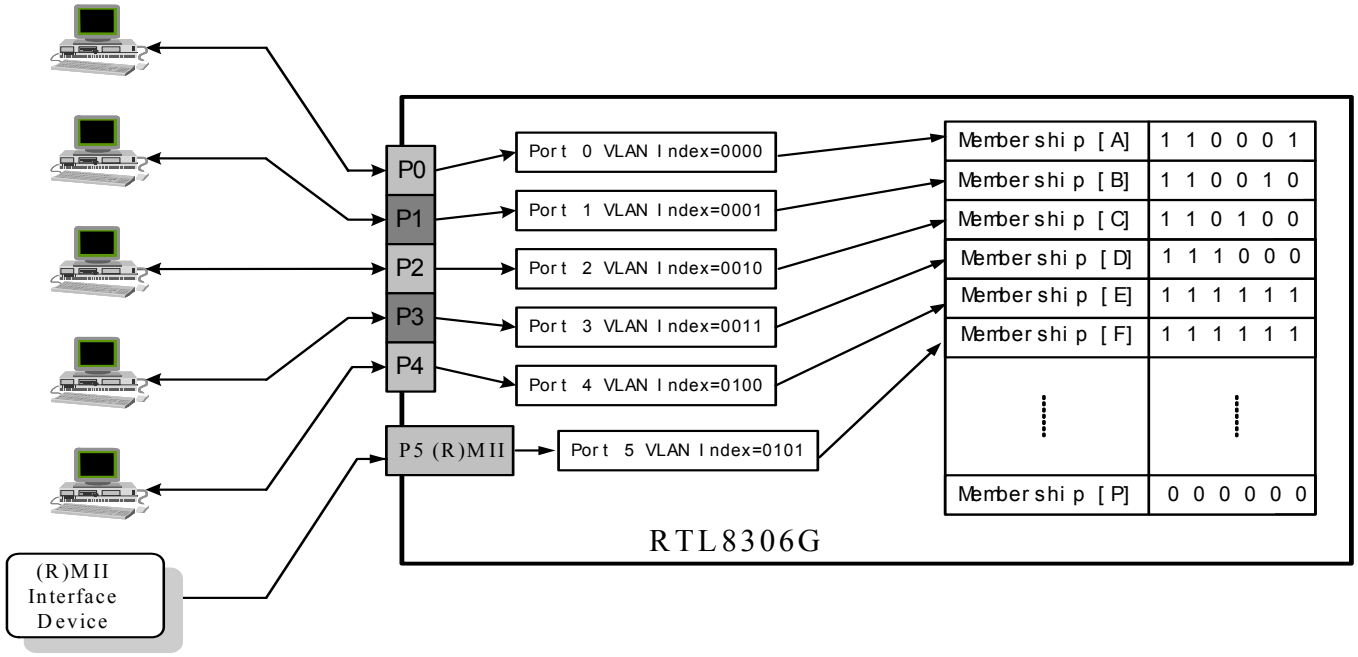


Figure 14. VLAN Grouping with Port5 MAC in Dual-(R)MII Mode

For non-VLAN tagged frames, the RTL8306G performs port-based VLAN. The VLAN ID associated with this indexed VLAN membership is the Port VID (PVID) of this port.

8.1.3. IEEE 802.1Q Tagged-VID Based VLAN

The RTL8306G supports 16 VLAN entries to perform IEEE 802.1Q-tagged VID-based VLAN mapping. The RTL8306G uses a 12-bit explicit identifier in the VLAN tag to associate received packets with a VLAN. If the VID of a VLAN-tagged frame does not match any of the 16 VLAN entries, the RTL8306G will drop the frame if the VLAN packet trap to the CPU port function is not disabled. Otherwise, the RTL8306G compares the explicit identifier in the VLAN tag with the 16 VLAN IDs to determine the VLAN association of this packet, and then forwards this packet to the member set of this VLAN. Two VIDs are reserved for special purposes. One of them is all 1's, which is reserved and currently unused. The other is all 0's, which indicates a priority tag. A priority-tagged frame should be treated as an untagged frame.

When '802.1Q tag aware VLAN' is enabled, the RTL8306G performs 802.1Q tag-based VLAN mapping for tagged frames, but still performs port-based VLAN mapping for untagged frames. If '802.1Q tag aware VLAN' is disabled, the RTL8306G performs only port-based VLAN mapping both on non-tagged and tagged frames.

Figure 15 illustrates the processing flow when '802.1Q tag aware VLAN' is enabled.

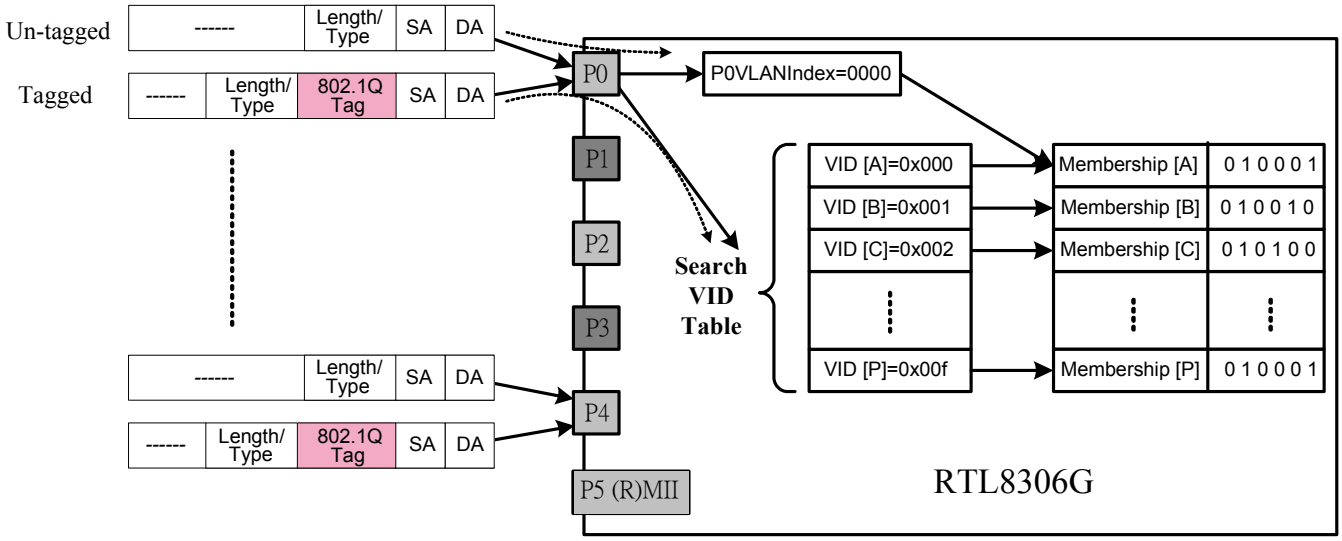


Figure 15. Tagged and Untagged Packet Forwarding when 802.1Q Tag Aware VLAN is Enabled

Two VLAN ingress filtering functions are supported by the RTL8306G. One provides the ability to receive VLAN-tagged frames only. Untagged or priority tagged (VID=0) frames will be dropped. The other can drop frames if the ingress port is not in the member set.

There are also four optional egress filtering functions:

- 'Unicast leaky VLAN' enables inter-VLAN unicast packet forwarding. That is, if the layer 2 lookup table search has a hit, then the unicast packet will be forwarded to the egress port, ignoring the egress rule.
- 'ARP leaky VLAN' enables broadcasting of ARP packets to all other ports, ignoring the egress rule.
- 'Multicast leaky VLAN' enables inter-VLAN multicast packet forwarding. Packets may be flooded to all the multicast address group member set, ignoring the VLAN member set domain limitation.
- 'Inter-VLAN mirror function' enables the inter-VLAN mirror function, ignoring the VLAN member set domain limitation. Default value is 'Enable the inter-VLAN mirror'.

Note: 'Unicast Leaky VLAN' and 'ARP Leaky VLAN' are supported by the RTL8306G through strapping.

8.1.4. VLAN Packet Trap to CPU Port

The RTL8306G supports trapping VLAN tagged packets to the CPU port when the VID does not match the entry in the VLAN table. With this function and the support of an external CPU, the RTL8306G can expand the VLAN table and support more than 16 VLAN entries. When using this function, the CPU function must be enabled and the CPU port must also be set. The behavior of VLAN packets trapped to the CPU will not follow the ingress rules of the VLAN (the ingress rule includes both discarding non-PVID, and also ingress filter options).

8.1.5. PVID

The RTL8306G supports Port VID (PVID) for each port to insert a PVID (or replace the VID with a PVID for VLAN-tagged packets) in the VLAN tag on an egress packet. The RTL8306G also provides an option to admit VLAN tagged packets with a specific PVID only. When IEEE 802.1Q tag-aware VLAN is enabled, the VLAN tag admit control and non-PVID Discard are enabled at the same time. Non-tagged packets and packets with an incorrect PVID will be dropped.

In IEEE 802.1Q tag-based VLAN applications, do not use port-based VLAN PVID, as the VID carried in the VLAN tag will be replaced with a PVID.

8.2. QoS Function

8.2.1. Bandwidth Control

8.2.1.1 Introduction

The RTL8306G supports MIN-MAX packet scheduling.

Packet scheduling offers three modes:

- Type I leaky bucket, which specifies the average rate of one queue (see Figure 16; only Q2 and Q3 have leaky bucket, Q0 and Q1 do not)
- Weighted Round Robin (WRR), which decides which queue is selected in one slot time to guarantee the minimal packet rate of one queue
- Port bandwidth control (type II leaky bucket) to control the bandwidth of the whole port

In addition, the RTL8306G can select one of the two sets of packet-scheduling configurations according to the packet-scheduling mode. Figure 16 shows the RTL8306G packet-scheduling block diagram.

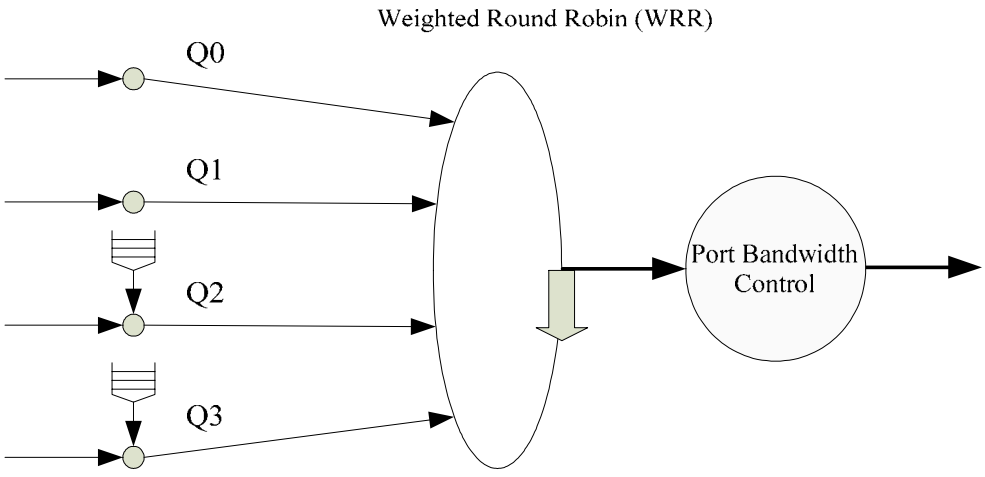


Figure 16. RTL8306G Packet-Scheduling Diagram

Weighted Round Robin (WRR)

WRR adds weighting on the basis of Round Robin; for example, assume Q3:Q2:Q1:Q0: 4:3:2:1, then the transmit order will be:

Q0->
Q1->Q1->
Q2->Q2->Q2->
Q3->Q3->Q3->Q3->

WRR guarantees a minimal packet rate for one queue only.

If there is strict priority (only in Q2 and Q3) and WRR at the same time, the queue with strict priority has higher priority than WRR. When the scheduler scans queues, queues with strict priority are scanned first, and then the other queues are scanned according to WRR. If there is more than one queue with strict priority, the queue with the bigger QID has higher priority.

8.2.1.2 Input (Rx) Bandwidth Control

Input bandwidth control limits the input bandwidth. When input traffic is more than the RX Bandwidth parameter, this port will either send out a ‘pause ON’ frame, or drop the input packet depending on flow control status.

8.2.2. Priority Assignment

Priority assignment specifies the priority of a received packet according to various rules. The RTL8306G can recognize the QoS priority information of incoming packets to give a different egress service priority.

The RTL8306G identifies the priority of packets based on several types of QoS priority information:

- Port-based priority
- IEEE 802.1p/Q VLAN priority tag
- DSCP priority field
- IP Address
- CPU tag

Below is a block diagram of the priority assignment.

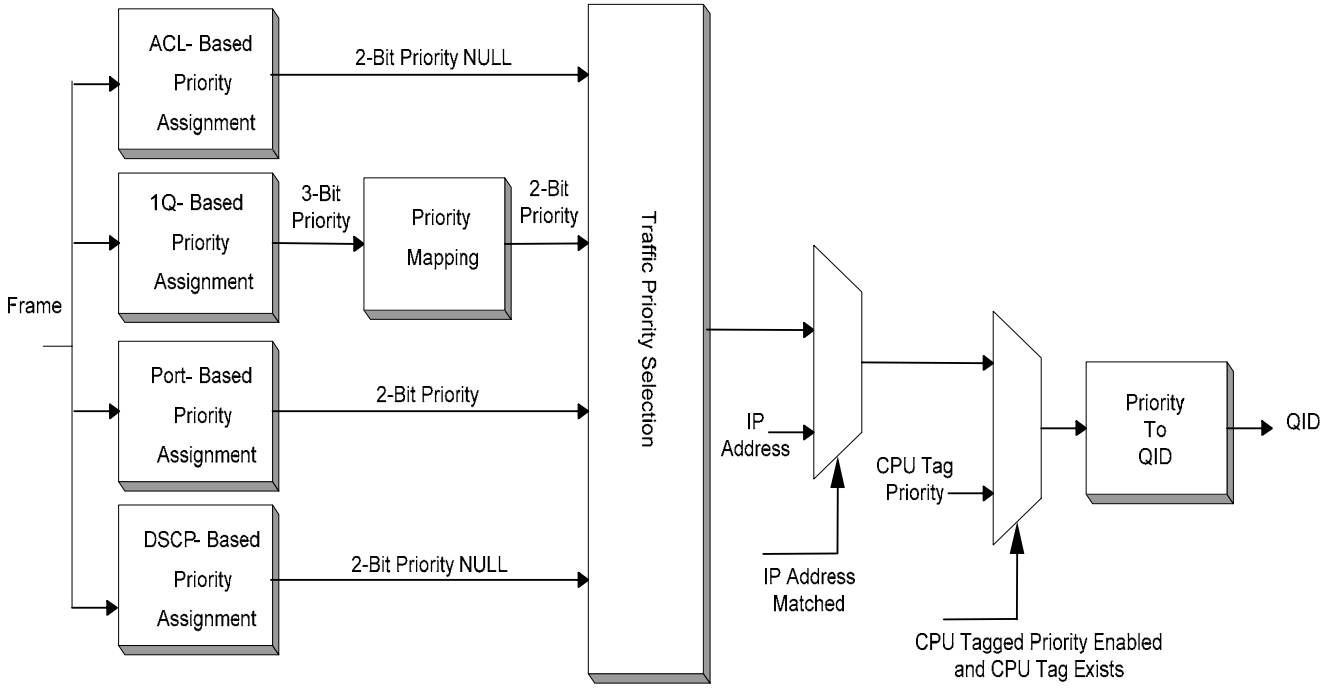


Figure 17. RTL8306G Priority Assignment Diagram

8.2.2.1 Queue Number Selection

In the RTL8306G, the output queue number of a particular port can be set. All ports follow a global configuration. The maximum number of output queues per port is 4. After changing the queue number via SMI (Serial Management Interface), the external device must perform a soft reset in order to update the configuration.

8.2.2.2 Port-Based Priority Assignment

Each physical port is assigned a 2-bit priority level. Packets received from a high-priority port are sent to the high-priority queue of the destination port. Port-based priority can be disabled by register setting.

8.2.2.3 IEEE 802.1Q-Based Priority Assignment

In IEEE 802.1Q-based priority assignment, when a packet is VLAN-tagged or priority-tagged, the 3-bit priority is specified by tag. When a packet is untagged, the 802.1Q-based priority is assigned to the default 2-bit priority information of a physical port. So, each port must provide a default 2-bit priority (every received packet must be assigned a 2-bit 1Q-Based Priority). When the priority comes from a packet, the 1Q-based priority is acquired by mapping 3-bit tag priority to 2-bit priority though a RTL8306G(M) 1Q-based Priority Mapping Table. The 1Q-based priority can be disabled.

8.2.2.4 DSCP-Based Priority Assignment

DSCP (Differentiated Services Code Point)-based priority assignment maps the DSCP of an IP packet to 2-bit priority information through a DSCP to priority table, as DSCP is only in the IP packet. A non-IP packet (such as a Layer 2 frame, ARP, etc) will get a NULL instead of a 2-bit priority. For an IPv6 IP header, DSCP-based priority assignment acquires the DSCP value according to the class of IPv6 header.

In the RTL8306G, DSCP-based priority assignment provides a DSCP to Priority Table of EF (Expected Forwarding), AF (Assured Forwarding), and network control. If the DSCP of a packet is not matched in the table, the DSCP-based priority is 0b00, The DSCP-based priority can be disabled by control bit DisDSPri[i]. The RTL8306G provides two sets of registers to set Differential service priority. When they are enabled, the priority value can be set in registers.

8.2.2.5 IP Address-Based Priority

When IP-based priority is enabled, any incoming packets with source or destination IP address equal to the configuration in register IP Priority Address [A] and IP Priority Mask [A], or IP Priority Address [B] and IP Priority Mask [B] will be set to a 2-bit priority.

IP priority [A] and IP priority [B] may be enabled or disabled independently. IP address-based priority can be enabled or disabled by the control register.

8.2.2.6 CPU Tag-Based Priority

A packet transmitted from the CPU port may have CPU tag priority assigned in the ‘priority’ field of the CPU (Table 17). CPU tag-based priority can be enabled via register setting.

Table 17. CPU Tag Format

15	8	7	0
Realtek EtherType(2) [0x8899]			
Protocol (4-bit) [0x9]	Priority (2-bit)	Reserved (4-bit)	Tx/Rx (6-bit)

There are two limitations for the control bit:

- When CPU tag priority is disabled, the switch controller will only recognize the port-based priority of packets that have both the CPU tag and VLAN tag.
- When CPU tagged-packet awareness is disabled, CPU tag-based priority will not function

8.2.2.7 Packet Priority Selection

As one received packet may simultaneously support several priority assignment mechanisms, e.g., Port-Based Priority, 1Q-Based Priority, DSCP-Based Priority, and CPU tag-Based Priority, it may get several different priority values.

- If it is enabled and the packet has a CPU tag, CPU tag-based priority has highest priority. The final priority is equal to CPU tag-based priority
- If CPU tag-based priority is not enabled, IP address priority has the highest priority. If the IP address is matched, the final priority is equal to the IP address priority
- If CPU tag-based priority and IP address priority are both disabled, the following rules are used to decide a final priority for the other four types of priority

There is a 4-bit register for each of the four types of priority, which represents the weight of the priority. The higher bit marked '1' in the register indicates a higher weight for the priority

For example, when Weight of port-based priority=0010, Weight of 1Q-based priority=0010, Weight of DSCP priority=0100, and Weight of CPU tag-Based priority=1000:

- If it has CPU tag-Based-Based Priority, the final priority is set to CPU tag-Based-Based Priority
- If it has DSCP-Based Priority (and no CPU tag-Based-Based Priority), the final priority is set to DSCP-Based Priority
- If it has neither CPU tag-Based nor DSCP-Based Priority, the priority is decided by the higher one between the Port-Based Priority and the1Q-Based Priority

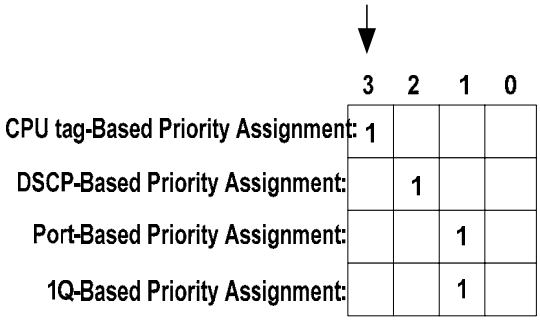


Figure 18. Packet Priority Selection

The 2-bit priority has four numbers; however, every port has at most four output queues, so every port needs a User Priority to Traffic Class Mapping Table to map the priority to QID. The whole system provides two sets of Traffic Class Mapping Tables. Each port can select one of them according to Traffic Class Mapping mode selection.

Priority	Number of Available Traffic Classes			
	1	2	3	4
0 (default)	0	0	1	1
1	0	0	0	0
2	0	1	1	2
3	0	1	2	3

8.2.2.8 Priority Controlled By Strapping Pin

The RTL8306G supports strapping pins to control port-based, DSCP-based, and 1Q-based priority. If any of those priorities are enabled through the strapping pins (pins 68, 91, 88, 86, 85, 84, 83), the output queue of each port will simultaneously be divided to 2 queues; a high queue and low queue. The default rate of the 2 queues weight of WRR is 16:1 (high:low). A synchronous change of the queue number will not occur in the RTL8306G when those priorities are enabled through the registers.

8.3. Lookup Table Function

8.3.1. Function Description

- 2048-entry lookup table
- 16-entry CAM to reduce hash collisions
- 4-way entry for each entry index to reduce MAC address hash collisions
- 2048-entry lookup table can be accessed by SMI and supports multicast and static addresses
- External Look-Up Table write access has higher priority than switch auto-learning function
- Supports LRU (Least Recently Used) function for lookup table learning

8.3.2. 4-Way Direct Mapping Algorithm

For unicast packet learning and search or multicast packet search, the RTL8306G applies a 4-Way Direct-Mapping algorithm.

The RTL8306G uses an index to assign the learning entry position. For each index, there are 4 entries to save the hash collision MAC address.

8.3.3. Lookup and CAM Table Definition

8.3.3.1 Lookup Table Access

All content of each lookup table entry of the RTL8306G can be accessed through SMI, including the destination port ID, aging timer, author properties, etc. All the lookup table entries can be read or written as multicast or unicast entries.

8.3.3.2 Least Recently Used (LRU) Function Description

In traditional switch learning, if a MAC address hash collision occurs and the CAM is full, then the later MAC address in the collision will not be learned into the lookup table. The LRU function attempts to resolve this problem.

When Enable LRU = 0b1, then the LRU function is enabled. If the Source MAC address of the incoming packet encounters a hash collision during the learning process, when the 4-way entries are all occupied and the 16-entry CAM are all full, then the switch will learn the address in one of the 4-way entries using the LRU aging timer. The criteria for selecting the entry is comparing via the aging timer and choosing the oldest one. If the aging timer of the 4 entries are the same, then the least Entry_Address[1:0] is selected.

There are 3-bit registers for the LRU function:

- Enable LRU: Enables or disables this function
- Disable CAM: For optional over-writing of the 4-way entries regardless of CAM status. LRU will directly over-write one of the 4-way entries, even if the CAM is not full
- CAM Full State: Indicates that the CAM is full. When the 16-entries in the CAM are full, the signal will be 0b1. When the CAM is not full, the signal will be 0b0

8.4. IEEE 802.1p Remarking Function

The RTL8306G provides IEEE 802.1p Remarking ability. Each port can enable or disable IEEE 802.1p Remarking ability.

In addition, there is a RTL8306G global IEEE 802.1p Remarking Table. When one port enables 802.1p Remarking ability, 2-bit priority (not QID) determined by the RTL8306G is mapped to 3-bit priority according to the 1p Remarking Table.

If the port's 1p remarking function is enabled, transmitting VLAN tagged packets will have the 1Q VLAN tag's Priority field replaced with the 3-bit 1p remarking Priority.

When the VLAN tags are inserted to non-tagged packets, the inserted tag's priority will accord with the 1p remarking table, even if the port's 1p remarking function is disabled. When the VLAN tag is replaced for a tagged packets and the 1p remarking function is disabled, the VLAN tag's VID will be replaced but the priority will not change.

8.5. MIBS Function

8.5.1. MIB Counter Description

The RTL8306G implements five 32-bit MIB Counters on each port for traffic management and diagnostic purposes. The five MIB counters are Tx Counter, Rx Counter, Rx Drop Counter, Rx CRC Counter, and Rx Fragment Counter. The Tx Counter and Rx Counter can be byte-based or packet-based for each port. There is also an on-off register for each port to enable or disable/clear MIB Counters. Pause frame on/off is not counted in any condition. These MIB Counters are described below:

- Tx Counter:
  TX byte or packet count. This counter is incremented once for every data byte/packet of a transmitted packet
- Rx Counter:
  RX byte or packet count. This counter is incremented once for every data byte of a received and forwarded good packet. RX byte/packet count includes both forwarded and dropped good packets. For mirror RX forwarded packets, if these are not good packets they will not be counted
- Rx Drop Counter:
  RX drop packet count. Packet drop events could be due to lack of resource, local packet, etc. If the mirror RX function is enabled and the packets are only received by the mirror port, these packets are also included in the mirrored port's drop packet counter. Packet lengths less than 64 bytes are not included
- Rx CRC Counter:
  RX CRC error packet count. This counter is incremented once for every received packet with a length more than 64 bytes but with a CRC error. Oversize packets are also included in this counter
- Rx Fragment Counter:
  RX fragment, collision, and undersize packet count. These packet lengths are less than 64 bytes

As data can only be read 16-bits at one time, when reading these 32-bit counters through an SMI interface, they should always read low bits (bit [15:0]) first. Both the low 16 bits and high 16 bits are latched, and it should read the high bits register in the immediately following read cycle.

8.5.2. MIB Counter Enable/Clear

After power on reset, the counters are all reset to 0. A read access of the MIB counter will not reset the counter to 0. When power-on occurs, the counters will be cleared to 0.

A Disable/Enable MIB Counter register is provided for each port. When 'Disable Port x MIB counter' is asserted to 1, the corresponding port's MIB counter will be cleared to 0 and counting stopped. When 'Disable Port x MIB counter' is asserted to 0, the corresponding port's MIB counter is enabled and starts counting.

8.5.3. MIB Counter Timeout

The period of time before the next read of the same counter should not be longer than the counter's timeout. The timeout of the 32-bit MIB counter depends on the object type and the port speed, and is calculated as shown in Table 18.

Table 18. MIB Counter Timeout

Port Speed	MIB Object Type	MIB Counter Timeout (Sec.)
100Mbps	Packet Count	28862
	Byte Count	348
10Mbps	Packet Count	288621
	Byte Count	3481

Note: Packet counter timeout is calculated based on 64-byte packets and byte counter timeout is calculated based on 1518-byte packets.

8.6. Storm Filter Function

The RTL8306G can effectively control broadcast storms caused by broadcast packets, multicast packets, and unknown DA unicast packets. An option to drop all broadcast packets (DA=ff-ff-ff-ff-ff-ff) sent to the CPU port is also provided. This function reduces the process loading of the CPU.

Note: Broadcast packets discussed here are packets whose DA is ff-ff-ff-ff-ff-ff.

Multicast packets are those whose DA is a multicast address, but excluding 01-80-C2-00-00-xx.

An unknown DA unicast packet is a packet whose DA is a unicast address and is not found in the lookup table of the switch.

When broadcast (or multicast, unknown DA unicast) storm filtering is enabled, each port of the RTL8306G will permit only 64 (or 32, 16, 8, as determined by register setting) consecutive broadcast (or multicast, unknown DA unicast) packets to be forwarded to other ports in each iteration of about 800ms (or 400ms, 200ms, 100ms, as determined by register setting). The RTL8306G drops all following incoming broadcast (or non-multicast, non-unknown DA unicast) packets in the iteration.

The 800ms timer is free running. The 64-packet counter counts from the first broadcast (or multicast, unknown DA unicast) packet received and it can be optionally reset to 0 after receiving a non-broadcast (or non-multicast, non-unknown DA unicast) packet. This option enables timer release only for the triggered storm filter. Once enabled, the storm filter can be released only after the storm filter timer times out.

The three types of storm filter work independently and can be employed simultaneously. For example, if the broadcast storm filter and multicast storm filter are enabled at one time, receiving a multicast packet (DA=01-80-C2-00-00-xx not included) at a specific port will cause the port's broadcast packet counter to reset and to begin counting multicast packets, and vice versa. If the interrupt is enabled, there will be an interrupt signal when a storm filter is triggered.

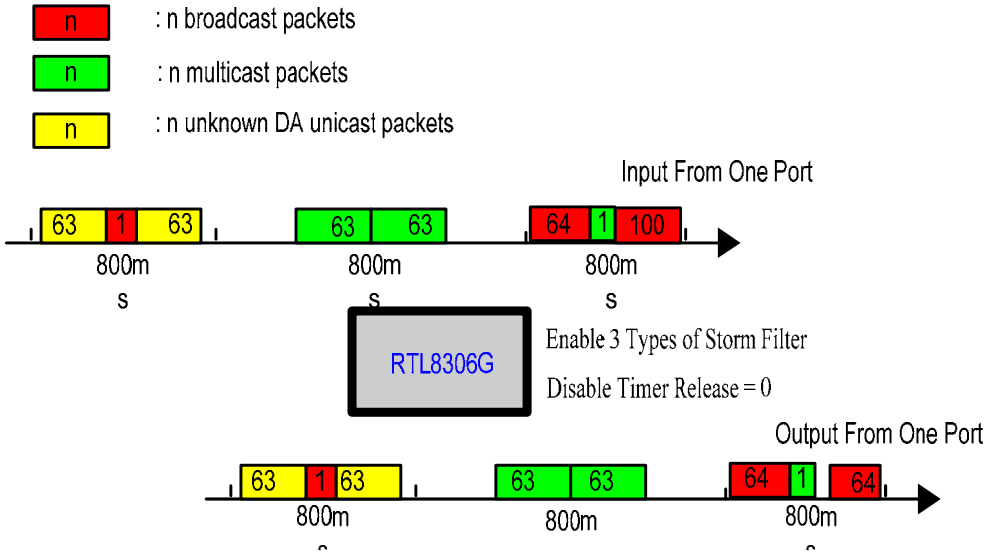


Figure 19. Storm Filter Application Example

8.7. CPU Interrupt Function

The RTL8306G supports a CPU interrupt function to inform the CPU of changes to the switch controller's link status and of storm filter events. When this function is enabled, the change of any port's link status or storm filter event will trigger a level mode and low active interrupt signal on the CPU interrupt pin (Pin 46). The output of the CPU interrupt pin can be optionally disabled.

As there is an interrupt event flag register that records the ports the link changes occur on, the CPU can get the correct interrupt source through the register when an interrupt occurs. Once the interrupt event flag register is read, the flag bits in it will be self-cleared. The output of the CPU interrupt pin is determined by the interrupt event flag register. It outputs high only when all of the flag bits in the interrupt event flag register are '0'. Otherwise, it outputs low.

There also is an interrupt mask register involved in the function implementation. Any port's link change interrupt can be disabled independently through this register.

8.8. IGMP & MLD Snooping Function

The RTL8306G supports IGMP v1/v2/v3 and MLD v1/v2 snooping. The RTL8306G can trap all IGMP and MLD packets to the CPU port. The CPU processes these packets, gets the IP multicast group information of all ports, and writes the correct multicast entry to the lookup table via SMI. The RTL8306G provides an option to drop or broadcast multicast packets when the multicast MAC address does not exist in the lookup table.

IGMP & MLD snooping only operates when the CPU port function is enabled. If the CPU port function and IGMP snooping are both enabled, the RTL8306G traps all packets to the CPU where:

- EtherType is 0x0800 and the protocol field in the IP header is 0x02 (for PPPoE packets the EtherType is 0x8864 and PPP protocol=0x0021)

If the CPU port function and MLD snooping are both enabled, the RTL8306G will trap all packets to the CPU where:

- EtherType is 0x86DD and the next header field in the IPv6 header is 0x00 (for PPPoE packets EtherType is 0x8864 and PPP protocol=0x0057) to CPU
- MLD packets have three characteristics:
  1. EtherType=0x86DD (2bytes) (for PPPoE packets, EtherType = 0x8864 and PPP protocol = 0x0057)
  2. 'Next header' = 0 (1byte) in IPv6 header
  3. 'Route alert option' = 0x05020000 (4bytes) in hop-by-hop option header

If a packet matches the first two characteristics, it will be trapped to the CPU. The CPU will then check the 'Route alert option' and other fields to determine whether the packet is an MLD packet.

To avoid a loop condition, IGMP and MLD packets received from the CPU port will never be trapped, even if all options enable trapping action.

A typical application of the RTL8306G IGMP and MLD snooping function is shown in Figure 20.

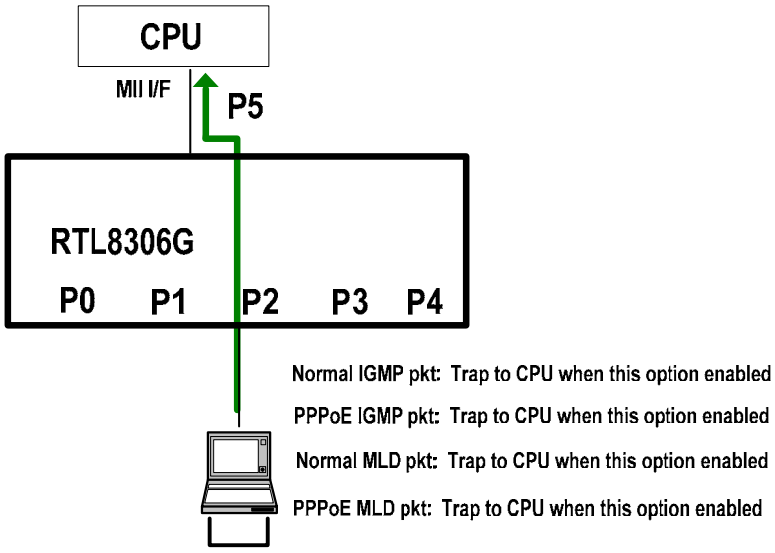


Figure 20. IGMP & MLD Application Example

8.9. CPU Tag Function

The RTL8306G can insert a CPU tag that contains source-port information to the packets sent to the CPU port.

There are two circumstances where the CPU tag is useful:

- The CPU needs the source-port information of the packets trapped to the CPU
- The CPU can use the CPU tag to inform the RTL8306G of the packet's destination port

The tag format is shown in Table 19.

Table 19. CPU Tag Format

15 8	7 0
Realtek EtherType(2) [0x8899]	
Protocol (4-bit) [0x9]	Priority (2-bit)	Reserved (4-bit)	Tx/Rx (6-bit)

The CPU tag is inserted behind the packet's SA. The EtherType field of the tag is assigned by register. Its default value is 0x8899, which is a Realtek proprietary number. The following protocol field is fixed to 0x9.

When the RTL8306G inserts a CPU tag to a packet forwarded to the CPU, the priority field will be filled with the packet final priority from the QoS rule.

- When the RTL8306G receives a packet with a CPU tag inserted by the CPU, the priority field indicates the CPU-assigned priority for this packet
- The Tx/Rx field is Rx when the CPU tag is inserted by the RTL8306G, and it indicates the packet's source port. The Tx/Rx field is Tx when the CPU tag is inserted by the CPU, and it indicates the packet's destination port

The bit for Tx/Rx field to port mapping is shown in Table 20. Writing '1' in the field means the corresponding port is the source port (for Rx) or destination port (for Tx) of the packet.

Table 20. Bit to Port Mapping in CPU Tag

Tx/Rx					
MSB					**LSB**
Port 5	Port 4	Port 3	Port 2	Port 1	Port 0

CPU tag insertion is independent from IGMP & MLD snooping. All packets sent to the CPU port (including any packets unicast or broadcast to the CPU port) will be inserted with a CPU tag when CPU tag insertion is enabled. When CPU tag removal is enabled, if the EtherType matches the CPU tag content register and the following 4 bits are 0x9, the RTL8306G will remove the 32 bits following the SA of the packet. Then the RTL8306G retrieves the CPU assigned priority in the tag and forwards it with the destination port information in the CPU tag.

There is an option for the RTL8306G to check a CPU-tagged packet's CRC, which can greatly reduce the external CPU's loading. Another configuration option enables or disables CPU tagged-packet awareness.

A typical application of the RTL8306G CPU tag function is shown in Figure 21.

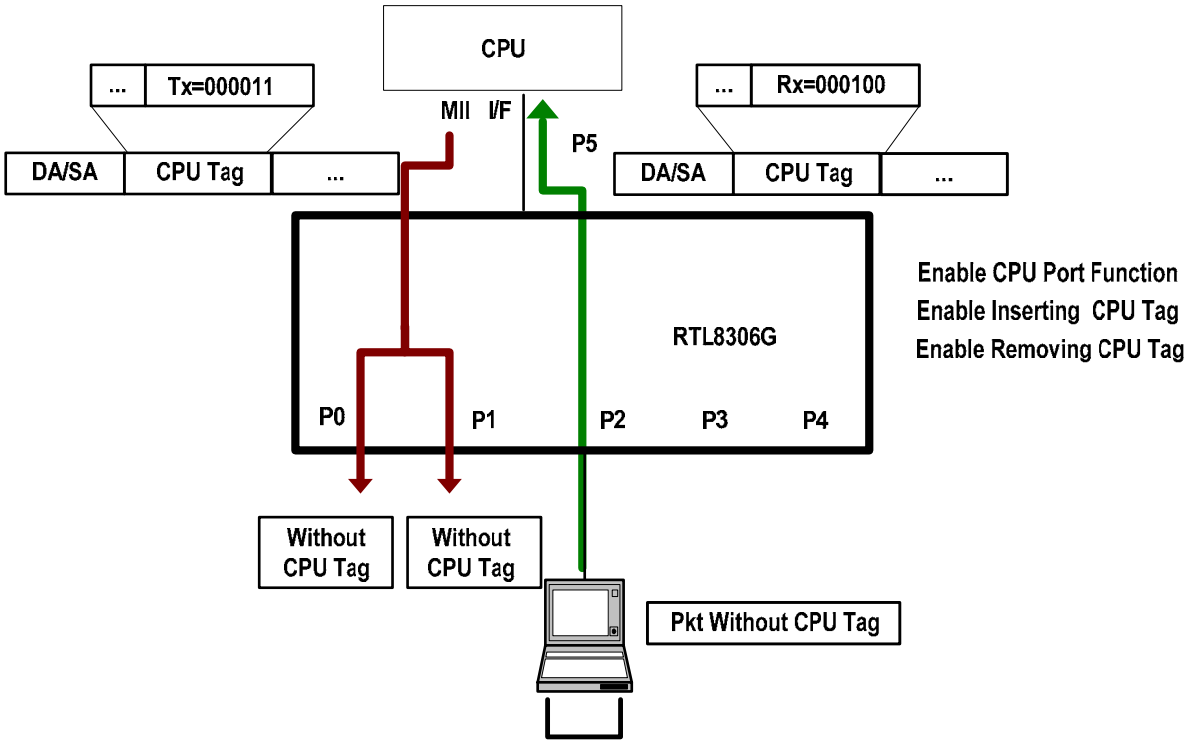


Figure 21. CPU Tag Application Example

8.10. IEEE 802.1x Function

The RTL8306G supports IEEE 802.1x Port-based/MAC-based Access Control.

When port-based access control and MAC-based access control are both enabled, only frames that comply with both port-based access control and MAC-based access control will be forwarded. The IEEE 802.1x Port-based/MAC-based Access Control rules will be ignored for the following two types of packets:

- CPU tagged packets (only when CPU tagged-packet awareness is disabled)
- Reserved control packets (which will be trapped to the CPU)

8.10.1. Port-Based Access Control

When a PC host connects to a RTL8306G-controlled switch, the switch will ask the PC host for authentication. The switch will transmit the information sent by the host to the authentication server for authenticating.

- When the register 'Port-based Authorization status of 802.1x for Port x'=1, that is, the port is authenticated, its traffic will be normally received or sent
- When the register 'Port-based Authorization status of 802.1x for Port x'=0, that is, the port is not authenticated, its traffic will not be normally forwarded

The register 'Direction of 802.1x control for Port x' decides whether or not the traffic of other ports can be forwarded to the port.

- If 'Direction of 802.1x control for Port x'=0, packets need to pass 802.1x authorization in the input direction and the output direction for Port-Based Access Control
- If 'Direction of 802.1x control for Port x'=1, packets only need pass 802.1x authorization in the input direction for Port-Based Access Control. Output direction packets will bypass the 802.1x authorization rule

8.10.2. MAC-Based Access Control

MAC-Based Access Control provides authentication for multiple logical ports. Each logical port represents a source MAC address. There are multiple logical ports for a physical port. When a logical port or a MAC address is authenticated, the DTE using the MAC address has the authorization to access the network. A frame with a source MAC address that is not authenticated by the 802.1x function will be dropped or trapped to the CPU.

When the register bit 'Enable Mac-based authorization of 802.1x for Port x'=1, it means port n has MAC-Based access control ability. In this condition, if a MAC address is authenticated by EAPOL, the 'Author' bit in the corresponding lookup table entry should be set to '1', which indicates that the address is authenticated. If a MAC address is unauthenticated, the 'Author' bit should be set to '0'. A received frame with unauthenticated source MAC address will be dropped or trapped to the CPU, which is determined based on the register 'Operation of 802.1x unauthorized frame'.

There is another register used for the control of MAC-based access:

- If the register 'Direction for 802.1x MAC-Based Access Control'=0, the forwarding packets need to pass 802.1x authorization in both the input direction and output direction for Mac-Based Access Control.
- If 'Direction for 802.1x MAC-Based Access Control'=1, the forwarding packets only need pass 802.1x authorization in the input direction for Mac-Based Access Control.

IEEE 802.1X MAC-based authentication processing is handled by the CPU and the authentication server. When a Source-MAC-Address is authorized, the CPU will write an 802.1X MAC-Based Entry (AUTH=1) into the MAC-Address-Table. The behavior is determined based on Table 21.

Table 21. IEEE 802.1x MAC-Based Entry

MAC-Based	Static	Auth	Description	Aging	Aging Out	Update MBR
0 (Disable)	0	0	General Dynamic Entry	Yes	Yes	Yes
0	0	1	802.1x Dynamic Entry (do not bind host to any specified port)	Yes	No	Yes
0	1	0	General Static Entry	Yes	No	No
0	1	1	802.1x Static Entry (bind host to a specified port)	Yes	No	No
1 (Enable)	0	0	General Dynamic Entry	Yes	Yes	Yes
1	0	1	802.1x Dynamic Entry (do not bind authenticated host to any specified port)	Yes	No	Yes
1	1	0	General Static Entry	Yes	No	No
1	1	1	802.1x Static Entry (bind authenticated host to a specified port)	Yes	No	No

8.11. IEEE 802.1D Function

When using IEEE 802.1D, the RTL8306G supports four status' for each port:

Disabled

The port will not transmit/receive packets, and will not perform learning.

Blocking

The port will only receive BPDU spanning tree protocol packets, but will not transmit any packets, and will not perform learning.

Learning

The port will receive any packet, including BPDU spanning tree protocol packets, and will perform learning, but will only transmit BPDU spanning tree protocol packets.

Forwarding

The port will transmit/receive all packets, and will perform learning.

The RTL8306G also supports a per-port transmission/reception enable/disable function. Users can control the port state via register.

Behaviors are shown in the following table.

Table 22. Behavior on TX_EN, RX_EN, and PSTAn

A: All packets
B: BPDU packet
D: Disable. RX will not learn; TX will not send any packets
L: Learn all packets, but do not forward

TX_EN	RX_EN	PSTAn	Description
0	0	00	RX (D) TX (D)
		01	RX (D) TX (D)
		10	RX (D) TX (D)
		11	RX (D) TX (D)
0	1	00	RX (D) TX (D)
		01	RX (B) TX (D)
		10	RX (L) TX (B)
		11	RX (A) TX (D)
1	0	00	RX (D) TX (D)
		01	RX (D) TX (D)
		10	RX (D) TX (B)
		11	RX (D) TX (A)
1	1	00	RX (D) TX (D)
		01	RX (B) TX (D)
		10	RX (L) TX (B)
		11	RX (A) TX (A)

8.12. Input & Output Drop Function

If some destination ports are blocking or the buffer is full, the frames to these ports will be dropped.

There are two types of drop:

- Input Drop: Drop the frame directly. Do not forward to any port.
- Output Drop: Forward only to non-blocking ports.

For the RTL8306G, the dropping of broadcast, multicast, and unknown DA frames can be controlled independently.

The Input/Output drop behavior abides by the rules shown in Table 23.

Table 23. Behavior According to En_input, En_Bro_input, En_Mul_input, En_UDA_input

En_input			
0	En_Bro_input	0	Output Drop
		1	Input Drop
	En_Mul_input	0	Output Drop
		1	Input Drop
	En_UDA_input	0	Output Drop
		1	Input Drop
1	En_Bro_input	0	Input Drop
		1	Input Drop
	En_Mul_input	0	Input Drop
		1	Input Drop
	En_UDA_input	0	Input Drop
		1	Input Drop

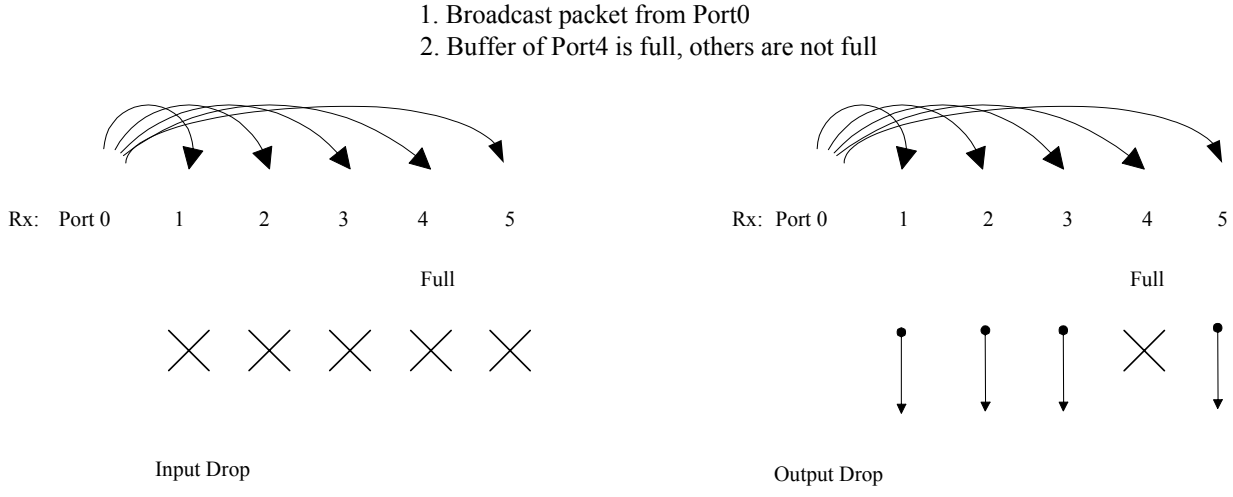


Figure 22. Broadcast Input Drop vs. Output Drop

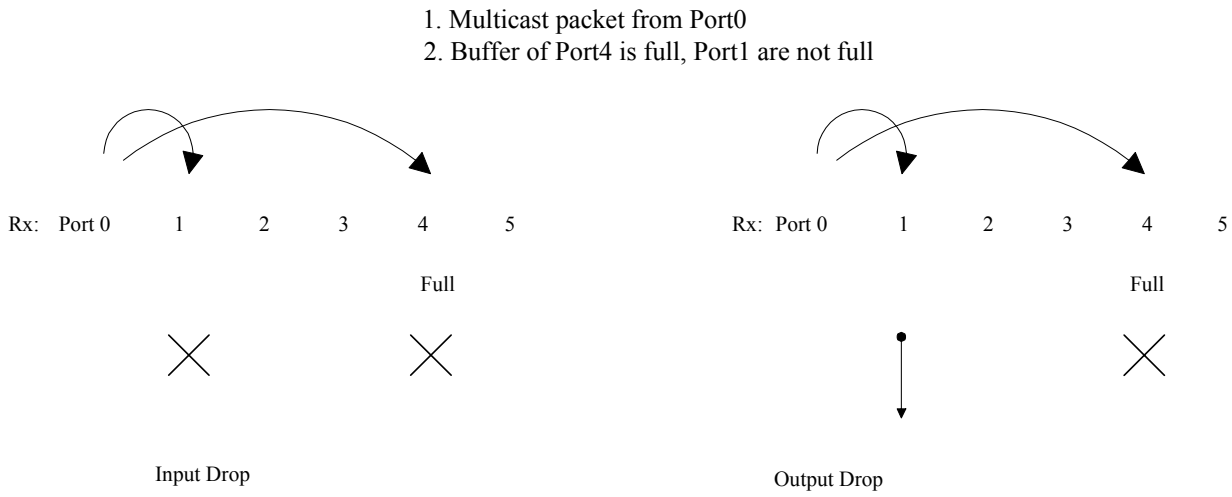


Figure 23. Multicast Input Drop vs. Output Drop

8.13. Port Mirroring

The RTL8306G supports one set of mirroring functions for all 6 ports. The Mirror port can mirror both the TX and RX packets of the mirrored port. When a port is set as mirror port, mirrored packets will be sent to this port. Only one port can be set as mirror port. The mirror port can be selected in *Mirror Port ID [2:0]*. The mirrored TX port and the mirrored RX port can be selected in *Enable mirror port [5:0] TX* and *Enable mirror port [5:0] RX*.

If the mirror port and normal port send packets to mirrored ports at the same time, and mirror self filter is enabled (*Enable mirror filter*=1), mirrored TX packets will not include packets sent from the mirror port. For example, Port_M mirror port_N TX, Port_N TX packets include packets from port_M and port_L. If *Enable mirror filter*=1, port_M can only mirror packets from port_L.

If the SA and DA filter function is enabled (*Enable mirror function*=1), the mirror port can only mirror a TX mirrored port's packets with a matching DA (depending on the *Mirrored MAC address [47:0]* register setting). The Mirror port can also only mirror an RX mirrored port's packets with a matching SA (depending on the *Mirrored MAC address [47:0]* register setting).

The mirror port also has the VLAN mirror leaky function. When mirrored ports belong to one VLAN (A), and the mirror port belongs to another VLAN (B), the mirror port can mirror packets inter-VLAN when *Disable inter-VLANs mirror function*=0.

If the mirror port is not validated, it cannot mirror other ports. If the mirror port has been validated, but the mirrored port TX is not validated, the mirror port can mirror RX, but cannot mirror TX.

If the CPU port is set as mirror port, mirrored packets will have a CPU tag (if CPU tag function is enabled). If the CPU port is set as mirrored port, the mirror port cannot mirror packets with a CPU tag, but can mirror packets without a CPU tag.

When mirroring TX, if one queue by which packets are sent out is full, the Mirror port cannot mirror TX, but can mirror RX.

8.14. LED Function

The RTL8306G provides flexible LED functions for diagnostics. These include: three combinations of link, activity, speed, duplex, and collision, which are ideal for bi-color LED displays.

The RTL8306G provides a CPU controlling LED function. Some registers are defined to control LED displays.

The RTL8306G also provides a loop-detection function and alarm, for network existence notification, with an output pin that can be designed as a visual LED or a status input pin for a CPU.

Each port has four LED indicator pins. These are divided into 4 groups (A, B, C, D). When the RTL8306G controls an LED, each pin may have different indicator meanings, as set by pins LEDMODE[1:0]. When the CPU controls an LED, each pin's indicator meaning is set according to the meaning set in the corresponding register.

All LED statuses are represented as active-low or high depending on input strapping, except Bi-color Link/Act in Bi-color LED mode, whose polarity depends on Spd status.

The RTL8306G supports four parallel LEDs (Group A, B, C, D) for each port, and two special LEDs (SELMIIMAC# and LOOPLED#). Each port has four LED indicator pins. Upon reset, the RTL8306G checks LED functions by blinking all LEDs once for 320ms. This function can be disabled by asserting EN_RST_LINK to 0.

LED_BLINK_TIME determines the LED blinking period for activity and collision (1: 43ms and 0: 120ms). The parallel LEDs corresponding to port 4 can be tri-stated (disable LED functions) for MII port application by setting ENP4LED to 0. In UTP applications, this bit should be set to 1.

All LED pins are dual function pins: input operation for configuration upon reset, and output operation for LED after reset. If the pin input is floating upon reset, the pin output is active low after reset. Otherwise, if the pin input is pulled down upon reset, the pin output is active high after reset.

Exception: Bi-color Link/Act mode of pin LED_ADD[4:0] when LED Mode[1:0]=10.

For detailed descriptions of these pins, refer to Table 7, page 20, and Table 24, page 66.

The following page shows example circuits for LEDs. Typical values for pull-down resistors are 10KΩ.

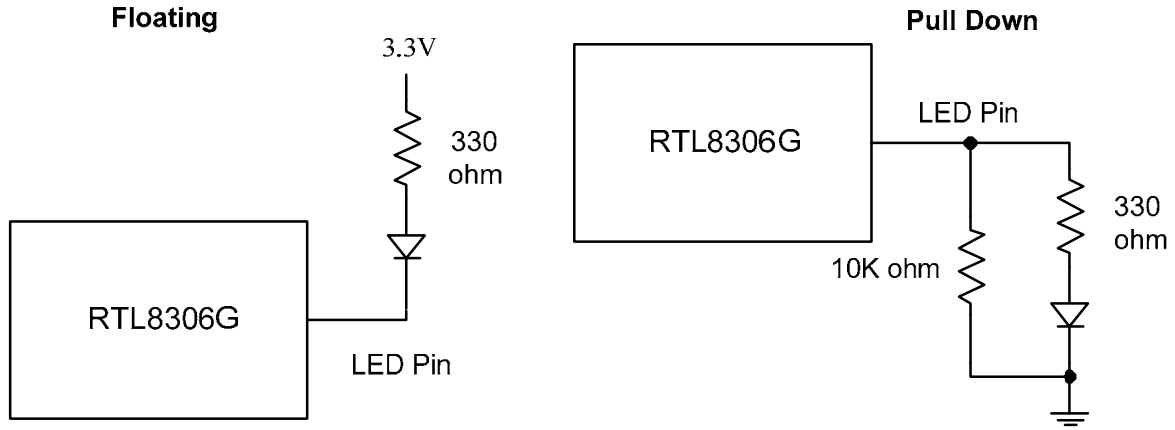


Figure 24. Floating and Pull-Down of LED Pins for Single-Color LED

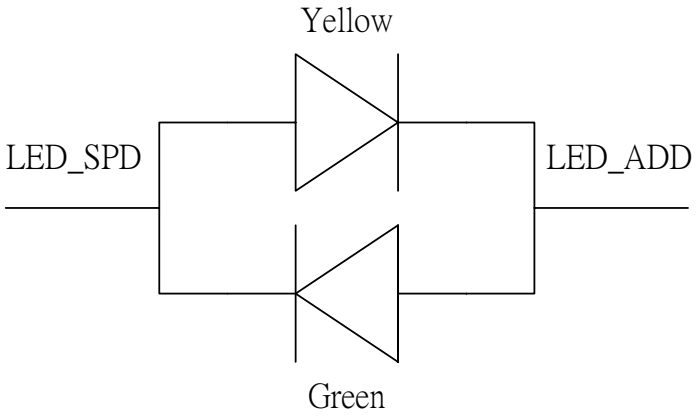


Figure 25. Two-Pin Bi-Color LED for SPD Floating or Pull-high

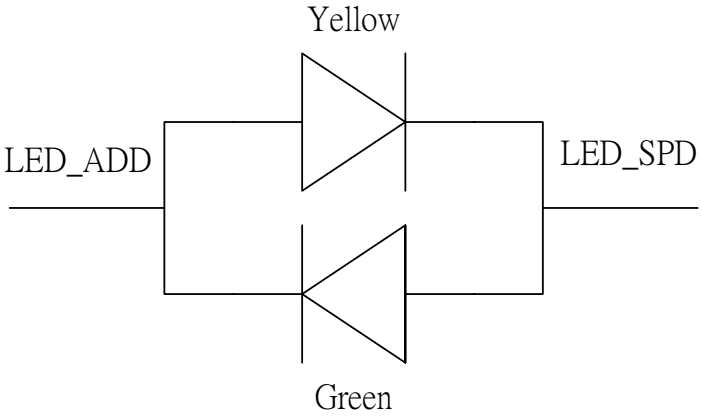


Figure 26. Two-Pin Bi-Color LED for SPD Pull-Down

Note: The polarity of the Bi-color LED should be reversed when Group B pins' input changes.

8.14.1. RTL8306G Controlling LED

For single-color LEDs, each pin may have different indicator meanings set by pins LEDMode[1:0]. For detailed descriptions, refer to Table 7, page 20, and Table 24, page 66.

For two-pin Bi-color LED mode (LEDMode[1:0]=10), Bi-color Link/Act (pin LED_ADD) and Spd (pin LED_SPD) can be used for one Bi-color LED package, which is a single LED package with two LEDs connected in parallel with opposite polarity. When LEDMode[1:0]=10, the active status of LED_ADD is the opposite of LED_SPD.

Table 24. Spd and Bi-Color Link/Act Truth Table when RTL8306G Controlling LED

Indication	Bi-Color State	Spd: Input=Floating, Active Low. Bi-color Link/Act: The active status of LED_ADD is the opposite of LED_SPD and does not interact with input upon reset.		Spd: Input=Pull-down, Active high. Bi-color Link/Act: The active status of LED_ADD is the opposite of LED_SPD and does not interact with input upon reset.	
		Spd	Link/Act	Spd	Link/Act
No Link	Both Off	0	0	0	0
		1	1	1	1
100M Link	Green On	0	1	1	0
10M Link	Yellow On	1	0	0	1
100M Act	Green Flash	0	Flash	1	Flash
10M Act	Yellow Flash	1	Flash	0	Flash

Note: '1' or '0' in table means pin output High/Low.

8.14.2. CPU Controlling LED

For single-color LED, LEDs display corresponding registers.

For two-pin Bi-color LED mode (GroupB_Control=1, GroupD_Control=1), the active status of Bi-color LEDs only depends on group B pins' input upon reset. The pin output follows the rules below:

- Group B pins input High upon reset: Register=0->Pin output High. Register=1->Pin output Low
- Group B pins input Low upon reset: Register=0->Pin output Low. Register=1->Pin output High

Table 25. Bi-Color LED Truth Table when CPU Controlling LED

Bi-Color State	Group B Register	Group D Register
Both Off	0	0
	1	1
Green On	1	0
Yellow On	0	1
Green Flash	1	Flash
Yellow Flash	0	Flash

8.15. GreenEthernet

8.15.1. Link-On and Cable Length Power Saving

The RTL8306G provides link-on and dynamic detection of cable length and dynamic adjustment of power required for the detected cable length. This feature provides high performance with minimum power consumption.

8.15.2. Link-Down Power Saving

The RTL8306G implements link-down power saving on a per-port basis, greatly cutting power consumption when the network cable is disconnected.

9. Register Descriptions

9.1. Register List

For PHY configuration, register 0~5 in PHY 0~4 are used for the 1st~5th PHY.

Register 0~5 in PHY 5 ~ 6 are used for the 5th and 6th MAC when Dual MII is enabled.

In this section the following abbreviations are used:

RO: Read Only
RW: Read/Write
LL: Latch Low until clear
LH: Latch High until clear
SC: Self Clearing

Table 26. Register Descriptions

Name	PHY	Page	Register	Register Description	Default
Port 0 PHY Register	0	0, 1, 2, 3	0	Control Register	0x3100
			1	Status Register	0x7849
			2	PHY Identifier 1	0x001C
			3	PHY Identifier 2	0xC852
			4	Auto-Negotiation Advertisement Register	0x05E1
			5	Auto-Negotiation Link Partner Ability Register	0x0001
			16	Global Control Register 0	0x07FA
		0, 1	18	Global Control Register 2	0x7FFF
			19	Global Control Register 3	0xFFFF
			22	Port 0 Control Register 0	0x877F
			24	Port 0 Control Register 1	0x0ED1
Port 1 PHY Register	1	0, 1, 2, 3	0	Control Register	0x3100
			1	Status Register	0x7849
			2	PHY Identifier 1	0x001C
			3	PHY Identifier 2	0xC852
			4	Auto-Negotiation Advertisement Register	0x05E1
			5	Auto-Negotiation Link Partner Ability Register	0x0001
		0, 1	22	Port 1 Control Register 0	0x877F
			24	Port 1 Control Register 1	0x1ED2
Port 2 PHY Register	2	0, 1, 2, 3	0	Control Register	0x3100
			1	Status Register	0x7849
			2	PHY Identifier 1	0x001C
			3	PHY Identifier 2	0xC852
			4	Auto-Negotiation Advertisement Register	0x05E1
			5	Auto-Negotiation Link Partner Ability Register	0x0001
		0, 1	22	Port 2 Control Register 0	0x877F
			23	Global Option Register 1	0x0020
			24	Port 2 Control Register 1	0x2ED4

Name	PHY	Page	Register	Register Description	Default
Port 3 PHY Register	3	0, 1, 2, 3	0	Control Register	0x3100
			1	Status Register	0x7849
			2	PHY Identifier 1	0x001C
			3	PHY Identifier 2	0xC852
			4	Auto-Negotiation Advertisement Register	0x05E1
			5	Auto-Negotiation Link Partner Ability Register	0x0001
			16	Switch MAC Address	0x5452
		0, 1	17	Switch MAC Address	0x834C
			18	Switch MAC Address	0xC005
			22	Port 3 Control Register 0	0x877F
			24	Port 3 Control Register 1	0x3ED8
Port 4 PHY Register	4	0, 1, 2, 3	0	Control Register	0x3100
			1	Status Register	0x7849
			2	PHY Identifier 1	0x001C
			3	PHY Identifier 2	0xC852
			4	Auto-Negotiation Advertisement Register	0x05E1
			5	Auto-Negotiation Link Partner Ability Register	0x0001
		0, 1	22	Port 4 Control Register 0	0x877F
			24	Port 4 Control Register 1	0x4EDF
PHY Register for Port 4 MAC	5	0, 1, 2, 3	0	Control Register	0x3100
			1	Status Register	0x7869
			2	PHY Identifier 1	0x001C
			3	PHY Identifier 2	0xC852
			4	Auto-Negotiation Advertisement Register	0x05E1
			5	Auto-Negotiation Link Partner Ability Register	0x05E1
PHY Register for Port 5 MAC	6	0, 1, 2, 3	0	Control Register	0x2100
			1	Status Register	0x7869
			2	PHY Identifier 1	0x001C
			3	PHY Identifier 2	0xC852
			4	Auto-Negotiation Advertisement Register	0x05E1
			5	Auto-Negotiation Link Partner Ability Register	0x05E1
		0, 1	22	Port 5 Control Register 0	0x073F
			24	Port 5 Control Register 1	0x8EFF

9.2. PHY 0 Registers

9.2.1. PHY 0 Register 0 (Page 0, 1, 2, 3): Control

Table 27. PHY 0 Register 0 (Page 0, 1, 2, 3): Control

Reg.bit	Name	Mode	Description	Default
0.15	Reset	RW/SC	1: PHY reset. This bit is self-clearing.	0
0.14	Loopback (Digital loopback)	RW	1: Enable loopback. This will loopback TXD to RXD and ignore all activity on the cable media 0: Normal operation This function is usable only when this PHY is operated in 10Base-T full duplex or 100Base-TX full duplex.	0
0.13	Speed Select	RW	1: 100Mbps 0: 10Mbps When NWay is enabled, this bit reflects the result of auto-negotiation (Read only). When NWay is disabled, this bit can be set through SMI. (Read/Write).	From pin 107 GxSpd100 strapping option, default 1
0.12	Auto Negotiation Enable	RW	1: Enable auto-negotiation process 0: Disable auto-negotiation process This bit can be set through SMI (Read/Write).	From pin 104 GxANEG strapping option, default 1
0.11	Power Down	RW	1: Power down. All functions will be disabled except SMI function 0: Normal operation	0
0.10	Isolate	RW	1: Electrically isolates the PHY from MII. PHY is still able to respond to MDC/MDIO 0: Normal operation	0
0.9	Restart Auto Negotiation	RW/SC	1: Restart Auto-Negotiation process 0: Normal operation	0
0.8	Duplex Mode	RW	1: Full duplex operation 0: Half duplex operation When NWay is enabled (Reg0.12=1), this bit reflects the result of auto-negotiation (Read only). When NWay is disabled (Reg0.12=0, force mode of UTP), this bit can be set through SMI (Read/Write).	From pin 109 strapping option, default 1
0.[7:0]	Reserved	-	-	0000 0000

9.2.2. PHY 0 Register 1 (Page 0, 1, 2, 3): Status

Table 28. PHY 0 Register 1 (Page 0, 1, 2, 3): Status

Reg.bit	Name	Mode	Description	Default
1.15	100Base_T4	RO	0: No 100Base-T4 capability	0
1.14	100Base_TX_FD	RO	1: 100Base-TX full duplex capable 0: Not 100Base-TX full duplex capable	1
1.13	100Base_TX_HD	RO	1: 100Base-TX half duplex capable 0: Not 100Base-TX half duplex capable	1
1.12	10Base_T_FD	RO	1: 10Base-TX full duplex capable 0: Not 10Base-TX full duplex capable	1
1.11	10Base_T_HD	RO	1: 10Base-TX half duplex capable 0: Not 10Base-TX half duplex capable	1
1.[10:7]	Reserved	RO	Reserved.	0000
1.6	MF Preamble Suppression	RO	The RTL8306G will accept management frames with preamble suppressed. (The RTL8306G accepts management frames without preamble. 32 minimum preamble bits are required for the first SMI read/write transaction after reset. One idle bit is required between any two management transactions as defined in IEEE 802.3u).	1
1.5	Auto-negotiate Complete	RO	1: Auto-negotiation process completed. MII Reg.4 and 5 are valid if this bit is set 0: Auto-negotiation process not completed	0
1.4	Remote Fault	RO/LH	1: Remote fault condition detected 0: No remote fault	0
1.3	Auto-Negotiation Ability	RO	1: NWay auto-negotiation capable (permanently =1)	1
1.2	Link Status	RO/LL	1: Link is established. If the link fails, this bit will be 0 until after reading this bit again 0: Link has failed	0
1.1	Jabber Detect	RO/LH	0: No Jabber detected RTL8306G does not support this function	0
1.0	Extended Capability	RO	1: Extended register capable (permanently =1)	1

9.2.3. PHY 0 Register 2 (Page 0, 1, 2, 3): PHY Identifier 1

Table 29. PHY 0 Register 2 (Page 0, 1, 2, 3): PHY Identifier 1

Reg.bit	Name	Mode	Description	Default
2.[15:0]	OUI	RO	Composed of the 3rd to 18th bits of the Organizationally Unique Identifier (OUI), respectively.	0x001C

9.2.4. PHY 0 Register 3 (Page 0, 1, 2, 3): PHY Identifier 2

Table 30. PHY 0 Register 3 (Page 0, 1, 2, 3): PHY Identifier 2

Reg.bit	Name	Mode	Description	Default
3.[15:10]	OUI	RO	Assigned to the 19th through 24th bits of the Organizationally Unique Identifier (OUI).	110010
3.[9:4]	Model Number	RO	Manufacturer's model number 05.	000101
3.[3:0]	Revision Number	RO	Manufacturer's revision number 02.	0010

9.2.5. PHY 0 Register 4 (Page 0, 1, 2, 3): Auto-Negotiation Advertisement

Table 31. PHY 0 Register 4 (Page 0, 1, 2, 3): Auto-Negotiation Advertisement

Reg.bit	Name	Mode	Description	Default
4.15	Next Page	RO	1: Next Page enabled 0: Next Page disabled (Permanently =0)	0
4.14	Acknowledge	RO	Permanently =0	0
4.13	Remote Fault	RW	1: Advertises that the RTL8306G has detected a remote fault 0: No remote fault detected	0
4.12	Reserved	RO	Reserved.	0
4.11	Asym Pause	RW	1: Enable Asymmetric Pause 0: Disable Asymmetric Pause	0
4.10	Pause	RW	1: Advertises that the RTL8306G possesses 802.3x flow control capability 0: No flow control capability	From pin 76 strapping option, default 1
4.9	100Base-T4	RO	Technology not supported (Permanently =0)	0
4.8	100Base-TX-FD	RW	1: 100Base-TX full duplex capable 0: Not 100Base-TX full duplex capable	From pin 107, 109 strapping option
4.7	100Base-TX	RW	1: 100Base-TX half duplex capable 0: Not 100Base-TX half duplex capable	From pin 107, 109 strapping option
4.6	10Base-T-FD	RW	1: 10Base-TX full duplex capable 0: Not 10Base-TX full duplex capable	From pin 107, 109 strapping option
4.5	10Base-T	RW	1: 10Base-TX half duplex capable 0: Not 10Base-TX half duplex capable	1
4.[4:0]	Selector Field	RW	[00001]=IEEE 802.3	00001

9.2.6. PHY 0 Register 5 (Page 0, 1, 2, 3): Auto-Negotiation Link Partner Ability

Table 32. PHY 0 Register 5 (Page 0, 1, 2, 3): Auto-Negotiation Link Partner Ability

Reg.bit	Name	Mode	Description	Default
5.15	Next Page	RO	1: Link partner desires Next Page transfer 0: Link partner does not desire Next Page transfer	0
5.14	Acknowledge	RO	1: Link Partner acknowledges reception of Fast Link Pulse (FLP) words 0: Not acknowledged by Link Partner	0
5.13	Remote Fault	RO	1: Remote Fault indicated by Link Partner 0: No remote fault indicated by Link Partner	0
5.12	Reserved	RO	Reserved.	0
5.11	Asym Pause	RO	1: Enable Asymmetric Pause 0: Disable Asymmetric Pause	0
5.10	Pause	RO	1: Flow control supported by Link Partner 0: Flow control not supported by Link Partner	0
5.9	100Base-T4	RO	1: 100Base-T4 supported by Link Partner 0: 100Base-T4 not supported by Link Partner	0
5.8	100Base-TX-FD	RO	1: 100Base-TX full duplex supported by Link Partner 0: 100Base-TX full duplex not supported by Link Partner When auto negotiation is disabled, this bit will be set if Reg0.13=1 and Reg0.8=1after link is established.	0
5.7	100Base-TX	RO	1: 100Base-TX half duplex supported by Link Partner 0: 100Base-TX half duplex not supported by Link Partner When auto negotiation is disabled, this bit will be set if Reg0.13=1 and Reg0.8=0after link is established.	0
5.6	10Base-T-FD	RO	1: 10Base-TX full duplex supported by Link Partner 0: 10Base-TX full duplex not supported by Link Partner When auto negotiation is disabled, this bit will be set if Reg0.13=0 and Reg0.8=1after link is established.	0
5.5	10Base-T	RO	1: 10Base-TX half duplex supported by Link Partner 0: 10Base-TX half duplex not supported by Link Partner. When auto negotiation is disabled, this bit will be set if Reg0.13=0 and Reg0.8=0after link is established.	0
5.[4:0]	Selector Field	RO	[00001]=IEEE 802.3	00001

9.2.7. PHY 0 Register 16 (Page 0, 1, 2, 3): Global Control 0

Table 33. PHY 0 Register 16 (Page 0, 1, 2, 3): Global Control 0

Reg.bit	Name	Mode	Description	Default
16.15	Page selection (Selpage)	RW	[~16.1 16.15] 00: Select the registers in page 0 01: Select the registers in page 1 10: Select the registers in page 2 11: Select the registers in page 3	0
16.[14:8]	Reserved	-	Reserved.	0000111
16.7	EEPROM existence	RO	1: EEPROM does not exist. (pin EnEEPROM=0 or pin EnEEPROM=1 but EEPROM does not exist) 0: EEPROM exists (pin EnEEPROM=1 and EEPROM exists)	From Pin 73 ENEEPROM strapping option, default 1
16.6	Reserved	-	Reserved.	1
16.5	IEEE 802.3x transmit flow control enable	RW	1: Enable transmit flow control based on auto-negotiation results 0: Will not enable transmit flow control no matter what the auto-negotiation result is *Note: This bit is global and has higher priority than NWay result.*	1
16.4	IEEE 802.3x receive flow control enable	RW	1: When the RTL8306G receives a pause control frame, it has the ability to stop the next transmission of a normal frame until the timer is expired based on the auto negotiation result 0: Will not flow control received frames no matter what the auto-negotiation result is *Note: This bit is global and has higher priority than NWay result.*	1
16.3	Enable port 4 LED	RW	1: Drive LED pin of port 4 0: Do not drive LED pins of port 4 for special application. In UTP application, this bit should be set to 1 to drive LEDs of port 4.	1
16.2	Enable loop detection function	RW	1: Enable loop detection function 0: Disable loop detection function	0
16.1	Page selection (Selpage)	RW	[~16.1 16.15] 00: Select the registers in page 0 01: Select the registers in page 1 10: Select the registers in page 2 11: Select the registers in page 3	1
16.0	Reserved	-	Reserved.	0

9.2.8. PHY 0 Register 18 (Page 0, 1): Global Control 2

Table 34. PHY 0 Register 18 (Page 0, 1): Global Control 2

Reg.bit	Name	Mode	Description	Default
18.15	Reserved	-	Reserved.	0
18.14	Maximum Frame Length	RW	1: 1536 Byte 0: 1552 Byte	Pin 114 Max1536 strap option Default=1
18.[13:10]	Reserved	-	Reserved.	1111
18.9	Enable 48 pass 1	RW	1: 48 pass 1, continuously collides 48 input packets then passes 1 packet to retain system resource and avoid partition in the repeater when the packet buffer is full 0: Continuously collides to avoid packet loss when the packet buffer is full	Pin 97 En48pass1 strap option Default=1
18.8	Reserved	-	Reserved.	1
18.7	Disable HomePlug	RW	1: Disable HomePlug: Use input RXDV as CRS of Port4MII 0: Enable HomePlug: Use input pin 48 P4FULL as CRS of Port4MII	Pin 92 DISHOMEPLUG strap option Default=1
18.6	Enable defer	RW	1: Enable carrier sense deferring for half duplex back pressure 0: Disable carrier sense deferring for half duplex back pressure	Pin 90 EnDefer strap option Default=1
18.5	LED blink time	RW	1: On 43ms, then Off 43ms 0: On 120ms, then Off 120ms	Pin 89 LED_BLNK_TIME strap option Default=1
18.[4:2]	Reserved	-	Reserved.	111
18.1	Enable power-on blinking	RW	1: Enable power-on LED blinking for diagnosis 0: Disable power-on LED blinking for diagnosis	Pin 71 En_Rst_Blnk strap option Default=1
18.0	Reserved	-	Reserved.	1

9.2.9. PHY 0 Register 19 (Page 0, 1): Global Control 3

Table 35. PHY 0 Register 19 (Page 0,1): Global Control 3

Reg.bit	Name	Mode	Description	Default
19.[15:14]	Reserved	-	Reserved.	11
19.[13:12]	LED Mode[1:0]	RW	11: Mode 3: Speed, Link+Act, Duplex+Col, Link/Act/Speed 10: Mode 2: Speed, Act, Duplex/Col, Bi-color Link/Activity 01: Mode 1: Speed, RxAct, TxAct, Link 00: Mode 0: Duplex+Speed+Col+Bi-color Link/Act	Pin 55, 54 LEDMode[1:0] strap option Default = 11
19.11	Reserved	-	Reserved.	1
19.[10:0]	Reserved	-	Reserved.	111 11111111

9.2.10. PHY 0 Register 22 (Page 0, 1): Port 0 Control Register 0

Table 36. PHY 0 Register 22 (Page 0, 1): Port 0 Control Register 0

Reg.bit	Name	Mode	Description	Default
22.15	Reserved	-	Reserved.	1
22.14	Reserved	-	Reserved.	0
22.13	Port 0 Local loopback	RW	1: Perform 'local loopback', i.e. loop MAC's RX back to TX 0: Normal operation	0
22.[12:11]	Reserved	-	Reserved.	00
22.10	Port 0 802.1p priority Disable	RW	1: Disable 802.1p priority classification for ingress packets on port 0 0: Enable 802.1p priority classification	Pin 91 DisTagPri strap option Default = 1
22.9	Port 0 Diffserv priority Disable	RW	1: Disable Diffserv priority classification for ingress packets on port 0 0: Enable Diffserv priority classification	Pin 68 DisDSPri strap option Default = 1
22.8	Port 0 port-based priority Disable	RW	1: Disable port based priority QoS function on port 0 0: Enable port based priority QoS function on port 0. Ingress packet on port 0 will be classified as high priority	Pin 83 DisPortPri[0]strap option Default = 1
22.7	SetAsym0	RW	Same as the Register 4.11	0
22.6	Port 0 auto negotiation Enable	RW	1: Enable port 0 auto negotiation 0: Disable port 0 auto negotiation, the speed and duplex are decided by bit 5 and 4 of this register	From pin 104 GxANEG strapping option, default 1
22.[5:4]	Port 0 Speed and Duplex ability	RW	In Auto-negotiation mode: 11: MII Reg.0.8=1, 0.13=1, 4.8=1, 4.7=1, 4.6=1, 4.5=1 10: MII Reg.0.8=0, 0.13=1, 4.8=0, 4.7=1, 4.6=1, 4.5=1 01: MII Reg.0.8=1, 0.13=0, 4.8=0, 4.7=0, 4.6=1, 4.5=1 00: MII Reg.0.8=0, 0.13=0, 4.8=0, 4.7=0, 4.6=0, 4.5=1 In Force mode: 11: MII Reg0.8=1, 0.13=1, 4.8=1, 4.7=0, 4.6=0, 4.5=0 10: MII Reg0.8=0, 0.13=1, 4.8=0, 4.7=1, 4.6=0, 4.5=0 01: MII Reg0.8=1, 0.13=0, 4.8=0, 4.7=0, 4.6=1, 4.5=0 00: MII Reg0.8=0, 0.13=0, 4.8=0, 4.7=0, 4.6=0, 4.5=1	From pin 107, 109 strapping option
22.3	Port 0 802.3x flow control ability Enable	RW	1: Enable port 0 full duplex flow control ability 0: Disable port 0 full duplex flow control ability	From pin 76 GxENFC strapping option default 1
22.2	Port 0 Backpressure Enable	RW	1: Enable port 0 half duplex backpressure 0: Disable port 0 half duplex backpressure	From pin 78 ENBKPRS strapping option
22.[1:0]	Reserved	-	Reserved.	11

9.2.11. PHY 0 Register 24 (Page 0, 1): Port 0 Control Register 1

Table 37. PHY 0 Register 24 (Page 0,1): Port 0 Control Register 1

Reg.bit	Name	Mode	Description	Default
24.[15:12]	Reserved	-	Reserved.	0000
24.11	Port 0 Transmission Enable	RW	1: Enable packet transmission on port 0 0: Disable packet transmission on port 0	1
24.10	Port 0 Reception Enable	RW	1: Enable packet reception on port 0 0: Disable packet reception on port 0	1
24.9	Port 0 Learning Enable	RW	1: Enable switch address learning capability 0: Disable switch address learning capability	1
24.8	Port 0 Loop Status	RO	1: A loop has been detected on port 0 0: No loop exists on port 0	0
24.7	Port 0 Auto Crossover Enable	RW	1: Enable auto crossover detection of port 0 0: Disable auto crossover detection of port 0	Pin 69 En_AutoXover strap option Default = 1
24.6	Port 0 MDI or MDIX Select	RW	1: Medium interface of port 0 is MDI when auto crossover detection is disabled 0: Medium interface of port 0 is MDIX when auto crossover detection is disabled	1
24.[5:0]	Reserved	-	Reserved.	01 0001

9.3. PHY 1 Registers

9.3.1. PHY 1 Register 0 (Page 0, 1, 2, 3): Control

This register has the same definition as PHY 0 Register 0 (Page 0, 1, 2, 3): Control, page 70.

9.3.2. PHY 1 Register 1 (Page 0, 1, 2, 3): Status

This register has the same definition as PHY 0 Register 1 (Page 0, 1, 2, 3): Status, page 71.

9.3.3. PHY 1 Register 2 (Page 0, 1, 2, 3): PHY Identifier 1

This register has the same definition as PHY 0 Register 2 (Page 0, 1, 2, 3): PHY Identifier 1, page 71.

9.3.4. PHY 1 Register 3 (Page 0, 1, 2, 3): PHY Identifier 2

This register has the same definition as PHY 0 Register 3 (Page 0, 1, 2, 3): PHY Identifier 2, page 72.

9.3.5. PHY 1 Register 4 (Page 0, 1, 2, 3): Auto-Negotiation Advertisement

This register has the same definition as PHY 0 Register 4 (Page 0, 1, 2, 3): Auto-Negotiation Advertisement, page 72.

9.3.6. PHY 1 Register 5 (Page 0, 1, 2, 3): Auto-Negotiation Link Partner Ability

This register has the same definition as PHY 0 Register 5 (Page 0, 1, 2, 3): Auto-Negotiation Link Partner Ability, page 73.

9.3.7. PHY 1 Register 22 (Page 0, 1): Port 1 Control Register 0

This register has the same definition as PHY 0 Register 22 (Page 0, 1): Port 0 Control Register 0, page 76.

Note: Reg 22.8 is pin DisPortPri[1] strap option for port 1. Default value for 22.8 is 1.

9.3.8. PHY 1 Register 24 (Page 0, 1): Port 1 Control Register 1

Table 38. PHY 1 Register 24 (Page 0, 1): Port 1 Control Register 1

Reg.bit	Name	Mode	Description	Default
24.[15:12]	Reserved	-	Reserved.	0001
24.11	Port 1 Transmission Enable	RW	1: Enable packet transmission on port 1 0: Disable packet transmission on port 1	1
24.10	Port 1 Reception Enable	RW	1: Enable packet reception on port 1 0: Disable packet reception on port 1	1
24.9	Port 1 Learning Enable	RW	1: Enable switch address learning capability 0: Disable switch address learning capability	1
24.8	Port 1 Loop Status	RO	1: A loop has been detected on port 1 0: No loop exists on port 1	0
24.7	Port 1 auto crossover Enable	RW	1: Enable auto crossover detection of port 1 0: Disable auto crossover detection of port 1	Pin 69 strapping option Default = 1
24.6	Port 1 MDI or MDIX Select	RW	1: Medium interface of port 1 is MDI when auto crossover detection is disabled 0: Medium interface of port 1 is MDIX when auto crossover detection is disabled	1
24.[5:0]	Reserved	-	Reserved.	01 0010

9.4. PHY 2 Registers

9.4.1. PHY 2 Register 0 (Page 0, 1, 2, 3): Control

This register has the same definition as PHY 0 Register 0 (Page 0, 1, 2, 3): Control, page 70.

9.4.2. PHY 2 Register 1 (Page 0, 1, 2, 3): Status

This register has the same definition as PHY 0 Register 1 (Page 0, 1, 2, 3): Status, page 71.

9.4.3. PHY 2 Register 2 (Page 0, 1, 2, 3): PHY Identifier 1

This register has the same definition as PHY 0 Register 2 (Page 0, 1, 2, 3): PHY Identifier 1, page 71.

9.4.4. PHY 2 Register 3 (Page 0, 1, 2, 3): PHY Identifier 2

This register has the same definition as PHY 0 Register 3 (Page 0, 1, 2, 3): PHY Identifier 2, page 72.

9.4.5. PHY 2 Register 4 (Page 0, 1, 2, 3): Auto-Negotiation Advertisement

This register has the same definition as PHY 0 Register 4 (Page 0, 1, 2, 3): Auto-Negotiation Advertisement, page 72.

9.4.6. PHY 2 Register 5 (Page 0, 1, 2, 3): Auto-Negotiation Link Partner Ability

This register has the same definition as PHY 0 Register 5 (Page 0, 1, 2, 3): Auto-Negotiation Link Partner Ability, page 73.

9.4.7. PHY 2 Register 22 (Page 0, 1): Port 1 Control Register 0

This register has the same definition as PHY 0 Register 22 (Page 0, 1): Port 0 Control Register 0, page 76.

Note: Reg 22.8 is pin DisPortPri[1] strap option for port 1. Default value for 22.8 is 1.

9.4.8. PHY 2 Register 23 (Page 0, 1): Global Option Register 1

Table 39. PHY 2 Register 23 (Page 0,1): Global Option Register 1

Reg.bit	Name	Mode	Description	Default
23.[15]	FixIFG	RW	0: InterFrame Gap (IFG) compensation 1: Fix IFG to 96-bit	0
23.[14:0]	Reserved	-	Reserved.	0000000100000

9.4.9. PHY 2 Register 24 (Page 0, 1): Port 2 Control Register 2

Table 40. PHY 2 Register 24 (Page 0, 1): Port 2 Control Register 2

Reg.bit	Name	Mode	Description	Default
24.[15:12]	Reserved	-	Reserved.	0010
24.11	Port 2 Transmission Enable	RW	1: Enable packet transmission on port 2 0: Disable packet transmission on port 2	1
24.10	Port 2 Reception Enable	RW	1: Enable packet reception on port 2 0: Disable packet reception on port 2	1
24.9	Port 2 Learning Enable	RW	1: Enable switch address learning capability 0: Disable switch address learning capability	1
24.8	Port 2 Loop Status	RO	1: A loop has been detected on port 2 0: No loop exists on port 2	0
24.7	Port 2 auto crossover Enable (EnAutoMDIX)	RW	1: Enable auto crossover detection of port 2 0: Disable auto crossover detection of port 2	Pin 69 strapping option Default = 1
24.6	Port 2 MDI or MDIX Select (SELMDI)	RW	1: Medium interface of port 2 is MDI when auto crossover detection is disabled 0: Medium interface of port 2 is MDIX when auto crossover detection is disabled	1
24.[5:0]	Reserved	-	Reserved.	01 0100

9.5. PHY 3 Registers

9.5.1. PHY 3 Register 0 (Page 0, 1, 2, 3): Control

This register has the same definition as PHY 0 Register 0 (Page 0, 1, 2, 3): Control, page 70.

9.5.2. PHY 3 Register 1 (Page 0, 1, 2, 3): Status

This register has the same definition as PHY 0 Register 1 (Page 0, 1, 2, 3): Status, page 71.

9.5.3. PHY 3 Register 2 (Page 0, 1, 2, 3): PHY Identifier 1

This register has the same definition as PHY 0 Register 2 (Page 0, 1, 2, 3): PHY Identifier 1, page 71.

9.5.4. PHY 3 Register 3 (Page 0, 1, 2, 3): PHY Identifier 2

This register has the same definition as PHY 0 Register 3 (Page 0, 1, 2, 3): PHY Identifier 2, page 72.

9.5.5. PHY 3 Register 4 (Page 0, 1, 2, 3): Auto-Negotiation Advertisement

This register has the same definition as PHY 0 Register 4 (Page 0, 1, 2, 3): Auto-Negotiation Advertisement, page 72.

9.5.6. PHY 3 Register 5 (Page 0, 1, 2, 3): Auto-Negotiation Link Partner Ability

This register has the same definition as PHY 0 Register 5 (Page 0, 1, 2, 3): Auto-Negotiation Link Partner Ability, page 73.

9.5.7. PHY 3 Register 16 (Page 0, 1, 2, 3): Switch MAC Address

Table 41. PHY 3 Register 16 (Page 0, 1, 2, 3): Switch MAC Address

Reg.bit	Name	Mode	Description	Default
16	Switch MAC Address [47:32]	RW	16.[15:8] = Switch MAC Address Byte 4 16.[7:0] = Switch MAC Address Byte 5	0x5452

9.5.8. PHY 3 Register 17~18 (Page 0, 1): Switch MAC Address

Table 42. PHY 3 Register 17~18 (Page 0, 1): Switch MAC Address

Reg.bit	Name	Mode	Description	Default
17	Switch MAC Address [31:16]	RW	17.[15:8] = Switch MAC Address Byte 2 17.[7:0] = Switch MAC Address Byte 3	0x834C
18	Switch MAC Address [15:0]	RW	18.[15:8] = Switch MAC Address Byte 0 18.[7:0] = Switch MAC Address Byte 1	0xC005

9.5.9. PHY 3 Register 22 (Page 0, 1): Port 1 Control Register 0

This register has the same definition as PHY 0 Register 22 (Page 0, 1): Port 0 Control Register 0, page 76.

Note: Reg 22.8 is pin DisPortPri[1] strap option for port 1. Default value for 22.8 is 1.

9.5.10. PHY 3 Register 24 (Page 0, 1): Port 3 Control Register 1

Table 43. PHY 3 Register 24 (Page 0, 1): Port 3 Control Register 1

Reg.bit	Name	Mode	Description	Default
24.[15:12]	Reserved	-	Reserved.	0011
24.11	Port 3 Transmission Enable	RW	1: Enable packet transmission on port 3 0: Disable packet transmission on port 3	1
24.10	Port 3 Reception Enable	RW	1: Enable packet reception on port 3 0: Disable packet reception on port 3	1
24.9	Port 3 Learning Enable	RW	1: Enable switch address learning capability 0: Disable switch address learning capability	1
24.8	Port 3 Loop Status	RO	1: A loop has been detected on port 3 0: No loop exists on port 3	0
24.7	Port 3 auto crossover Enable	RW	1: Enable auto crossover detection of port 3 0: Disable auto crossover detection of port 3	Pin 69 strapping option Default = 1
24.6	Port 3 MDI or MDIX Select	RW	1: Medium interface of port 3 is MDI when auto crossover detection is disabled 0: Medium interface of port 3 is MDIX when auto crossover detection is disabled	1
24.[5:0]	Reserved	-	Reserved.	01 1000

9.6. PHY 4 Registers

9.6.1. PHY 4 Register 0 (Page 0, 1, 2, 3): Control

This register has the same definition as PHY 0 Register 0 (Page 0, 1, 2, 3): Control, page 70.

9.6.2. PHY 4 Register 1 (Page 0, 1, 2, 3): Status

This register has the same definition as PHY 0 Register 1 (Page 0, 1, 2, 3): Status, page 71.

9.6.3. PHY 4 Register 2 (Page 0, 1, 2, 3): PHY Identifier 1

This register has the same definition as PHY 0 Register 2 (Page 0, 1, 2, 3): PHY Identifier 1, page 71.

9.6.4. PHY 4 Register 3 (Page 0, 1, 2, 3): PHY Identifier 2

This register has the same definition as PHY 0 Register 3 (Page 0, 1, 2, 3): PHY Identifier 2, page 72.

9.6.5. PHY 4 Register 4 (Page 0, 1, 2, 3): Auto-Negotiation Advertisement

This register has the same definition as PHY 0 Register 4 (Page 0, 1, 2, 3): Auto-Negotiation Advertisement, page 72.

9.6.6. PHY 4 Register 5 (Page 0, 1, 2, 3): Auto-Negotiation Link Partner Ability

This register has the same definition as PHY 0 Register 5 (Page 0, 1, 2, 3): Auto-Negotiation Link Partner Ability, page 73.

9.6.7. PHY 4 Register 22 (Page 0, 1): Port 1 Control Register 0

This register has the same definition as PHY 0 Register 22 (Page 0, 1): Port 0 Control Register 0, page 76.

Note: Reg 22.8 is pin DisPortPri[1] strap option for port 1. Default value for 22.8 is 1.

9.6.8. PHY 4 Register 24 (Page 0, 1): Port 4 Control Register 1

Table 44. PHY 4 Register 24 (Page 0, 1): Port 4 Control Register 1

Reg.bit	Name	Mode	Description	Default
24.[15:12]	Reserved	-	Reserved.	0100
24.11	Port 4 Transmission Enable	RW	1: Enable packet transmission on port 4 0: Disable packet transmission on port 4	1
24.10	Port 4 Reception Enable	RW	1: Enable packet reception on port 4 0: Disable packet reception on port 4	1
24.9	Port 4 Learning Enable	RW	1: Enable switch address learning capability 0: Disable switch address learning capability	1
24.8	Port 4 Loop Status	RO	1: A loop has been detected on port 4 0: No loop exists on port 4	0
24.7	Port 4 auto crossover Enable (EnAutoMDIX)	RW	1: Enable auto crossover detection of port 4 0: Disable auto crossover detection of port 4	Pin 69 strapping option; Default=1
24.6	Port 4 MDI or MDIX Select (SELMDI)	RW	1: Medium interface of port 4 is MDI when auto crossover detection is disabled 0: Medium interface of port 4 is MDIX when auto crossover detection is disabled	1
24.[5:0]	Reserved	-	Reserved.	01 1111

9.7. PHY 5 Registers

9.7.1. PHY 5 Register 0 (Page 0, 1, 2, 3): Control

Table 45. PHY 5 Register 0 (Page 0, 1, 2, 3): Control

Reg.bit	Name	Mode	Description	Default
0.15	Reset	RO	0: No reset allowed (permanently =0)	0
0.14	Loopback (digital loopback)	RO	0: Normal operation (permanently =0)	0
0.13	Speed Select	RW	1: 100Mbps 0: 10Mbps When NWay is enabled, this bit reflects the result of auto-negotiation (Read only). When NWay is disabled, this bit can be set through SMI (Read/Write).	Pin 47 P4SPDSTA strap option default 1
0.12	Auto Negotiation Enable	RW	1: Enable auto-negotiation process 0: Disable auto-negotiation process This bit can be set through SMI (Read/Write).	Pin 103 P4ANEG strap option
0.11	Power Down	RO	0: Normal operation (permanently =0)	0
0.10	Isolate	RO	0: Normal operation (permanently =0)	0
0.9	Restart Auto Negotiation	RO	0: Normal operation (permanently =0)	0
0.8	Duplex Mode	RW	1: Full duplex operation 0: Half duplex operation When NWay is enabled, this bit reflects the result of auto-negotiation (Read only). When NWay is disabled, this bit may be set through SMI (Read/Write).	Pin 48 P4DUPSTA strap option, default 1
0.[7:0]	Reserved	-	Reserved.	0000 0000

9.7.2. PHY 5 Register 1 (Page 0, 1, 2, 3): Status

Table 46. PHY 5 Register 1 (Page 0, 1, 2, 3): Status

Reg.bit	Name	Mode	Description	Default
1.15	100Base_T4	RO	0: No 100Base-T4 capability	0
1.14	100Base_TX_FD	RO	1: 100Base-TX full duplex capable (permanently =1)	1
1.13	100Base_TX_HD	RO	1: 100Base-TX half duplex capable (permanently =1)	1
1.12	10Base_T_FD	RO	1: 10Base-TX full duplex capable (permanently =1)	1
1.11	10Base_T_HD	RO	1: 10Base-TX half duplex capable (permanently =1)	1
1.[10:7]	Reserved	RO	Reserved.	0000
1.6	MF Preamble Suppression	RO	The RTL8306G will accept management frames with preamble suppressed (permanently =1).	1
1.5	Auto-negotiate Complete	RO	1: Auto-negotiation process completed. MII Reg.4, 5 are valid if this bit is set (permanently =1)	1
1.4	Remote Fault	RO	0: No remote fault (permanently =0)	0
1.3	Auto-Negotiation Ability	RO	1: NWay auto-negotiation capable (permanently =1)	1
1.2	Link Status	RO	1: Link is established 0: Link is failed This bit reflects the status of pin P4LNKSTA# in real time.	Pin 49 P4LNKSTA# strap option default 0
1.1	Jabber Detect	RO	0: No Jabber detected (permanently =0)	0
1.0	Extended Capability	RO	1: Extended register capable (permanently =1)	1

9.7.3. PHY 5 Register 2 (Page 0, 1, 2, 3): PHY Identifier 1

Table 47. PHY 5 Register 2 (Page 0, 1, 2, 3): PHY Identifier 1

Reg.bit	Name	Mode	Description	Default
2.[15:0]	OUI	RO	Composed of the 3rd to 18th bits of the Organizationally Unique Identifier (OUI), respectively.	0x001C

9.7.4. PHY 5 Register 3 (Page 0, 1, 2, 3): PHY Identifier 2

Table 48. PHY 5 Register 3 (Page 0, 1, 2, 3): PHY Identifier 2

Reg.bit	Name	Mode	Description	Default
3.[15:10]	OUI	RO	Assigned to the 19th through 24th bits of the OUI.	1100 10
3.[9:4]	Model Number	RO	Manufacturer's model number 05.	00 0101
3.[3:0]	Revision Number	RO	Manufacturer's revision number 02.	0010

9.7.5. PHY 5 Register 4 (Page 0, 1, 2, 3): Auto-Negotiation Advertisement

Table 49. PHY 5 Register 4 (Page 0, 1, 2, 3): Auto-Negotiation Advertisement

Reg.bit	Name	Mode	Description	Default
4.15	Next Page	RO	1: Next Page enabled 0: Next Page disabled (Permanently =0)	0
4.14	Acknowledge	RO	Permanently =0.	0
4.13	Remote Fault	RO	1: Advertises that the RTL8306G has detected a remote fault 0: No remote fault detected	0
4.[12:11]	Reserved	RO	Reserved.	00
4.10	Pause	RW	1: Advertises that the RTL8306G possesses 802.3x flow control capability 0: No flow control capability	Pin 46 P4FLCTRL strap option, default 1
4.9	100Base-T4	RO	Not supported (Permanently =0).	0
4.8	100Base-TX-FD	RW	1: 100Base-TX full duplex capable 0: Not 100Base-TX full duplex capable	Pin 48 P4DUPSTA and pin 47 P4SPDSTA strap option
4.7	100Base-TX	RW	1: 100Base-TX half duplex capable 0: Not 100Base-TX half duplex capable	Pin 47 P4SPDSTA strap option
4.6	10Base-T-FD	RW	1: 10Base-TX full duplex capable 0: Not 10Base-TX full duplex capable	Pin 48 P4DUPSTA or pin 47 P4SPDSTA strap option
4.5	10Base-T	RW	1: 10Base-TX half duplex capable 0: Not 10Base-TX half duplex capable	1
4.[4:0]	Selector Field	RO	[00001]=IEEE 802.3	0 0001

9.7.6. PHY 5 Register 5 (Page 0, 1, 2, 3): Auto-Negotiation Link Partner Ability

Table 50. PHY 5 Register 5 (Page 0, 1, 2, 3): Auto-Negotiation Link Partner Ability

Reg.bit	Name	Mode	Description	Default
5.15	Next Page	RO	1: Link partner desires Next Page transfer 0: Link partner does not desire Next Page transfer	0
5.14	Acknowledge	RO	1: Link Partner acknowledges reception of Fast Link Pulse (FLP) words 0: Not acknowledged by Link Partner	0
5.13	Remote Fault	RO	1: Remote fault indicated by Link Partner 0: No remote fault indicated by Link Partner	0
5.[12:11]	Reserved	RO	Reserved.	00
5.10	Pause	RO	1: Flow control supported by Link Partner 0: Flow control not supported by Link Partner	Same as Reg 4
5.9	100Base-T4	RO	1: 100Base-T4 supported by Link Partner 0: 100Base-T4 not supported by Link Partner	0

Reg.bit	Name	Mode	Description	Default
5.8	100Base-TX-FD	RO	1: 100Base-TX full duplex supported by Link Partner 0: 100Base-TX full duplex not supported by Link Partner When auto negotiation is disabled, this bit will be set if Reg0.13=1 and Reg0.8=1 after link is established	Same as Reg 4
5.7	100Base-TX	RO	1: 100Base-TX half duplex supported by Link Partner 0: 100Base-TX half duplex not supported by Link Partner When auto negotiation is disabled, this bit will be set if Reg0.13=1 and Reg0.8=0 after link is established.	Same as Reg 4
5.6	10Base-T-FD	RO	1: 10Base-TX full duplex supported by Link Partner 0: 10Base-TX full duplex not supported by Link Partner When auto negotiation is disabled, this bit will be set if Reg0.13=0 and Reg0.8=1 after link is established.	Same as Reg 4
5.5	10Base-T	RO	1: 10Base-TX half duplex supported by Link Partner 0: 10Base-TX half duplex not supported by Link Partner When auto negotiation is disabled, this bit will be set if Reg0.13=0 and Reg0.8=0 after link is established.	1
5.[4:0]	Selector Field	RO	[00001]=IEEE 802.3	00001

9.8. PHY 6 Registers

9.8.1. PHY 6 Register 0 (Page 0, 1, 2, 3): Control

Table 51. PHY 6 Register 0 (Page 0, 1, 2, 3): Control

Reg.bit	Name	Mode	Description	Default
0.15	Reset	RO	0: No reset allowed (permanently =0)	0
0.14	Loopback (digital loopback)	RO	0: Normal operation (permanently =0)	0
0.13	Speed Select	RW	1: 100Mbps 0: 10Mbps When NWay is enabled, this bit reflects the result of auto-negotiation (Read only). When NWay is disabled, this bit can be set through SMI (Read/Write).	1
0.12	Auto Negotiation Enable	RW	1: Enable auto-negotiation process 0: Disable auto-negotiation process This bit can be set through SMI (Read/Write).	0
0.11	Power Down	RO	0: Normal operation (permanently =0)	0
0.10	Isolate	RO	0: Normal operation (permanently =0)	0
0.9	Restart Auto Negotiation	RO	0: Normal operation (permanently =0)	0
0.8	Duplex Mode	RW	1: Full duplex operation 0: Half duplex operation When NWay is enabled, this bit reflects the result of auto-negotiation (Read only). When NWay is disabled, this bit may be set through SMI (Read/Write).	1
0.[7:0]	Reserved	-	Reserved.	0000 0000

9.8.2. PHY 6 Register 1 (Page 0, 1, 2, 3): Status

Table 52. PHY 6 Register 1 (Page 0, 1, 2, 3): Status

Reg.bit	Name	Mode	Description	Default
1.15	100Base_T4	RO	0: No 100Base-T4 capability	0
1.14	100Base_TX_FD	RO	1: 100Base-TX full duplex capable (permanently =1)	1
1.13	100Base_TX_HD	RO	1: 100Base-TX half duplex capable (permanently =1)	1
1.12	10Base_T_FD	RO	1: 10Base-TX full duplex capable (permanently =1)	1
1.11	10Base_T_HD	RO	1: 10Base-TX half duplex capable (permanently =1)	1
1.[10:7]	Reserved	RO	Reserved.	0000
1.6	MF Preamble Suppression	RO	The RTL8306G will accept management frames with preamble suppressed (permanently =1).	1
1.5	Auto-negotiate Complete	RO	1: Auto-negotiation process completed. MII Reg.4, 5 are valid if this bit is set (permanently =1)	1
1.4	Remote Fault	RO	0: No remote fault (permanently =0)	0
1.3	Auto-Negotiation Ability	RO	1: NWay auto-negotiation capable (permanently =1)	1
1.2	Link Status	RO	1: Link is established 0: Link failed	0
1.1	Jabber Detect	RO	0: No Jabber detected (permanently =0)	0
1.0	Extended Capability	RO	1: Extended register capable (permanently =1)	1

9.8.3. PHY 6 Register 2 (Page 0, 1, 2, 3): PHY Identifier 1

Table 53. PHY 6 Register 2 (Page 0, 1, 2, 3): PHY Identifier 1

Reg.bit	Name	Mode	Description	Default
2.[15:0]	OUI	RO	Composed of the 3rd to 18th bits of the Organizationally Unique Identifier (OUI), respectively.	0x001C

9.8.4. PHY 6 Register 3 (Page 0, 1, 2, 3): PHY Identifier 2

Table 54. PHY 6 Register 3 (Page 0, 1, 2, 3): PHY Identifier 2

Reg.bit	Name	Mode	Description	Default
3.[15:10]	OUI	RO	Assigned to the 19th through 24th bits of the OUI.	1100 10
3.[9:4]	Model Number	RO	Manufacturer's model number 05.	00 0101
3.[3:0]	Revision Number	RO	Manufacturer's revision number 02.	0010

9.8.5. PHY 6 Register 4 (Page 0, 1, 2, 3): Auto-Negotiation Advertisement

Table 55. PHY 6 Register 4 (Page 0, 1, 2, 3): Auto-Negotiation Advertisement

Reg.bit	Name	Mode	Description	Default
4.15	Next Page	RO	1: Next Page enabled 0: Next Page disabled (Permanently =0)	0
4.14	Acknowledge	RO	Permanently =0.	0
4.13	Remote Fault	RO	1: Advertises that the RTL8306G has detected a remote fault 0: No remote fault detected	0
4.[12:11]	Reserved	RO	Reserved.	00
4.10	Pause	RW	1: Advertises that the RTL8306G possesses 802.3x flow control capability 0: No flow control capability	1
4.9	100Base-T4	RO	Not supported (Permanently =0).	0
4.8	100Base-TX-FD	RW	1: 100Base-TX full duplex capable 0: Not 100Base-TX full duplex capable	1
4.7	100Base-TX	RW	1: 100Base-TX half duplex capable 0: Not 100Base-TX half duplex capable	1
4.6	10Base-T-FD	RW	1: 10Base-TX full duplex capable 0: Not 10Base-TX full duplex capable	1
4.5	10Base-T	RW	1: 10Base-TX half duplex capable 0: Not 10Base-TX half duplex capable	1
4.[4:0]	Selector Field	RO	[00001]=IEEE 802.3.	0 0001

9.8.6. PHY 6 Register 5 (Page 0, 1, 2, 3): Auto-Negotiation Link Partner Ability

Table 56. PHY 6 Register 5 (Page 0, 1, 2, 3): Auto-Negotiation Link Partner Ability

Reg.bit	Name	Mode	Description	Default
5.15	Next Page	RO	1: Link partner desires Next Page transfer 0: Link partner does not desire Next Page transfer	0
5.14	Acknowledge	RO	1: Link Partner acknowledges reception of Fast Link Pulse (FLP) words 0: Not acknowledged by Link Partner	0
5.13	Remote Fault	RO	1: Remote Fault indicated by Link Partner 0: No remote fault indicated by Link Partner	0
5.[12:11]	Reserved	RO	Reserved.	00
5.10	Pause	RO	1: Flow control supported by Link Partner 0: Flow control not supported by Link Partner	1
5.9	100Base-T4	RO	1: 100Base-T4 supported by Link Partner 0: 100Base-T4 not supported by Link Partner	0
5.8	100Base-TX-FD	RO	1: 100Base-TX full duplex supported by Link Partner 0: 100Base-TX full duplex not supported by Link Partner When auto negotiation is disabled, this bit will be set if Reg0.13=1 and Reg0.8=1after link is established.	1

Reg.bit	Name	Mode	Description	Default
5.7	100Base-TX	RO	1: 100Base-TX half duplex supported by Link Partner 0: 100Base-TX half duplex not supported by Link Partner When auto negotiation is disabled, this bit will be set if Reg0.13=1 and Reg0.8=0 after link is established.	1
5.6	10Base-T-FD	RO	1: 10Base-TX full duplex supported by Link Partner 0: 10Base-TX full duplex not supported by Link Partner When auto negotiation is disabled, this bit will be set if Reg0.13=0 and Reg0.8=1 after link is established.	1
5.5	10Base-T	RO	1: 10Base-TX half duplex supported by Link Partner 0: 10Base-TX half duplex not supported by Link Partner When auto negotiation is disabled, this bit will be set if Reg0.13=0 and Reg0.8=0 after link is established.	1
5.[4:0]	Selector Field	RO	[00001]=IEEE 802.3	00001

9.8.7. PHY 6 Register 22 (Page 0, 1): Port 5 Control Register 0

Table 57. PHY 6 Register 22 (Page 0, 1): Port 5 Control Register 0

Reg.bit	Name	Mode	Description	Default
22.15	Port5 link status	RW	1: Port 5 link up and Reg 1.2=1 0: Port 5 link down and Reg 1.2=0 Whenever this bit changes, the PHY6 Reg1.2 will change simultaneously.	0
22.14	Reserved	-	Reserved.	0
22.13	Port 5 Local loopback	RW	1: Perform 'local loopback', i.e. loop MAC's RX back to TX 0: Normal operation	0
22.12	Port 5 Null VID replacement	RW	1: The switch will replace a NULL VID with a port VID (12-bits) 0: No replacement for a NULL VID	0
22.11	Port 5 Non PVID packets Discard	RW	1: If the received packets are tagged, the switch will discard packets whose VID does not match ingress port default VID, which is indexed by port 5's 'Port based VLAN index' 0: No packets will be dropped	0
22.10	Port 5 802.1p priority Disable	RW	1: Disable 802.1p priority classification for ingress packets on port 5 0: Enable 802.1p priority classification	1
22.9	Port 5 Diffserv priority Disable	RW	1: Disable Diffserv priority classification for ingress packets on port 5 0: Enable Diffserv priority classification	1
22.8	Port 5 port-based priority Disable	RW	1: Disable port-based priority QoS function on port 5 0: Enable port-based priority QoS function on port 5. Ingress packets on port 5 will be classified as high priority	1
22.7	Reserved	RO	Permanently 0.	0
22.6	Port 5 auto negotiation Enable	RW	1: Enable port 5 auto negotiation 0: Disable port 5 auto negotiation, the speed and duplex are decided by bit 5 and 4 of this register Whenever this bit changes, the PHY6 Reg0.12 will change simultaneously.	0

Reg.bit	Name	Mode	Description	Default
22.[5:4]	Port 5 Speed and Duplex ability	RW	11: MII Reg0.8=1, 0.13=1, 4.8=1, 4.7=0, 4.6=0, 4.5=0 10: MII Reg0.8=0, 0.13=1, 4.8=0, 4.7=1, 4.6=0, 4.5=0 01: MII Reg0.8=1, 0.13=0, 4.8=0, 4.7=0, 4.6=1, 4.5=0 00: MII Reg0.8=0, 0.13=0, 4.8=0, 4.7=0, 4.6=0, 4.5=1 Whenever bits 22.[5:4] change, the corresponding bits will change simultaneously.	11
22.3	Port 5 802.3x flow control ability Enable	RW	1: Enable port 5 full duplex flow control ability 0: Disable port 5 full duplex flow control ability Whenever its status changes, PHY 6 Reg 4.10 will change simultaneously	1
22.2	Port 5 Backpressure Enable	RW	1: Enable port 5 half duplex backpressure 0: Disable port 5 half duplex backpressure	1
22.[1:0]	Port 5 VLAN tag insertion and removal	RW	11: Do not insert or remove VLAN tags to/from packets that are output on this port 10: The switch will add VLAN tags to packets if they are not tagged when these packets are output on this port. The switch will not add tags to packets already tagged. The inserted tag is the ingress port's 'Default tag', which is indexed by port 5's 'Port based VLAN index' 01: The switch will remove VLAN tags from packets, if they are tagged when these packets are output on port 5. The switch will not modify packets received without tags. 00: The switch will remove VLAN tags from packets then add new tags to them. The inserted tag is the ingress port's "Default tag", which is indexed by port 5's 'Port based VLAN index'. This is a replacement processing for tagged packets and an insertion for untagged packets.	11

9.8.8. PHY 6 Register 24 (Page 0, 1): Port 5 Control Register 1

Table 58. PHY 6 Register 24 (Page 0, 1): Port 5 Control Register 1

Reg.bit	Name	Mode	Description	Default
24.15	Reserved	-	Reserved.	1
24.14	Disable IEEE 802.3x transmit flow control of port 5 MAC	RW	Only takes effect when PHY6 Reg.24.12=1. 1: Disable IEEE 802.3x transmit flow control ability of port 5 MAC 0: Enable IEEE 802.3x transmit flow control ability of port 5 MAC	0
24.13	Disable IEEE 802.3x receive flow control of port 5 MAC	RW	Only takes effect when PHY6 Reg.24.12=1. 1: Disable IEEE 802.3x receive flow control ability of port 5 MAC 0: Enable IEEE 802.3x receive flow control ability of port 5 MAC	0
24.12	Force asymmetric flow control of port 5 MAC	RW	0: No asymmetric flow control is provided. Use PHY6 Reg.4.10 to provide symmetric flow control both for pause reception and transmission 1: Enable asymmetric flow control of port 4 MAC. Use PHY6 Reg.24.13 for providing IEEE 802.3x receive flow control and use PHY6 Reg.24.14 for providing IEEE 802.3x transmit flow control	0
24.11	Port 5 Transmission Enable	RW	1: Enable packet transmission on port 5 0: Disable packet transmission on port 5	1
24.10	Port 5 Reception Enable	RW	1: Enable packet reception on port 5 0: Disable packet reception on port 5	1
24.9	Port 5 Learning Enable	RW	1: Enable switch address learning capability 0: Disable switch address learning capability	1
24.8	Port 5 Loop Status	RO	1: A loop has been detected on port 5 0: No loop exists on port 5	0
24.[7:0]	Reserved	-	Reserved.	11111111

10. Characteristics

10.1. Electrical Characteristics/Maximum Ratings

WARNING: Maximum ratings are limits beyond which permanent damage may be caused to the device or which may affect device reliability. All voltages are specified reference to GND unless otherwise specified.

Table 59. Electrical Characteristics/Maximum Ratings

Parameter	Min	Max	Units
Vcc Supply Referenced to GND	-0.5	+4.0	V
Digital Input Voltage	-0.5	VDD	V
DC Output Voltage	-0.5	VDD	V

10.2. Operating Range

Table 60. Operating Range

Parameter	Min	Max	Units
Storage Temperature	-55	+150	°C
Ambient Operating Temperature (Ta)	0	+70	°C
3.3V Vcc Supply Voltage Range (HVDD33, DVDD33)	3.15	3.45	V
1.8V Vcc Supply Voltage Range (DVDD18, AVDD18)	1.71	1.95	V

10.3. DC Characteristics

Table 61. DC Characteristics

Parameter	SYM	Condition	Min	Typical	Max	Units
TTL Input High Voltage	V_{ih}	-	2.0	-	-	V
TTL Input Low Voltage	V_{il}	-	-	-	0.8	V
TTL Input Current	I_{in}	-	-10	-	10	µA
TTL Input Capacitance	C_{in}	-	-	3	-	pF
Output High Voltage	V_{oh}	-	2.25	-	-	V
Output Low Voltage	V_{ol}	-	-	-	0.4	V
Output Three State Leakage Current	$\|I_{OZ}\|$	-	-	-	10	µA

10.4. AC Characteristics

Table 62. AC Characteristics

Parameter	SYM	Condition	Min	Typical	Max	Units
Transmitter, 100Base-TX						
Differential Output Voltage, Peak-to-Peak	V_{OD}	50Ω from each output to Vcc; best-fit over 14 bit times	-	1.007	-	V
Differential Output Voltage Symmetry	V_{OS}	50Ω from each output to Vcc, |Vp+|/ |Vp-|	-	99.1	-	%
Differential Output Overshoot	V_{OO}	Percent of Vp+ or Vp-	-	3.1	-	%
Rise/Fall Time	t_r ,t_f	10~90% of Vp+ or Vp-	-	4.1	-	ns
Rise/Fall Time Imbalance	$\|t_r - t_f\|$	-	-	0.17	-	ns
Duty Cycle Distortion	-	Deviation from best-fit time-grid, 010101 … Sequence	-	0.2	-	ns
Timing Jitter	-	Idle pattern	-	0.87	-	ns
TD Differential Output Impedance (Return Loss)	-	Return loss margin from 2Hz to 80MHz for reference resistance of 100Ω. The margin is the minimum difference between the limit line and the return loss curve	4.6	-	-	dB
RD Differential Output Impedance (Return Loss)	-	Return loss margin from 2Hz to 80MHz for reference resistance of 100Ω. The margin is the minimum difference between the limit line and the return loss curve	4.6	-	-	dB
Transmitter, 10Base-T						
Differential Output Voltage, Peak-to-Peak	V_{OD}	50Ω from each output to Vcc, all pattern	-	2.36	-	V
TP_IDL Silence Duration	-	Period of time from start of TP_IDL to link pulses or period of time between link pulses	-	10.48	-	ms
TD Short Circuit Fault Tolerance	-	Peak output current on TD short circuit for 10 seconds.	-	24	-	mA
TD Common-Mode Output Voltage	Ecm	Terminate each end with 50Ω resistive load	-	43.2	-	mV
Transmitter Output Jitter	-	-	-	6	-	ns
Harmonic Content	-	dB below fundamental, 20 cycles of all ones data	-	28	-	dB
Start-of-idle Pulse Width	-	TP_IDL width	-	256	-	ns

10.5. Digital Timing Characteristics

10.5.1. LED Timing

Table 63. LED Timing

Parameter	SYM	Condition	Min	Typical	Max	Units
LED Timing						
LED On Time	tLEDon	While LED blinking	43	-	120	ms
LED Off Time	tLEDoff	While LED blinking	43	-	120	ms

10.5.2. Reception/Transmission Data Timing of MII/RMII/SMI Interface

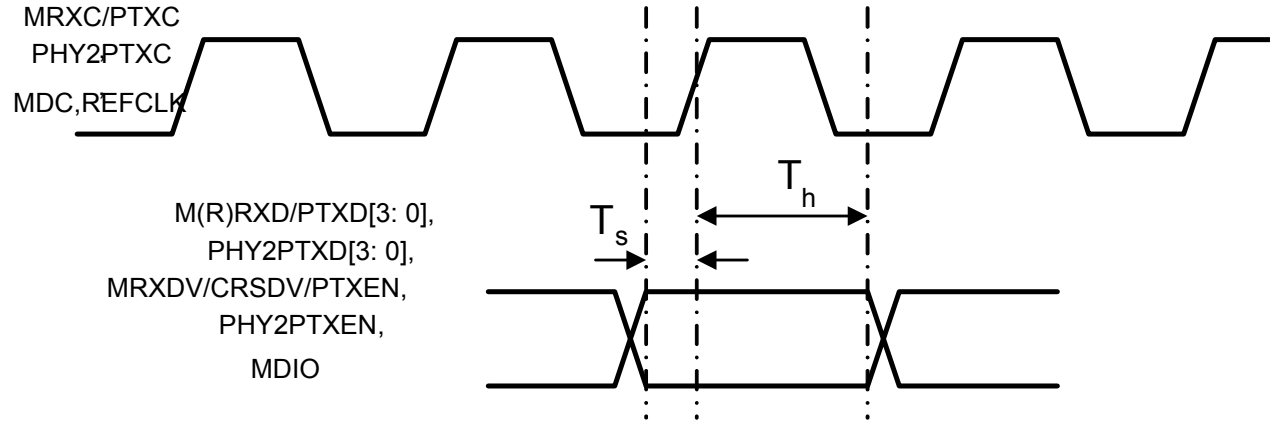


Figure 27. Reception Data Timing of MII/RMII/SMI Interface

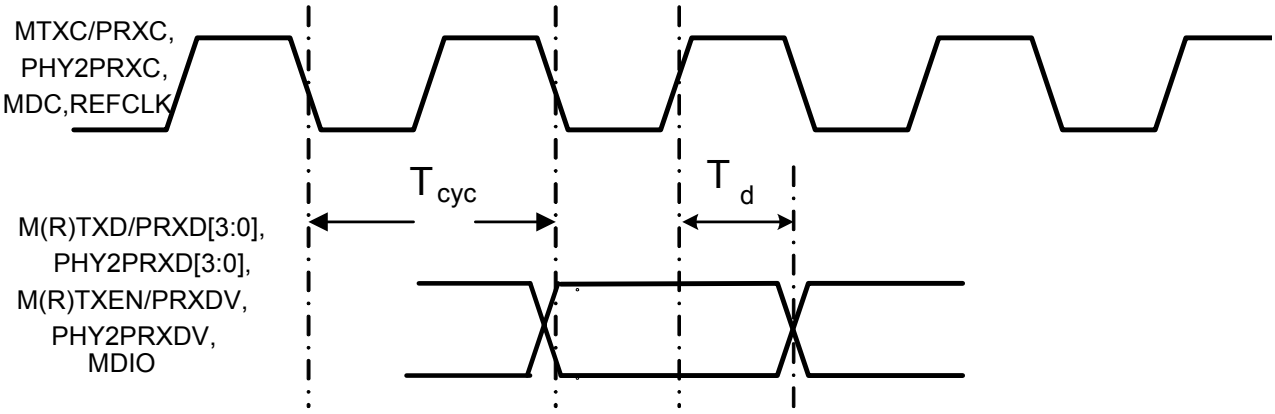


Figure 28. Transmission Data Timing of MII/RMII/SMI Interface

Table 64. MII & SMI DC Timing

Parameter	SYM	Description	I/O	Min	Type	Max	Units
MAC Mode MII Timing							
100BaseT MTXC/MRXC, MRXC/PTXC	T_{cyc}	MTXC/MRXC, MRXC/PTXC Clock Cycle Time	I	-	40 (±50 ppm)	-	ns
10BaseT MTXC/MRXC, MRXC/PTXC	T_{cyc}	MTXC/MRXC, MRXC/PTXC Clock Cycle Time	I	-	400 (±50 ppm)	-	ns
MTXD[3:0]/PRXD[3:0], MTXEN/PRXDV Output delay	T_d	MTXD[3:0]/PRXD[3:0], MTXEN/PRXDV to MTXC/PRXC Rising Edge Delay	O	4	5.2	6	ns
MRXD[3:0]/PTXD[3:0], MRXDV/PTXEN, Setup Time	T_s	MRXD[3:0]/PTXD[3:0], MRXDV/PTXEN to MRXC/PTXC Rising Edge Setup Time	I	4	-	-	ns
MRXD/PTXD, MRXDV/PTXEN, Hold Time	T_h	MRXD[3:0]/PTXD[3:0], MRXDV/PTXEN to MRXC/PTXC Rising Edge Hold Time	I	2	-	-	ns
PHY Mode MII Timing							
100BaseT MTXC/MRXC, MRXC/PTXC, PHY2PTXC, PHY2PRXC	T_{cyc}	MTXC/MRXC, MRXC/PTXC, PHY2PTXC, PHY2PRXC Clock Cycle Time	O	-	40 (±50 ppm)	-	ns
10BaseT MTXC/PRXC, MRXC/PTXC, PHY2PTXC, PHY2PRXC	T_{cyc}	MTXC/MRXC, MRXC/PTXC, PHY2PTXC, PHY2PRXC Clock Cycle Time	O	-	400 (±50 ppm)	-	ns
MTXD/PRXD[3:0], PHY2PRXD[3:0], MTXEN/PRXDV, PHY2PRXDV Output Delay	T_d	MTXD[3:0]/PRXD[3:0], PHY2PRXD[3:0], MTXEN/PRXDV, PHY2PRXDV to MTXC/PRXC Rising Edge Delay	O	20.5	22.5	23.5	ns
MRXD/PTXD[3:0], PHY2PTXD[3:0], MRXDV/PTXEN, PHY2PTXEN Setup Time	T_s	MRXD[3:0]/PTXD[3:0], MRXDV/PTXEN to MRXC/PTXC Rising Edge Setup Time	I	4	-	-	ns
MRXD/PTXD[3:0], PHY2PTXD[3:0], MRXDV/PTXEN, PHY2PTXEN Hold Time	T_h	MRXD[3:0]/PTXD[3:0], MRXDV/PTXEN to MRXC/PTXC Rising Edge Hold Time	I	2	-	-	ns
RMII Timing							
REFCLK	T_{cyc}	REFCLK Clock Cycle Time	O	-	20 (±50 ppm)	-	ns
RTXD[1:0], RTXEN Output Delay	T_d	RTXD[1:0], TXEN to REFCLK Rising Edge Delay	O	7.6	8.7	9.6	ns
RRXD[1:0], CRSDV Setup Time	T_s	RRXD[1:0], CRSDV to REFCLK Rising Edge Setup Time	I	4	-	-	ns
RRXD[1:0], CRSDV Hold Time	T_h	RRXD[1:0], CRSDV to REFCLK Rising Edge Hold Time	I	2	-	-	ns
SMI Timing							
MDC	T_{cyc}	MDC Clock Cycle	I	40	-	-	ns
MDIO Setup Time	T_s	Write Cycle	I	10	-	-	ns
MDIO Hold Time	T_h	Write Cycle	I	10	-	-	ns
MDIO Output Delay Relative to Rising Edge of MDC	T_d	Read Cycle	O		-	10	µs

11. Application Information

11.1. UTP (10Base-T/100Base-TX) Applications

Note that the center-tap on the primary side of the transformer must be connected to 1.8V and should be connected to ground via a 0.1µF capacitor.

Table 65. Transformer Vendors

Vendor	Quad	Single
Pulse	H1164	H1102
Magnetic 1	ML164	ML102

Two types of transformer are generally used for the RTL8306G. One is a Quad (4-port) transformer with one common pin on both sides of an internal connected central tap. The other is a Single (1-port) transformer with two pins on both sides of a separate central tap. The RTL8306G is designed for a transformer without a common mode choke on the primary side, and we recommend that a transformer with a common mode choke on the primary is not used with the RTL8306G.

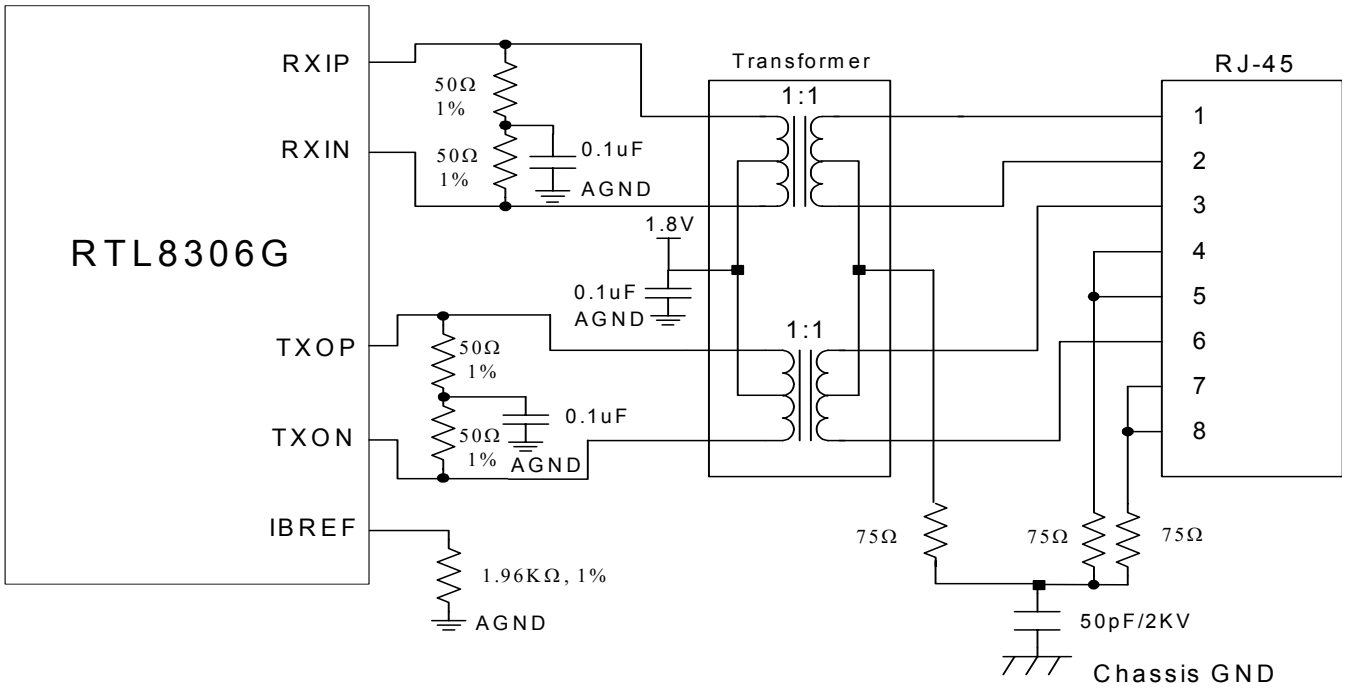


Figure 29. UTP Application for Transformer with Connected Central Tap

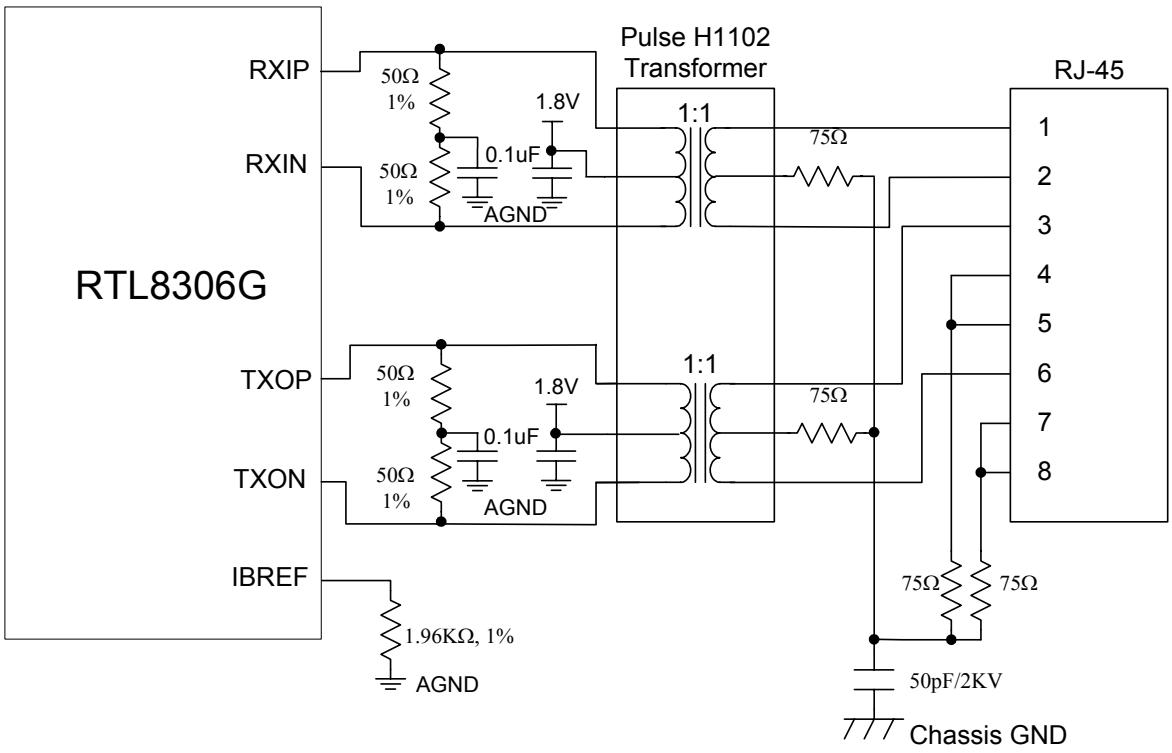


Figure 30. UTP Application for Transformer with Separate Central Tap

12. Design and Layout

In order to achieve maximum performance using the RTL8306G, good design attention is required throughout the design and layout process. The following are some suggestions to implement a high-performance system.

General Guidelines

- Provide a good power source, minimizing noise from switching power supply circuits (<50mV).
- Verify the ability of critical components, e.g. clock source and transformer, to meet application requirements.
- Keep power and ground noise levels below 50mV.
- Use bulk capacitors (4.7µF~10µF) between the power and ground planes.
- Use 0.1µF de-coupling capacitors to reduce high-frequency noise on the power and ground planes.
- Keep de-coupling capacitors as close as possible to the RTL8306G chip.

Differential Signal Layout Guidelines

- Keep differential pairs as close as possible and route both traces as identically as possible.
- Avoid vias and layer changes if possible.
- Keep transmit and receive pairs away from each other.

Clock Circuit

- If possible, surround the clock by ground trace to minimize high-frequency emissions.
- Keep the crystal or oscillator as close to the RTL8306G as possible.

1.8V Power

- Do not connect a bead directly between the collector of the PNP transistor and AVDD18. This will significantly affect the stability of the 1.8V power supply.
- Use a bulk capacitor (4.7µF~10µF) between the collector of the PNP transistor and the ground plane.
- Do not use one PNP transistor for more than one RTL8306G chip, even if the rating is enough. Use one transistor for each RTL8306G chip.

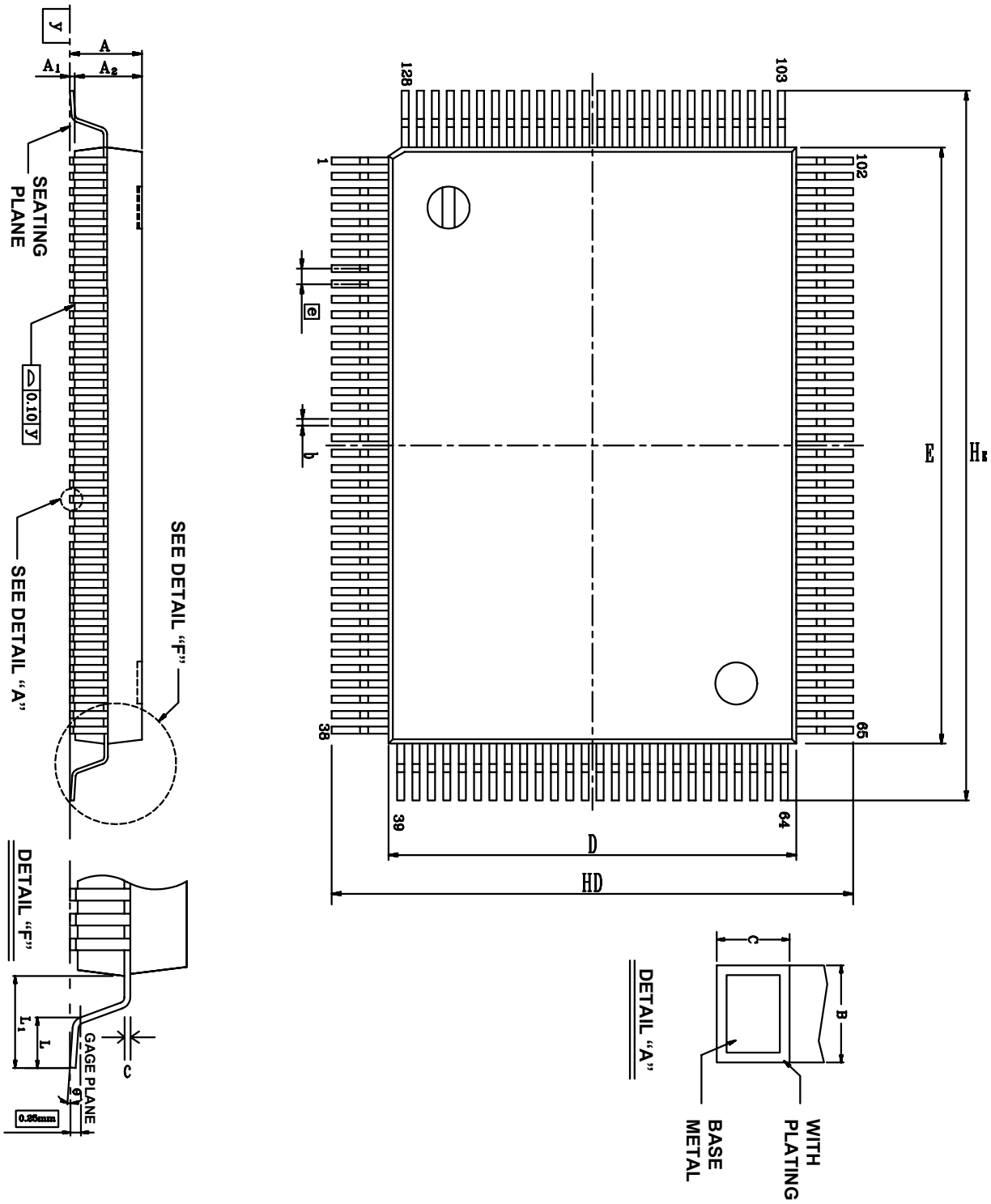
Power Plane

- Divide the power plane into 1.8V digital, 3.3V digital, and 1.8V analog.
- Use 0.1µF decoupling capacitors and bulk capacitors between each power plane and the ground plane.
- Power line connects from the source to the RTL8306G pin should be at least 10 mil wide.

Ground Plane

- Keep the system ground region as one continuous, unbroken plane that extends from the primary side of the transformer to the rest of the board.
- Place a moat (gap) between the system ground and chassis ground.
- Ensure the chassis ground area is voided at some point such that no ground loop exists on the chassis ground area.

13. Mechanical Dimensions



See the Mechanical Dimensions notes on the next page.

13.1. Mechanical Dimensions Notes

Symbol	Dimensions in inches			Dimensions in mm		
	Min	Typical	Max	Min	Typical	Max
A	-	-	0.134	-	-	3.40
A1	0.004	0.010	0.036	0.10	0.25	0.91
A2	0.102	0.112	0.122	2.60	2.85	3.10
b	0.005	0.009	0.013	0.12	0.22	0.32
c	0.002	0.006	0.010	0.05	0.15	0.25
D	0.541	0.551	0.561	13.75	14.00	14.25
E	0.778	0.787	0.797	19.75	20.00	20.25
e	0.010	0.020	0.030	0.25	0.5	0.75
HD	0.665	0.677	0.689	16.90	17.20	17.50
HE	0.902	0.913	0.925	22.90	23.20	23.50
L	0.027	0.035	0.043	0.68	0.88	1.08
L1	0.053	0.063	0.073	1.35	1.60	1.85
y	-	-	0.004	-	-	0.10
θ	0°	-	12°	0°	-	12°

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar rotrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. Should be based on final visual inspection.

TITLE: PQFP-128 -CU L/F, FOOTPRINT 3.2 mm			
LEADFRAME MATERIAL:			
APPROVE		DOC. NO.	
		VERSION	1.2
		PAGE	
CHECK		DWG NO.	Q128 - 1
		DATE	12 February 2003
REALTEK SEMICONDUCTOR CORP.			

14. Ordering Information

Table 66. Ordering Information

Part Number	Package	Status
RTL8306G-GR	128-Pin PQFP in 'Green' Package (RoHS Compliant)	Production

Note: See page 6 for package and version identification.

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