SBOS344C – SEPTEMBER 2005 – REVISED MAY 2012

4-20mA Current-Loop Transmitter

FEATURES

- LOW QUIESCENT CURRENT: 130μA
- 5V REGULATOR FOR EXTERNAL CIRCUITS
- LOW SPAN ERROR: 0.05%
- LOW NONLINEARITY ERROR: 0.003%
- WIDE-LOOP SUPPLY RANGE: 7.5V to 40V
- MSOP-8 AND DFN-8 PACKAGES

APPLICATIONS

- TWO-WIRE, 4-20mA CURRENT LOOP TRANSMITTER
- SMART TRANSMITTER
- INDUSTRIAL PROCESS CONTROL
- TEST SYSTEMS
- CURRENT AMPLIFIER
- VOLTAGE-TO-CURRENT AMPLIFIER

DESCRIPTION

The XTR117 is a precision current output converter designed to transmit analog 4-20mA signals over an industry-standard current loop. It provides accurate current scaling and output current limit functions.

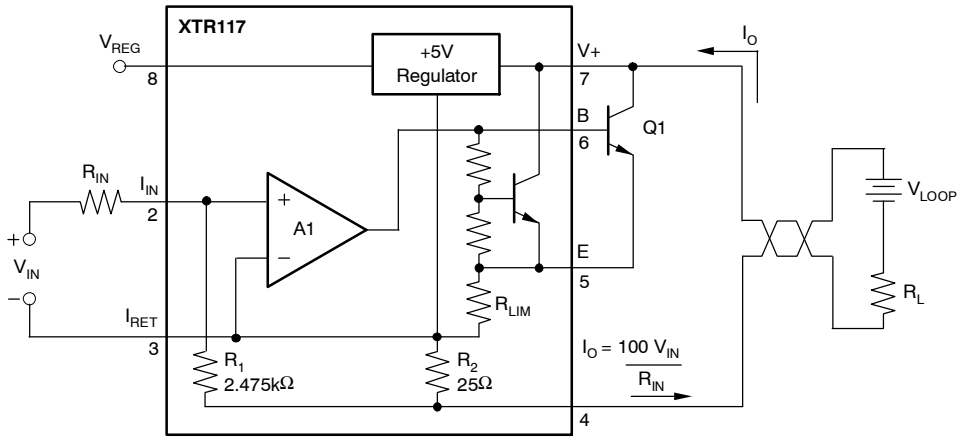
The on-chip voltage regulator (5V) can be used to power external circuitry. A current return pin (I_{RET}) senses any current used in external circuitry to assure an accurate control of the output current.

The XTR117 is a fundamental building block of smart sensors using 4-20mA current transmission. The XTR117 is specified for operation over the extended industrial temperature range, –40°C to +125°C.

RELATED 4-20mA PRODUCTS

XTR115	5V regulator output and 2.5V reference output
XTR116	5V regulator output and 4.096V reference output

NOTE: For 4-20mA complete bridge and RTO conditioner solutions, see the XTR product family website at www.ti.com.



ABSOLUTE MAXIMUM RATINGS(1)

Power Supply, V+ (referenced to I_O pin)	+50V
Input Voltage, (referenced to I_{RET} pin)	0V to V+
Output Current Limit	Continuous
V_{REG}, Short-Circuit	Continuous
Operating Temperature Range	–55°C to +125°C
Storage Temperature Range	–55°C to +150°C
Junction Temperature	+165°C
ESD Rating (Human Body Model)	2000V
(Charged Device Model)	1000V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

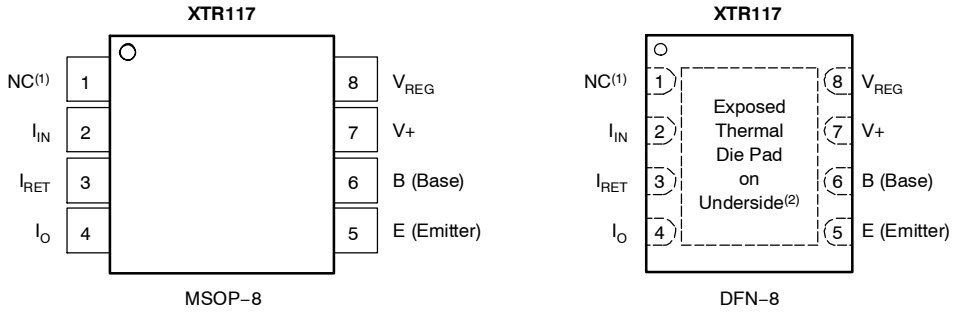
PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
XTR117	MSOP-8	DGK	BOZ
XTR117	DFN-8	DRB	BOY

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

PIN ASSIGNMENTS

Top View



NOTES: (1) NC = No connection. Leave unconnected on PCB.
(2) Connect thermal die pad to I_{RET} or leave unconnected on PCB.

ELECTRICAL CHARACTERISTICS: V+ = +24V

Boldface limits apply over the temperature range, **T_A = –40°C to +125°C**.

All specifications at T_A = +25°C, V+ = 24V, R_{IN} = 20kΩ, and TIP29C external transistor, unless otherwise noted.

PARAMETER		CONDITION	XTR117 MIN	XTR117 TYP	XTR117 MAX	UNITS
OUTPUT						
Output Current Equation	I_O			$I_O = I_{IN} \times 100$		
Output Current, Linear Range			0.20		25	mA
Over-Scale Limit	I_{LIM}			32		mA
Under-Scale Limit	I_{MIN}	I_{REG} = 0		0.13	0.20	mA
SPAN						
Span (Current Gain)	S			100		A/A
Error(1)		I_O = 200µA to 25mA		±0.05	±0.4	%
vs Temperature		**T_A = –40°C to +125°C**		**±3**	**±20**	**ppm/°C**
Nonlinearity		I_O = 200µA to 25mA		±0.003	±0.02	%
INPUT						
Offset Voltage (Op Amp)	V_{OS}	I_{IN} = 40µA		±100	±500	µV
vs Temperature		**T_A = –40°C to +125°C**		**±0.7**	**±6**	**µV/°C**
vs Supply Voltage, V+		V+ = 7.5V to 40V		+0.1	+2	µV/V
Bias Current	I_B			–35		nA
vs Temperature		**T_A = –40°C to +125°C**		**150**		**pA/°C**
Noise: 0.1Hz to 10Hz	e_n			0.6		μV_{PP}
DYNAMIC RESPONSE						
Small-Signal Bandwidth		C_{LOOP} = 0, R_L = 0		380		kHz
Slew Rate				3.2		mA/µs
V_{REG}(2)						
Voltage				5		V
Voltage Accuracy		I_{REG} = 0		±0.05	±0.1	V
vs Temperature		**T_A = –40°C to +125°C**		**±0.1**		**mV/°C**
vs Supply Voltage, V+		V+ = 7.5V to 40V		1		mV/V
vs Output Current				See Typical Characteristics		
Short-Circuit Current				12		mA
POWER SUPPLY						
Specified Voltage Range	V+			+24		V
Operating Voltage Range			+7.5		+40	V
Quiescent Current	I_Q			130	200	µA
Over Temperature		**T_A = –40°C to +125°C**			**250**	**µA**
TEMPERATURE RANGE						
Specified Range			–40		+125	°C
Operating Range			–55		+125	°C
Storage Range			–55		+150	°C
Thermal Resistance	θ_{JA}					
MSOP				150		°C/W
DFN				53		°C/W

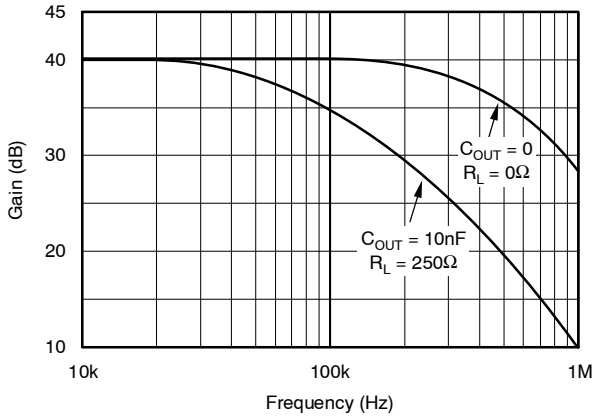
(1) Does not include initial error or temperature coefficient of R_{IN}.

(2) Voltage measured with respect to I_{RET} pin.

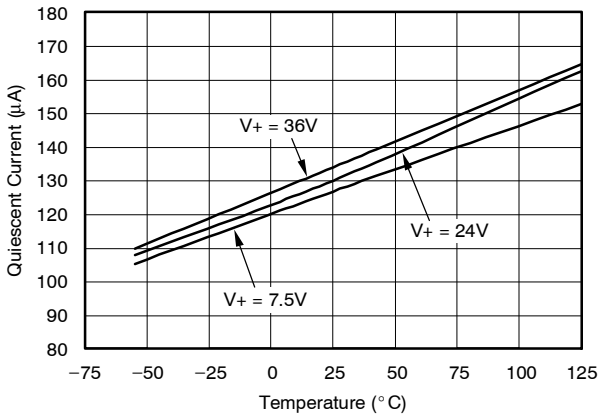
TYPICAL CHARACTERISTICS: V+ = +2.7V to +5.5V

At T_A = +25°C, V+ = 24V, R_{IN} = 20kΩ, and TIP29C external transistor, unless otherwise noted.

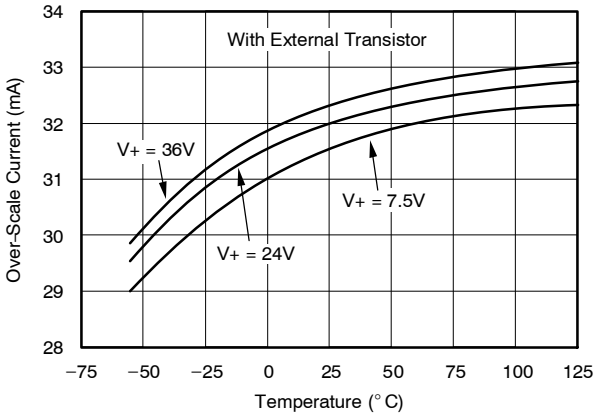
CURRENT GAIN vs FREQUENCY



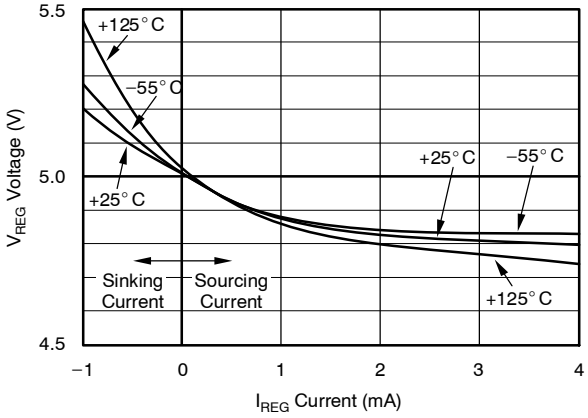
QUIESCENT CURRENT vs TEMPERATURE



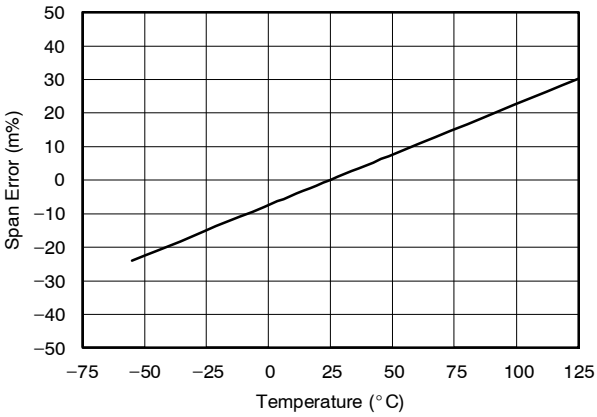
OVER-SCALE CURRENT vs TEMPERATURE



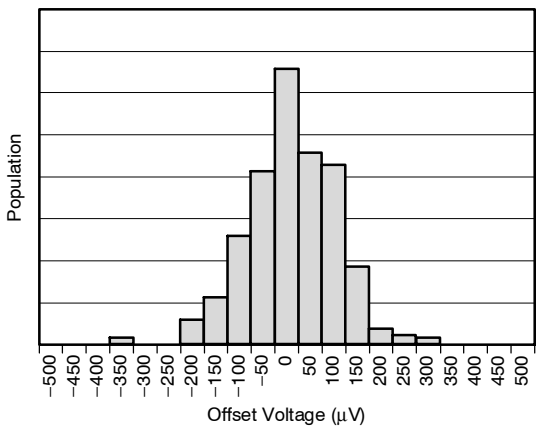
V_{REG} VOLTAGE vs V_{REG} CURRENT



SPAN ERROR vs TEMPERATURE



OFFSET VOLTAGE DISTRIBUTION



APPLICATIONS INFORMATION

BASIC OPERATION

The XTR117 is a precision current output converter designed to transmit analog 4-20mA signals over an industry-standard current loop. Figure 1 shows basic circuit connections with representative simplified input circuitry. The XTR117 is a two-wire current transmitter. Its input current (pin 2) controls the output current. A portion of the output current flows into the V+ power supply, pin 7. The remaining current flows in Q_1. External input circuitry connected to the XTR117 can be powered from V_{REG}. Current drawn from these terminals must be returned to I_{RET}, pin 3. The I_{RET} pin is a *local ground* for input circuitry driving the XTR117.

The XTR117 is a current-input device with a gain of 100. A current flowing into pin 2 produces $I_O = 100 \times I_{IN}$. The input voltage at the I_{IN} pin is zero (referred to the I_{RET} pin). A voltage input is converted to an input current with an external input resistor, R_{IN}, as shown in Figure 1. Typical full-scale input voltages range from 1V and upward. Full-scale inputs greater than 0.5V are recommend to minimize the effects of offset voltage and drift of A1.

EXTERNAL TRANSISTOR

The external transistor, Q_1, conducts the majority of the full-scale output current. Power dissipation in this transistor can approach 0.8W with high loop voltage (40V) and 20mA output current. The XTR117 is designed to use an external transistor to avoid on-chip, thermal-induced errors. Heat produced by Q_1 will still cause ambient temperature changes that can influence the XTR117 performance. To minimize these effects, locate Q_1 away from sensitive analog circuitry, including XTR117. Mount Q_1 so that heat is conducted to the outside of the transducer housing.

The XTR117 is designed to use virtually any NPN transistor with sufficient voltage, current and power rating. Case style and thermal mounting considerations often influence the choice for any given application. Several possible choices are listed in Figure 1. A MOSFET transistor will not improve the accuracy of the XTR117 and is not recommended.

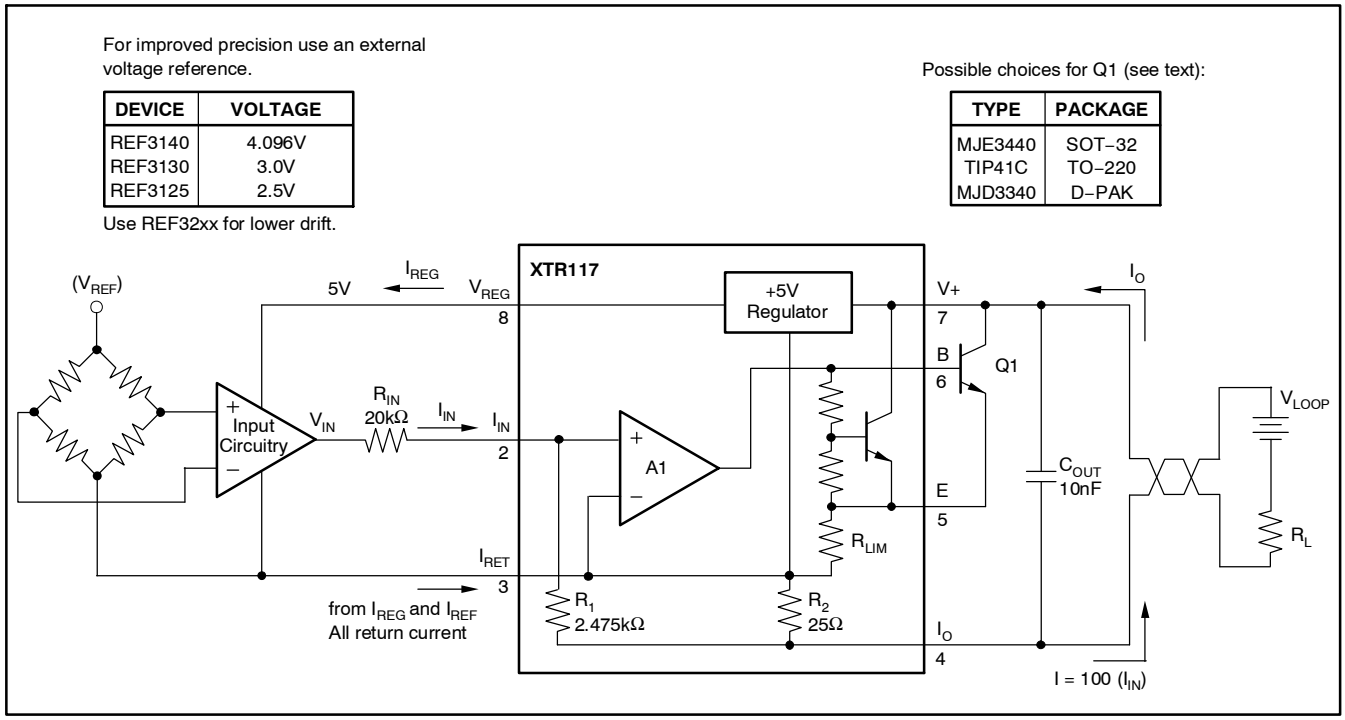


Figure 1. Basic Circuit Connections

MINIMUM OUTPUT CURRENT

The quiescent current of the XTR117 (typically 130μA) is the lower limit of its output current. Zero input current (I_{IN} = 0) will produce an I_O equal to the quiescent current. Output current will not begin to increase until $I_{IN} > I_Q/100$. Current drawn from V_{REG} will be added to this minimum output current. Up to 3.8mA is available to power external circuitry while still allowing the output current to go below 4mA.

OFFSETTING THE INPUT

A low-scale output of 4mA is produced by creating a 40μA input current. This input current can be created with the proper value resistor from an external reference voltage (V_{REF}) as shown in Figure 2. V_{REG} can be used as shown in Figure 2 but will not have the temperature stability of a high quality reference such as the REF3125.

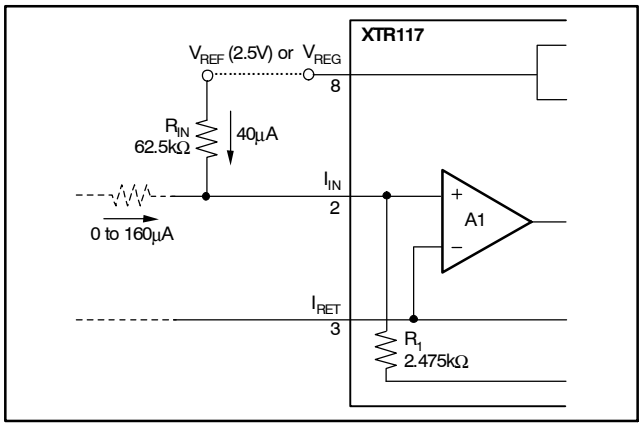


Figure 2. Creating Low-Scale Offset

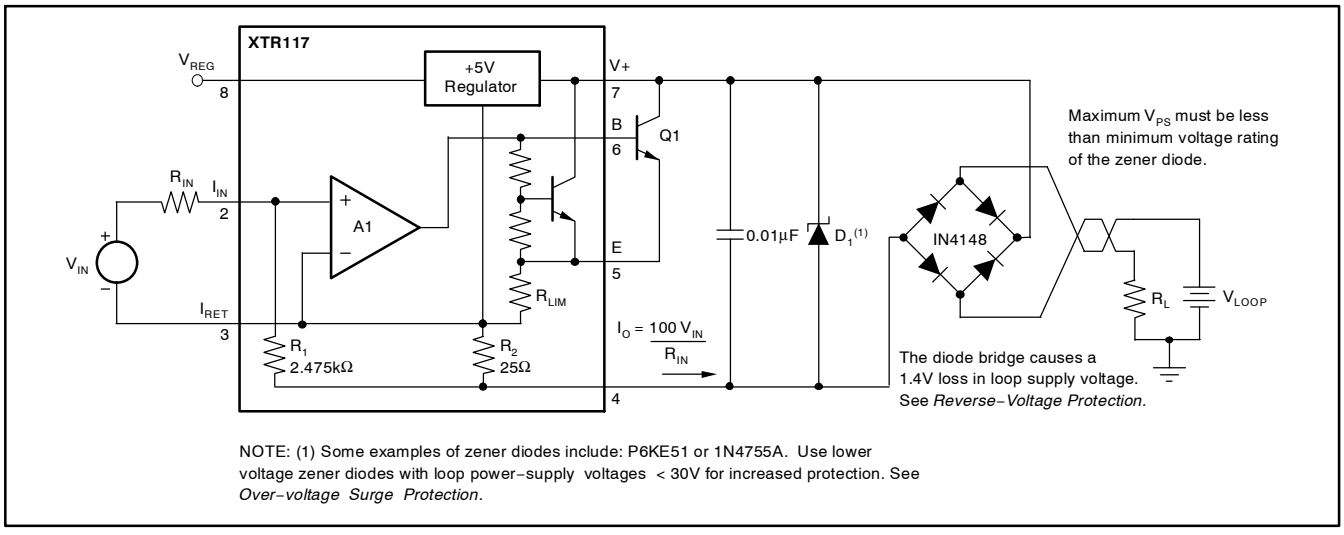
MAXIMUM OUTPUT CURRENT

The XTR117 provides accurate, linear output up to 25mA. Internal circuitry limits the output current to approximately 32mA to protect the transmitter and loop power/measurement circuitry.

It is possible to extend the output current range of the XTR117 by connecting an external resistor from pin 3 to pin 5, to change the current limit value. Since all output current must flow through internal resistors, it is possible to cause internal damage with excessive current. Output currents greater than 45mA may cause permanent damage.

REVERSE-VOLTAGE PROTECTION

The XTR117 low compliance voltage rating (minimum operating voltage) of 7.5V permits the use of various voltage protection methods without compromising operating range. Figure 3 shows a diode bridge circuit which allows normal operation even when the voltage connection lines are reversed. The bridge causes a two diode drop (approximately 1.4V) loss in loop supply voltage. This voltage drop results in a compliance voltage of approximately 9V—satisfactory for most applications. A diode can be inserted in series with the loop supply voltage and the V+ pin to protect against reverse output connection lines with only a 0.7V loss in loop supply voltage.



NOTE: (1) Some examples of zener diodes include: P6KE51 or 1N4755A. Use lower voltage zener diodes with loop power–supply voltages < 30V for increased protection. See *Over–voltage Surge Protection*.

Figure 3. Reverse Voltage Operation and Over-Voltage Surge Protection

OVER-VOLTAGE SURGE PROTECTION

Remote connections to current transmitters can sometimes be subjected to voltage surges. It is prudent to limit the maximum surge voltage applied to the XTR117 to as low as practical. Various zener diode and surge clamping diodes are specially designed for this purpose. Select a clamp diode with as low a voltage rating as possible for best protection. Absolute maximum power-supply rating on the XTR117 is specified at +50V. Keep overvoltages and transients below +50V to ensure reliable operation when the supply returns to normal (7.5V to 40V).

Most surge protection zener diodes have a diode characteristic in the forward direction that will conduct excessive current, possibly damaging receiving-side circuitry if the loop connections are reversed. If a surge protection diode is used, a series diode or diode bridge should be used for protection against reversed connections.

RADIO FREQUENCY INTERFERENCE

The long wire lengths of current loops invite radio frequency (RF) interference. RF interference can be rectified by the input circuitry of the XTR117 or preceding circuitry. This effect generally appears as an unstable output current that varies with the position of loop supply or input wiring. Interference may also enter at the input terminals. For integrated transmitter assemblies with short connections to the sensor, the interference more likely comes from the current loop connections.

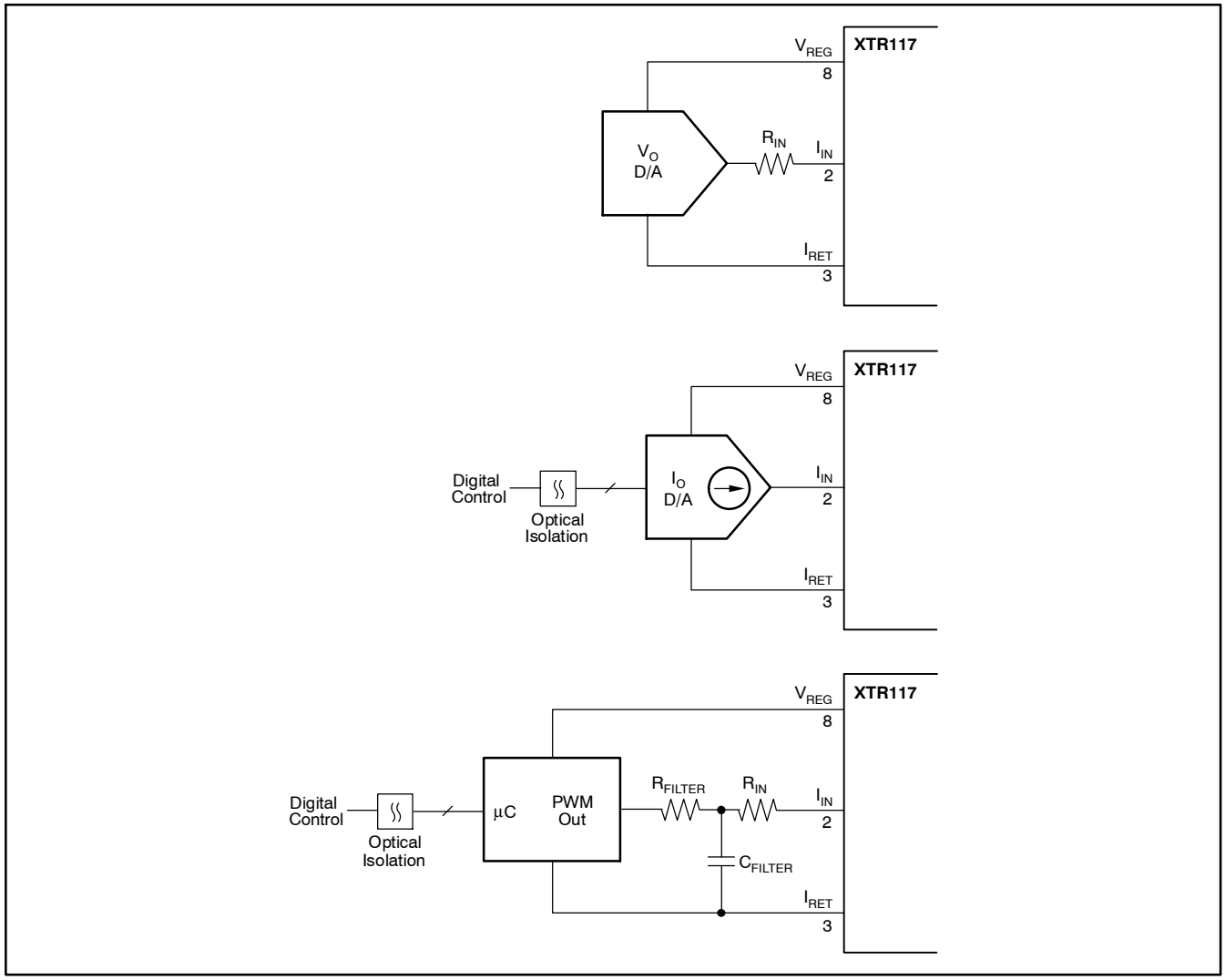


Figure 4. Digital Control Methods

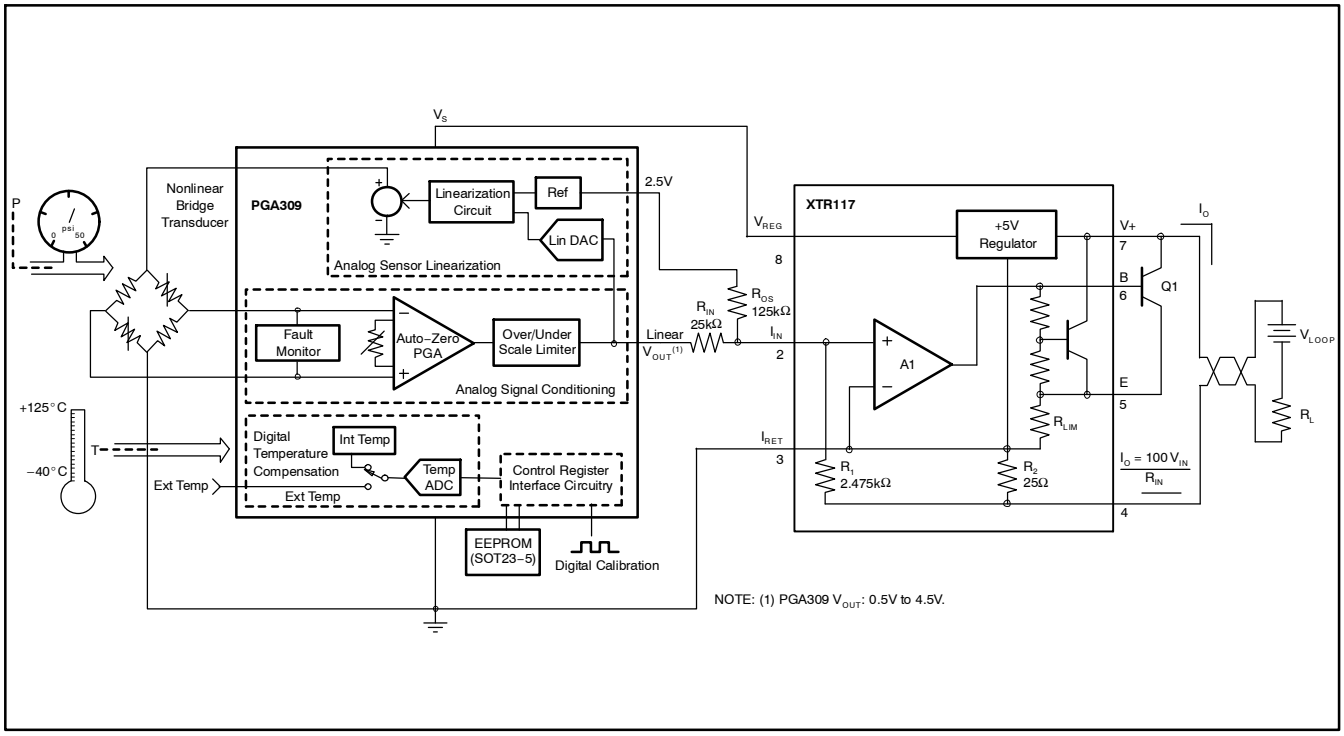


Figure 5. Complete 4-20mA Pressure Transducer Solution with PGA309 and XTR117

DFN PACKAGE

The XTR117 is offered in a DFN-8 package (also known as SON). The DFN is a QFN package with lead contacts on only two sides of the bottom of the package. This leadless package maximizes board space and enhances thermal and electrical characteristics through an exposed pad.

DFN packages are physically small, have a smaller routing area, improved thermal performance, and improved electrical parasitics. Additionally, the absence of external leads eliminates bent-lead issues.

The DFN package can be easily mounted using standard printed circuit board (PCB) assembly techniques. See Application Note, *QFN/SON PCB Attachment* (SLUA271) and Application Report, *Quad Flatpack No-Lead Logic Packages* (SCBA017), both available for download at www.ti.com.

The exposed leadframe die pad on the bottom of the package should be connected to I_{RET} or left unconnected.

LAYOUT GUIDELINES

The exposed leadframe die pad on the DFN package should be soldered to a thermal pad on the PCB. A mechanical drawing showing an example layout is attached at the end of this data sheet. Refinements to this layout may be required based on assembly process requirements. Mechanical drawings located at the end of this data sheet list the physical dimensions for the package and pad. The five holes in the landing pattern are optional, and are intended for use with thermal vias that connect the leadframe die pad to the heatsink area on the PCB.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term stability.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XTR117AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-3-260C-168 HR	-40 to 125	BOZ	Samples
XTR117AIDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-40 to 125	BOZ	Samples
XTR117AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-3-260C-168 HR	-40 to 125	BOZ	Samples
XTR117AIDGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-40 to 125	BOZ	Samples
XTR117AIDRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	BOY	Samples
XTR117AIDRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	BOY	Samples
XTR117AIDRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	BOY	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

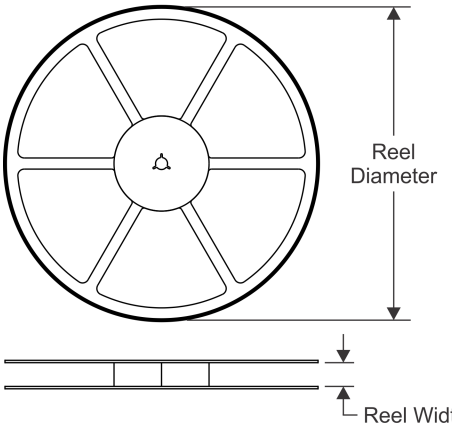
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

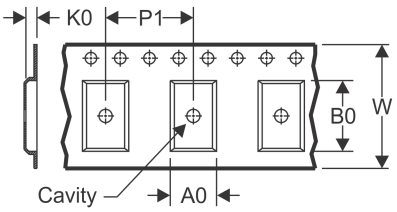
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

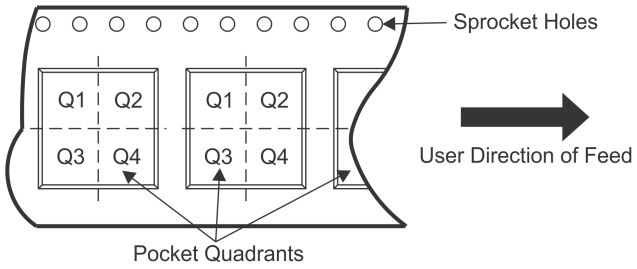


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

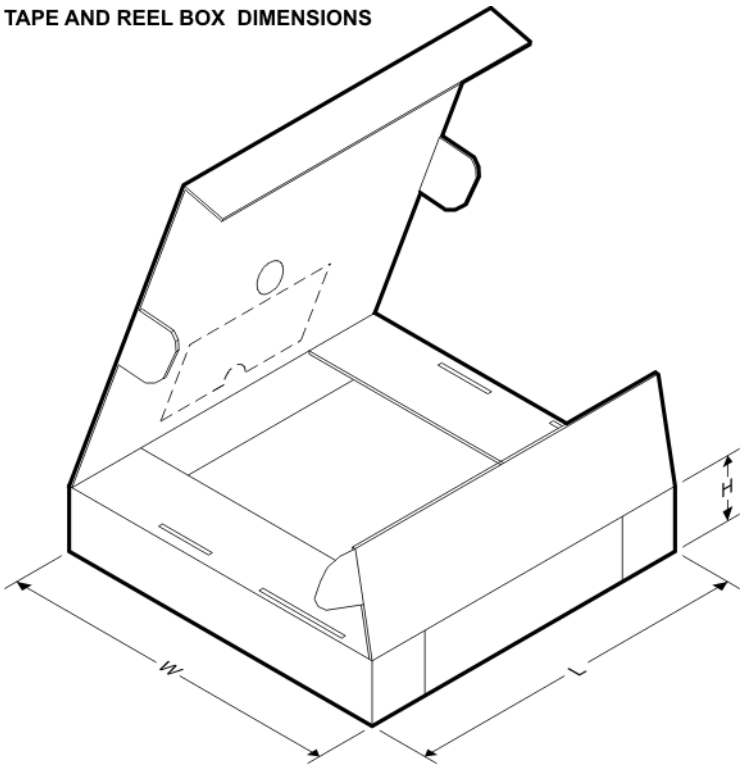
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XTR117AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
XTR117AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
XTR117AIDRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
XTR117AIDRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XTR117AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
XTR117AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
XTR117AIDRBR	SON	DRB	8	3000	367.0	367.0	35.0
XTR117AIDRBT	SON	DRB	8	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DRB 8

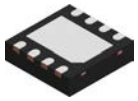
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

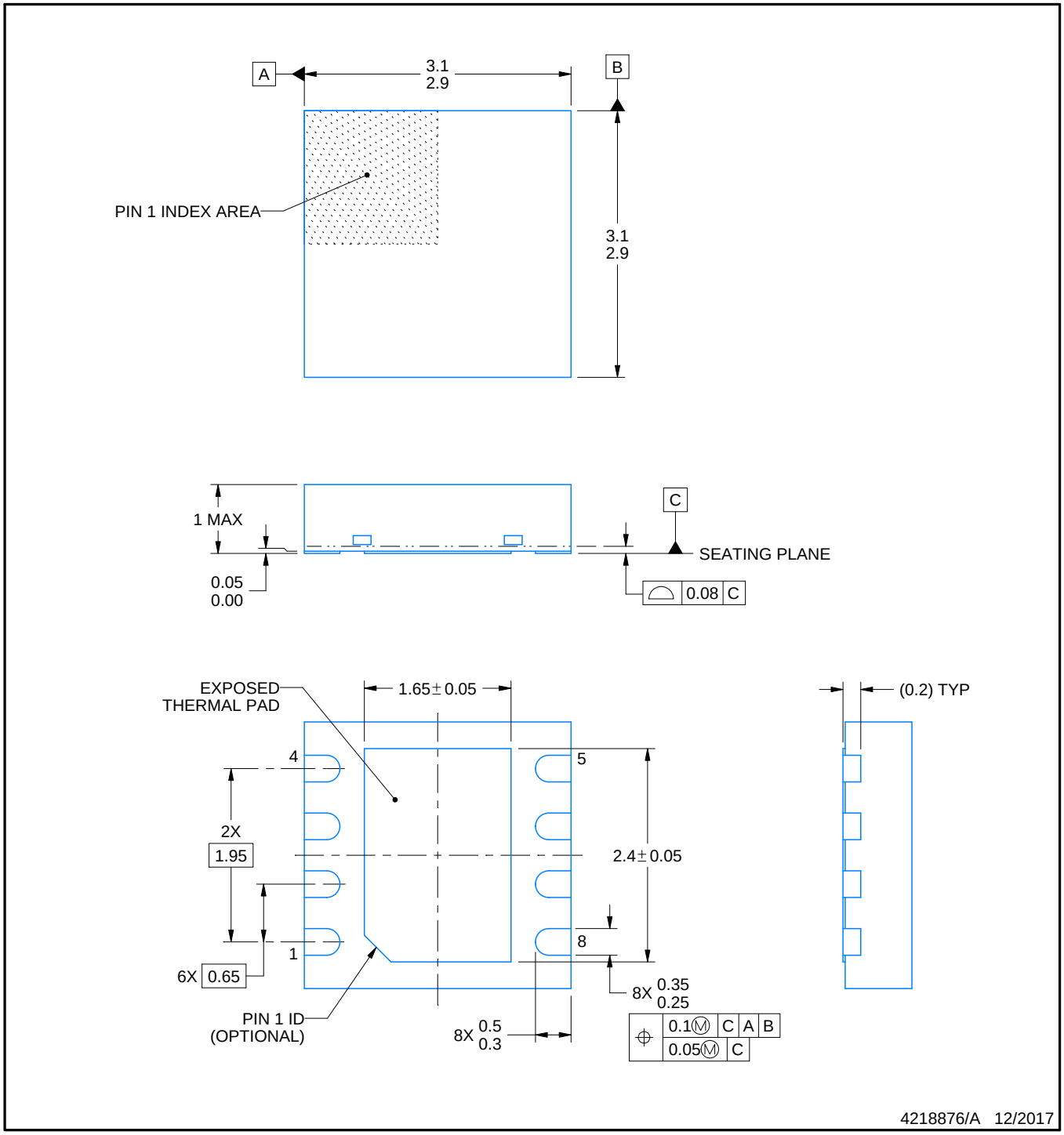
DRB0008B



PACKAGE OUTLINE

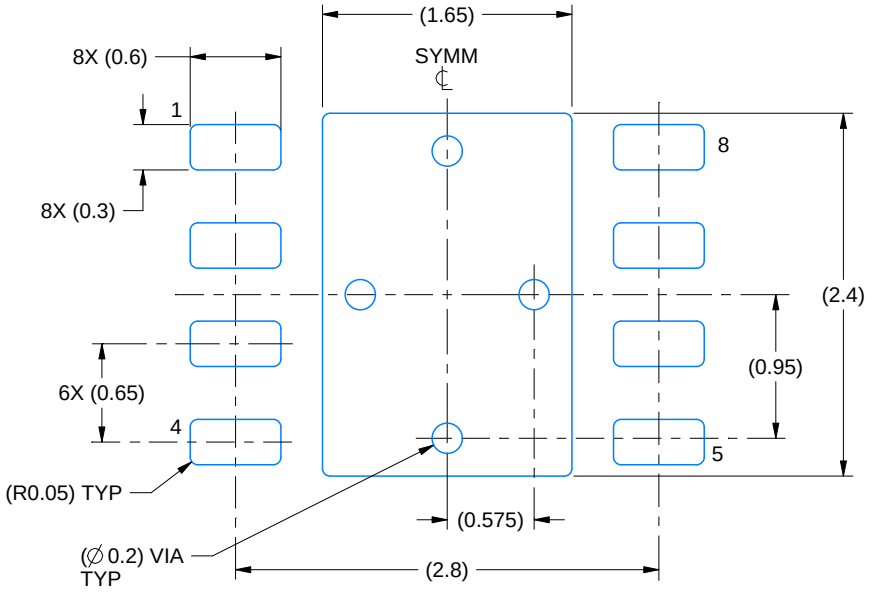
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

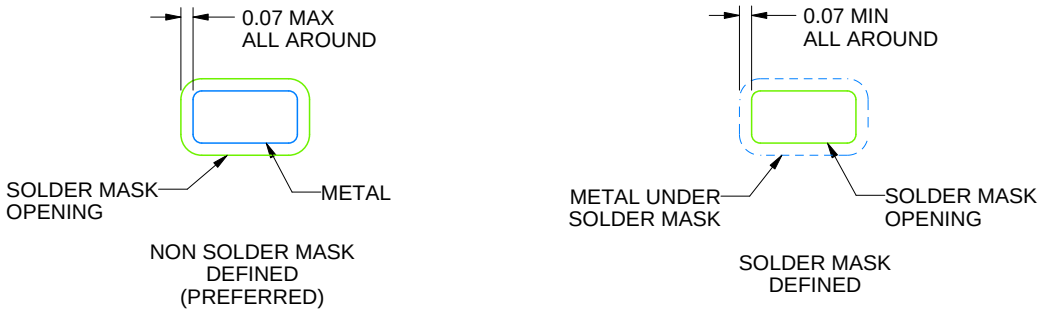


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

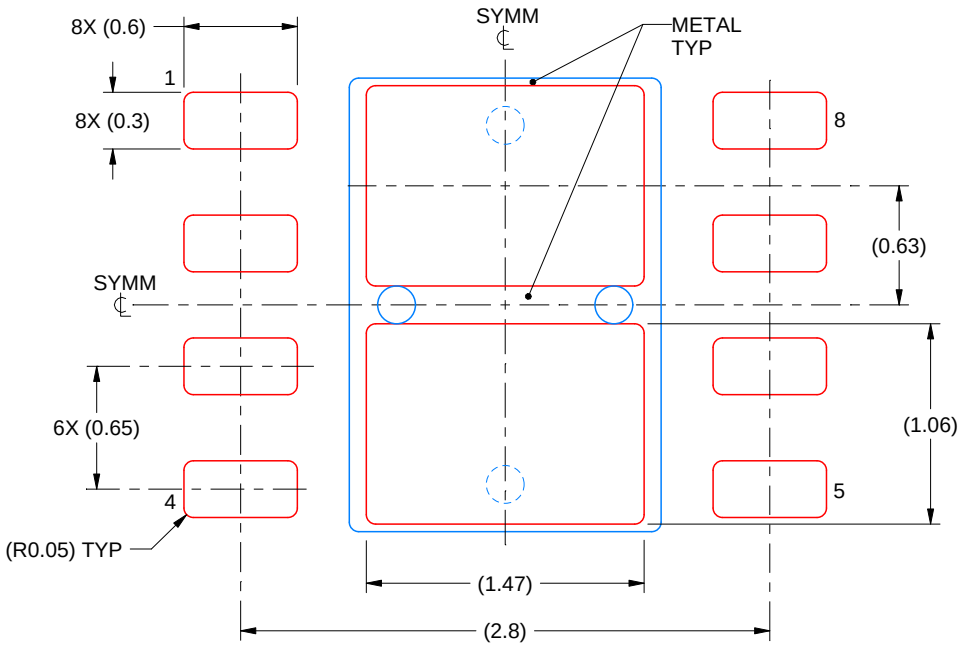


SOLDER MASK DETAILS

4218876/A 12/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

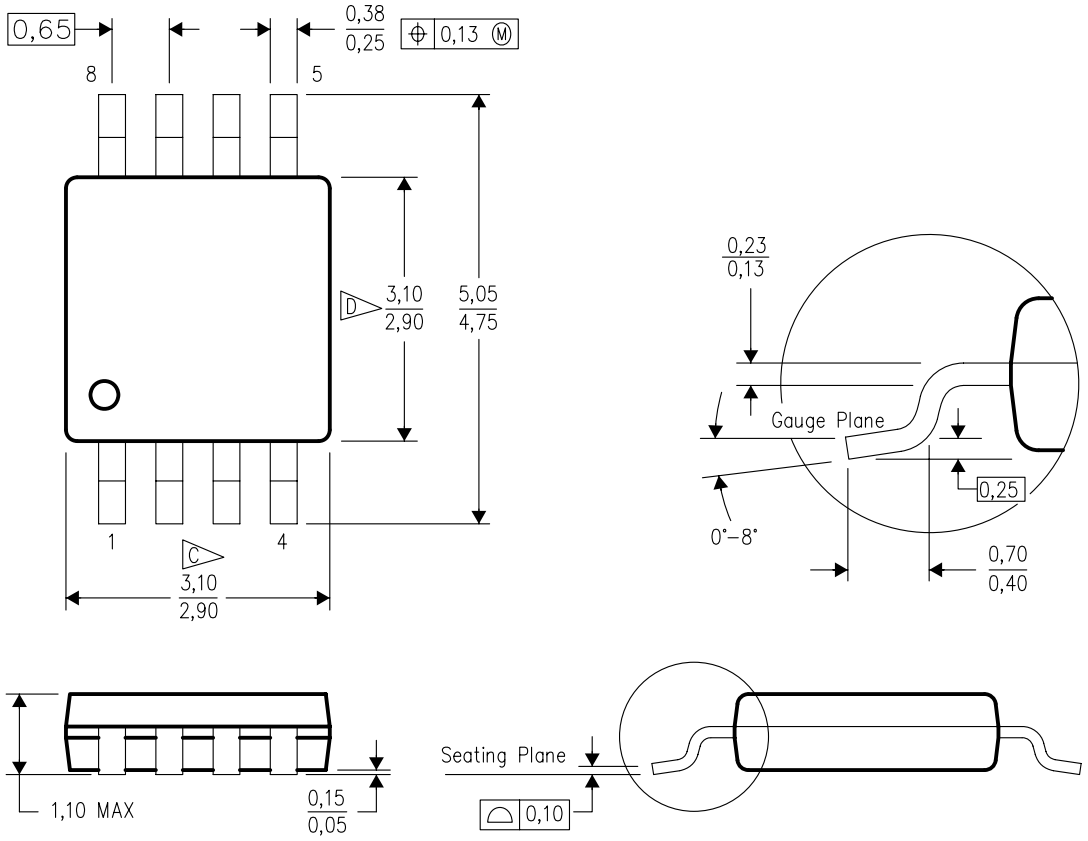
EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218876/A 12/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

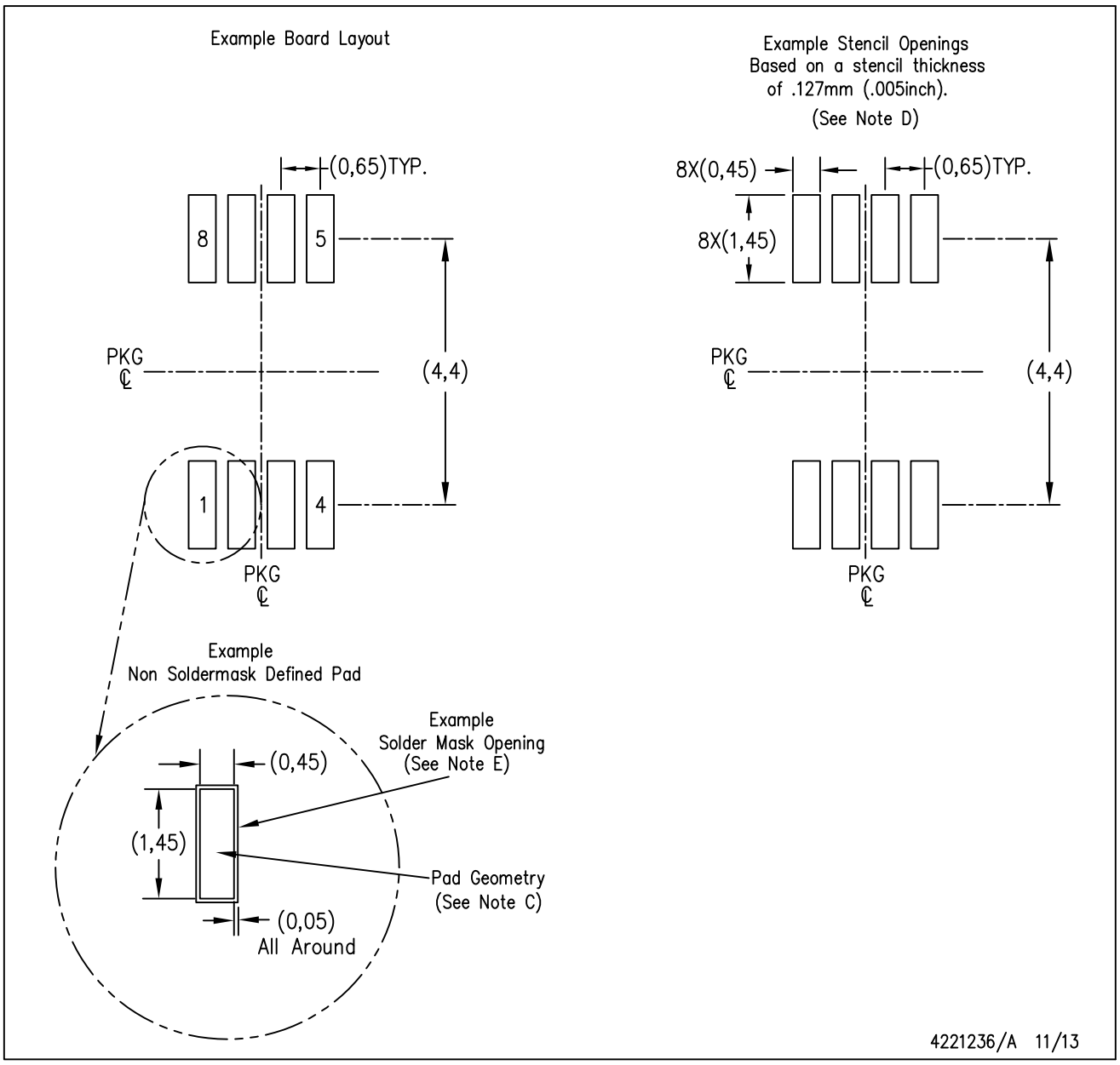
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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